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# A numerical study of partial-SOI LDMOSFETs

J.M. Park *, T. Grasser, H. Kosina, S. Selberherr

*Institute for Microelectronics, TU Vienna Gusshausstrasse 27–29, A-1040 Vienna, Austria*

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**Abstract**

The high-voltage and self-heating behavior of partial-SOI (silicon-on-insulator) LDMOSFETs were studied numerically. Different locations of the silicon window were considered to investigate the electrical and thermal effects. It is found that the potential distribution of the partial-SOI LDMOSFET with the silicon window under the drain is similar to that of standard junction isolation devices. With the silicon window under the source the potential distribution is similar to that of the conventional SOI LDMOSFET. Using the two-dimensional numerical simulator MINIMOS-NT, we confirm that the breakdown voltage of partial-SOI LDMOSFETs with a silicon window under the source is higher than that of partial-SOI LDMOSFET with a silicon window under the drain.


## 1. Introduction

Smart power ICs which monolithically integrate low-loss power devices and control circuitry, have attracted much attention in a wide variety of applications [1,2]. These ICs improve the reliability, reduce the volume and weight, and increase the efficiency of a system. Considerable effort has been spent on the development of smart power devices for automotive electronics, computer peripheral appliances, and portable equipment, such as cellular phones, video cameras, etc. Commonly used smart power devices are the lateral double diffused MOS transistors (LDMOSFETs) and lateral insulated gate bipolar transistors (LIGBTs) implemented in bulk silicon or SOI (silicon on insulator). New structures such as dual-gate oxide devices [3], LUDMOSFETs [4] and lateral super junction devices [5] are continuously proposed to improve the performance of the conventional lateral devices. One of the key issues in the realization of such 'smart power' technology is the isolation of power devices and low-voltage circuitry. SOI technology constitutes an attractive alternative to the traditional junction isolation. When high-voltage devices over 100 V are integrated on an SOI wafer, the isolation area between devices shrinks and lower leakage currents result in greatly improved high temperature performance. In general the breakdown voltage of an SOI structure is a function of the thickness of the silicon and the buried oxide layer [1]. The buried oxide helps to sustain a high electric field which results in a higher breakdown voltage. However, the operation of SOI power devices is limited by self-heating effects during switching and some fault conditions such as short circuit. Since the buried oxide underneath the device is a good thermal insulator, the temperature rise inside SOI power devices can be much higher than that of bulk silicon devices. Self-heating of SOI power devices can result in serious reliability problems during operation in a high temperature environment. To solve this problem, partial-SOI (P-SOI) technology was suggested [6,7], where a silicon window helps to reduce self-heating. In addition, potential lines spread into the substrate. Therefore it is possible to obtain higher breakdown voltages than those of conventional SOI devices, because the depletion layer in the substrate supports some voltage. This paper discusses the dependence of the breakdown voltage and temperature distribution on the location of the silicon window. We numerically confirm that the breakdown voltage of P-SOI LDMOSFET with a silicon window under the

* Corresponding author. Tel.: +43-1-58801-36033; fax: +43-1-58801-36099.
*E-mail address:* park@iue.tuwien.ac.at (J.M. Park).

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source is higher than that of P-SOI LDMOSFET with a silicon window under the drain.

## 2. Device structures

The schematic cross sections of the simulated devices are shown in Fig. 1–3. Generally, the breakdown voltage of the conventional SOI LDMOSFET is limited by the buried oxide thickness, SOI thickness and drift layer length. Fig. 1 shows a cross-sectional view of a conventional n-channel SOI LDMOSFET designed for breakdown voltage of 300 V with an SOI thickness $t_{soi}$ of 7 μm, and with a buried oxide thickness $t_{ox}$ of 2 μm. The drift region of the device is doped according to the RESURF principle [1] to achieve a maximum breakdown voltage. n-Channel P-SOI LDMOSFETs with a silicon window under the drain and under the source are shown in Figs. 2 and 3, respectively. As shown in the figures, silicon is used as a window instead of some part

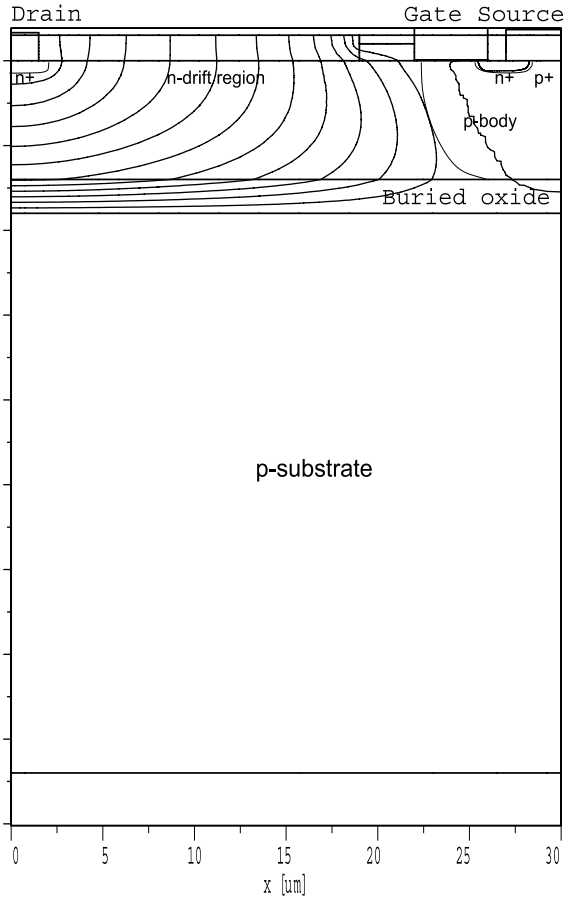


Fig. 1. Potential distribution of conventional SOI LDMOSFET.

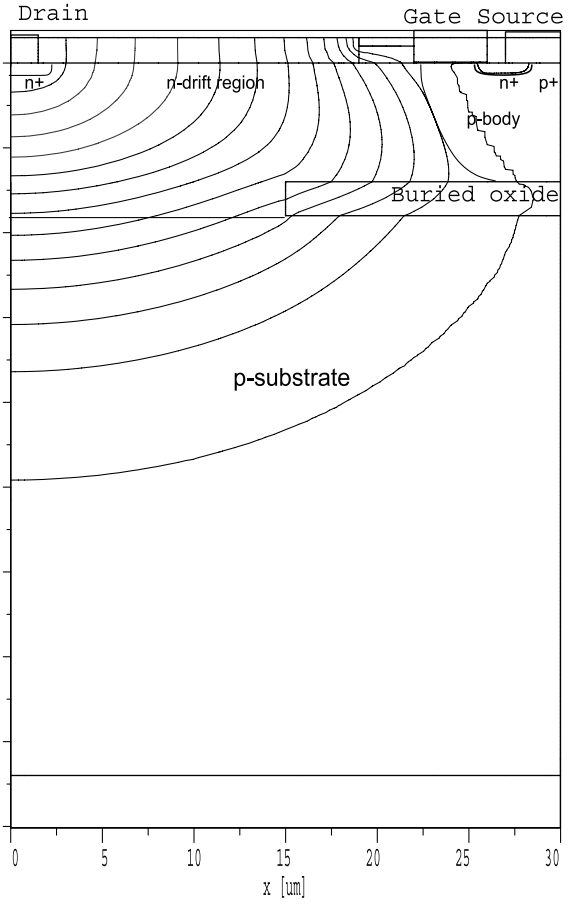


Fig. 2. Potential distribution of P-SOI LDMOSFET (silicon window: under drain).

of the buried oxide layer. The major variable parameters are the p-substrate doping concentration and the n-drift layer length. The $t_{soi}$, $t_{ox}$, and SOI layer doping concentration of the P-SOI LDMOSFETs are the same as those of the conventional SOI LDMOSFET shown in Fig. 1.

## 3. Simulation results

The main performance parameters for the smart power devices are the specific on resistance $R_{SP}$, and the breakdown voltage including thermal characteristics. $R_{SP}$ and breakdown voltage are inversely related to each other. Optimum design between breakdown voltage and $R_{SP}$ has been the main issue of these devices. P-SOI structures help to increase the breakdown voltage while maintaining $R_{SP}$, and reduce the self-heating problems by using high thermal conductive silicon as a window. The potential distribution of the conventional SOI

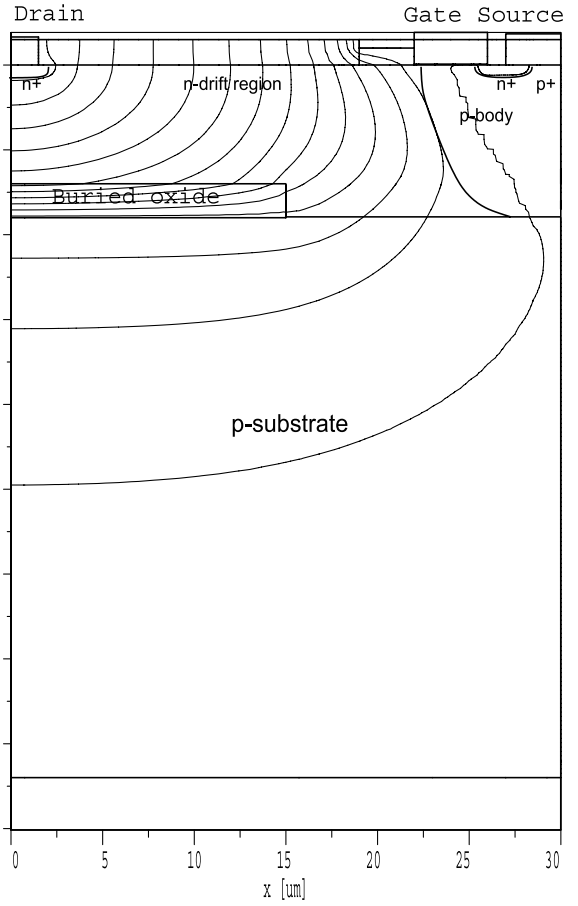


Fig. 3. Potential distribution of P-SOI LDMOSFET (silicon window: under source).

LDMOSFET and the P-SOI LDMOSFETs at breakdown are shown in Figs. 1–3, respectively. In the conventional SOI LDMOSFET, the buried oxide supports a large voltage, and it prevents potential lines from spreading into the substrate (Fig. 1). Almost all the voltage is supported by the buried oxide layer. The maximum electric field strength of buried oxide is determined by the electric field strength of silicon at the interface between the silicon and the buried oxide. To obtain a higher voltage with the thick film SOI LDMOSFETs, buried oxide or SOI layer thickness must be increased. As these parameters are increased to improve the breakdown voltage, thermal characteristics of the devices will be degraded. In the case of the P-SOI LDMOSFET, however, potential lines spread into the substrate. As shown in Fig. 2, the potential distribution of the P-SOI LDMOSFET with the silicon window under the drain is similar to that of standard junction isolation devices. Part of the voltage will be supported by the depletion layer in the substrate region. However, the buried oxide layer does not affect the breakdown voltage in this structure. The buried oxide is used only for the isolation of power devices and low-voltage circuitry. In the P-SOI LDMOSFET with the silicon window under the source (Fig. 3) the potential distribution in the buried oxide layer is similar to that of the conventional SOI LDMOSFET, so the buried oxide layer helps to increase the breakdown voltage together with the depletion region in the substrate. In addition, the temperature rise due to self-heating is reduced by the silicon window in the P-SOI LDMOSFETs. Two-dimensional numerical simulations with MINIMOS-NT [8] have been performed to investigate the influence of the window on the breakdown voltage and on the self-heating effects.

### 3.1. Breakdown voltage of P-SOI LDMOSFETs

The simulated breakdown voltages of P-SOI LDMOSFETs as a function of the substrate doping concentration $C_{sub}$ are shown in Fig. 4. The breakdown voltage increases with increasing $C_{sub}$ for the P-SOI with the silicon window under the drain, because the RESURF condition of the SOI structure is affected by $C_{sub}$. Below $C_{sub}$ of $4 \times 10^{14}$ cm$^{-3}$ in this structure, the breakdown voltage is lower than that of the conventional SOI LDMOSFET.

The solid lines in Fig. 5 show the electric field strength near the surface with substrate doping levels of $3 \times 10^{14}$ and $1 \times 10^{15}$ cm$^{-3}$, respectively. At the gate edge (near the lateral distance of 21 μm in Fig. 5), a high electric field can be seen with the low substrate doping concentration $C_{sub}$ of $3 \times 10^{14}$ cm$^{-3}$ and only a low electric field is found at the drain edge (near the lateral distance of 2 μm in Fig. 5). It means that the RESURF condition strongly depends on $C_{sub}$ in this structure. Further

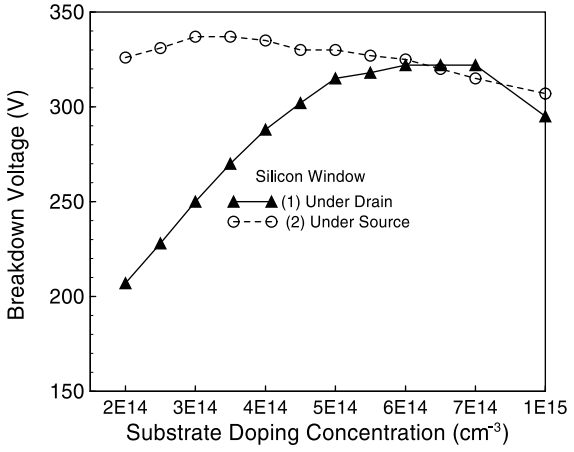


Fig. 4. Breakdown voltage versus substrate doping concentration of P-SOI LDMOSFETs ($L_d = 20$ μm).

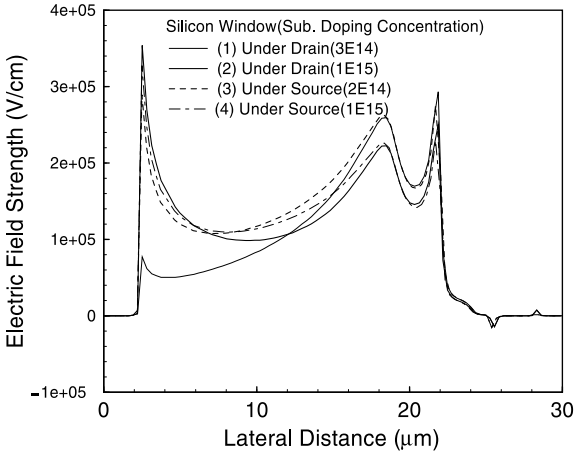


Fig. 5. Surface electric field strength for the two different silicon window positions.

increased $C_{sub}$ over $7 \times 10^{14}$ cm$^{-3}$ reduces the depletion layer width in the substrate region which decreases the breakdown voltage (solid line in Fig. 4). The buried oxide layer does not affect the breakdown voltage.

In the P-SOI with a silicon window under the source, the RESURF condition does not depend on the substrate doping concentration (from $2 \times 10^{14}$ to $1 \times 10^{15}$ cm$^{-3}$) as shown by the dashed lines in Figs. 4 and 5. However, the breakdown voltage decreases slowly with increasing $C_{sub}$ because of the reduced depletion layer width in the substrate region. Breakdown voltages versus n-drift layer length $L_d$ are shown in Fig. 6. The maximum breakdown voltage of the conventional SOI LDMOSFET is 300 V at $L_d = 20$ μm, and it does not change with increased n-drift layer length from 20 to 30 μm. The maximum voltage is limited by the RESURF condition of the SOI in this structure.

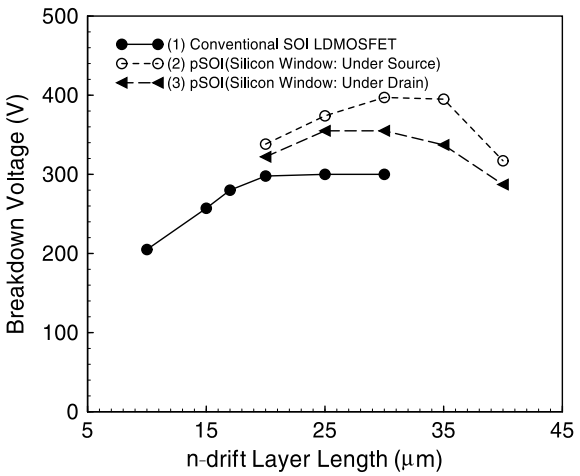


Fig. 6. Breakdown voltage versus n-drift layer length.

In the P-SOI with a silicon window under the drain, the breakdown voltage is determined by both the RESURF condition and depletion layer width of the substrate. The maximum breakdown voltage of this structure is 355 V at $C_{sub} = 6 \times 10^{14}$ cm$^{-3}$ and $L_d = 25$ μm. The improvement in the voltage handling capability is about 18%. Further increased $L_d$ over 30 μm decreases the breakdown voltage by the RESURF condition.

In the P-SOI with a silicon window under the source, both the buried oxide and depletion region of substrate help to increase the breakdown voltage. The maximum breakdown voltage of 397 V is obtained at $C_{sub} = 3 \times 10^{14}$ cm$^{-3}$ and $L_d = 30$ μm. The improvement in the voltage handling capability is about 32% compared to the conventional 300 V SOI LDMOSFET. Because the buried oxide and the depletion layer in the substrate region support the voltage, a higher breakdown voltage is obtained in this structure compared to that of the P-SOI with the silicon window under the drain.

### 3.2. Temperature dependence of the device characteristics and self-heating

Fig. 7 shows the leakage currents of P-SOI LDMOSFETs versus drain voltage as a function of the lattice temperature. The leakage current increases nearly exponentially with increasing temperature [9], because the space charge generation rate follows the intrinsic carrier density $n_i$. The shape of the leakage current does not change significantly with temperature, but the breakdown voltage increases. The increase of breakdown voltage is caused by the reduction of the mean free path of the carriers due to lattice scattering, requiring higher field for the carriers to initiate impact ionization. Generally, there are two components—a space charge generation

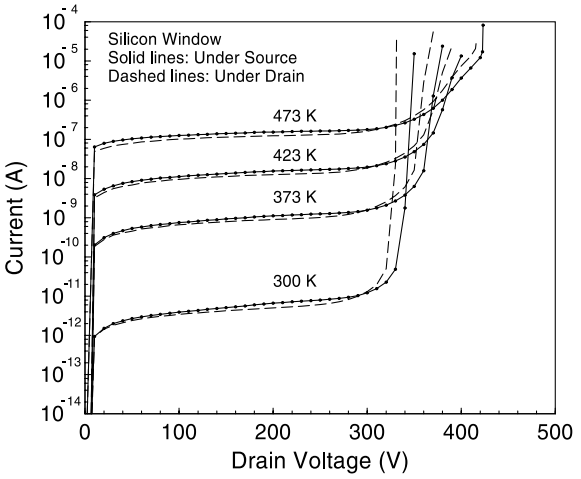


Fig. 7. Leakage current versus lattice temperature of P-SOI LDMOSFETs.

current and a diffusion leakage current—responsible for the leakage current under reverse bias conditions [10]. Diffusion leakage current will decrease with increasing the doping concentration. As shown in Figs. 2 and 3, the depletion layer widths of each P-SOI LDMOSFETs are almost the same. In the P-SOI with a silicon window under the drain, a higher substrate doping concentration was used to obtain the maximum breakdown voltage. Therefore, a lower leakage current (Fig. 7) is obtained compared to that in the P-SOI with a silicon window under the source. As shown in Fig. 8, the breakdown voltage shows a similar temperature dependence as conventional SOI LDMOSFETs but for P-SOI LDMOSFETs the slope is somewhat larger. This means that breakdown voltage characteristics of P-SOI LDMOSFETs are between SOI and junction isolated devices. The temperature distribution inside a device due to self-heating is determined by the heat generation profile and the thermal conduction inside the SOI LDMOSFETs [11]. In majority carrier devices such as MOSFETs, there is very little carrier recombination and as a result heat generation is mainly caused by Joule heating. This effect can be seen in SOI LDMOSFETs. It is proportional to the local resistances of the n-drift and channel region. Figs. 9 and 10 show the temperature distributions inside the P-SOI LDMOSFETs with an applied gate voltage $V_G$ of 15 V and a drain–source voltage $V_{DS}$ of 10 V. The bottom of the devices is assumed to be isothermal at 300 K. To reduce the simulation time, a substrate thickness of 36 μm is used. In these structures the silicon window acts as a good thermal conductor. In the P-SOI LDMOSFET with the silicon window under the drain, the temperature rise is highest in the gate region (310 K, white region in the figure) and decreases towards drain (308 K) as shown in Fig. 9. In the case of the P-SOI LDMOSFET with the silicon window under the source, the temperature rise is highest in the drain region (312 K) of the drift layer and decreases towards gate and source (307 K) as shown in Fig. 10. Fig. 11 shows a comparison of the temperature versus lateral distance under the surface for the conventional SOI LDMOSFET and the P-SOI LDMOSFETs. This figure shows that the silicon window in the P-SOI drastically reduces the temperature rise due to self-heating.

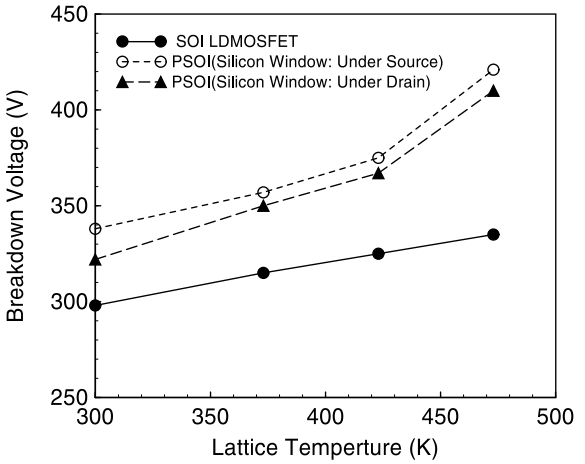


Fig. 8. Breakdown voltage versus lattice temperature ($L_d = 20$ μm).

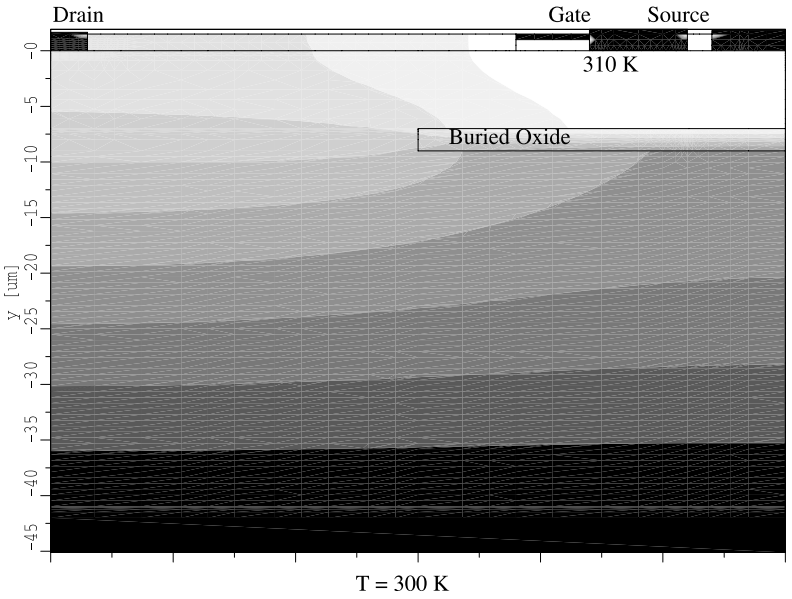


Fig. 9. Temperature distribution of a P-SOI LDMOSFET (silicon window: under drain).

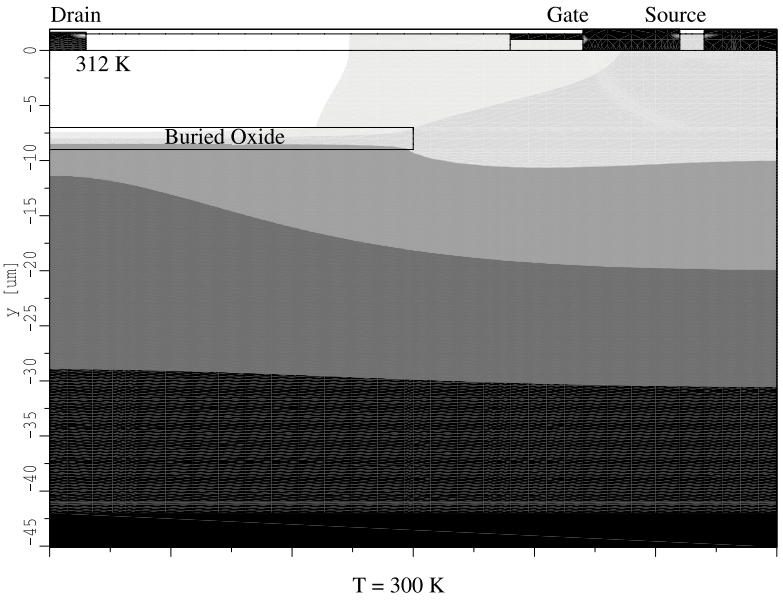


Fig. 10. Temperature distribution of a P-SOI LDMOSFET (silicon window: under source).

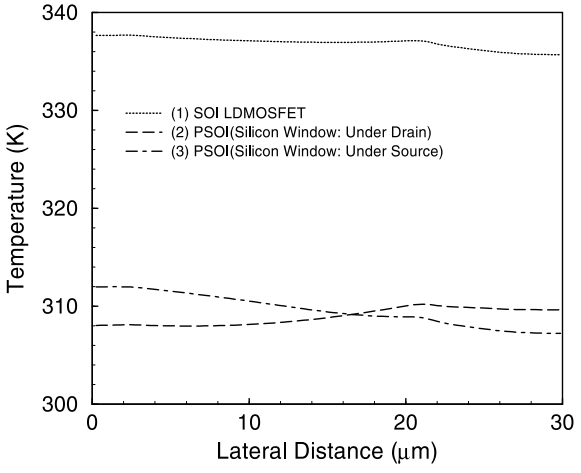


Fig. 11. Temperature versus lateral distance under top surface of the SOI structures.

## 4. Conclusions

We discussed the breakdown voltage and temperature dependence of P-SOI LDMOSFETs in terms of different locations of the silicon window. Our simulations confirmed that the breakdown voltage and self-heating effect of the P-SOI with the silicon window under the source is better than those of P-SOI with the silicon window under the drain. For the P-SOI LDMOSFET ($t_{soi} = 7$ μm and $t_{ox} = 2$ μm) with the silicon window under the drain, a maximum breakdown voltage of 355 V is obtained at $C_{sub} = 6 \times 10^{14}$ cm$^{-3}$ and $L_d = 25$ μm. For the P-SOI LDMOSFET with the silicon window under the source, a maximum breakdown voltage of 397 V is obtained at $C_{sub} = 3 \times 10^{14}$ cm$^{-3}$ and $L_d = 30$ μm. The improvement in the voltage handling capability is about 32% compared to conventional 300 V SOI LDMOSFET. Since the buried oxide and the depletion layer in the substrate region support the voltage, a higher breakdown voltage is obtained in this structure compared to that of a P-SOI with a silicon window under the drain.

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