A Parallel-Connected Single Phase Power Factor Correction Approach With Improved Efficiency

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***Abstract*—In this paper, a new parallel-connected single phase power factor correction (PFC) topology using two flyback converters is proposed to improve the output voltage regulation with simultaneous input power factor correction and control. This approach offers lower cost and higher efficiency by parallel processing of the total power. Flyback converter-I primarily regulates output voltage with fast dynamic response and processes 55% of the power. Flyback converter-II with ac/dc PFC stage regulates input current shaping and PFC, and processes the remaining 45% of the power. This paper presents a design example and circuit analysis for 200 W power supply. A parallel-connected interleaved structure offers smaller passive components, less losses even in continuous conduction inductor current mode, and reduced volt-ampere rating of dc/dc stage converter. TI-DSP, TMS320LF2407, is used for implementation. Simulation and experimental results show the performance improvement.**

***Index Terms*—Circuit analysis, PFC.**

I. Introduction

MODERN switching power converters require many features such as

1) high power factor;
2) lower harmonic content;
3) fast dynamic response;
4) low losses;
5) low cost;
6) simple control;
7) low EMI;
8) wide input voltage range;
9) isolation;
10) ride-through and hold-up time capability;
11) compact: size and weight.

A number of power factor correction circuits have been developed recently [1]–[5]. Normally a boost converter is employed for PFC with dc/dc stage to improve performance or a flyback converter is used to reduce the cost. Although both boost converter and flyback converter are capable for PFC applications [6], [7], the main difficulty in two-stage scheme employing a PFC boost and a dc/dc converter is the high cost and lower efficiency. However, single-stage method using the simplest flyback converter is not able to tightly regulate the output voltage.

In this paper, parallel-connected PFC approach is proposed to overcome the disadvantages of the two schemes in cascade (ac to dc and dc to dc) as well as to meet the design requirement as mentioned. The proposed scheme employs two flyback converters. The purpose of flyback converter-I with 55% power rating is to regulate output voltage and converter-II with 45% power rating is able to regulate input current. The flyback converter-II operates with continuous conduction mode (CCM) in input inductor current. The input diode current of the flyback converter-I has tailed waveform in which reverse recovery loss can be minimized [8], [9]. The goal of the proposed PFC scheme is to reduce the passive component size, to employ lower rated semiconductor, and to improve total efficiency. Simulation results show that the proposed topology is capable of offering good power factor correction and fast dynamic response.

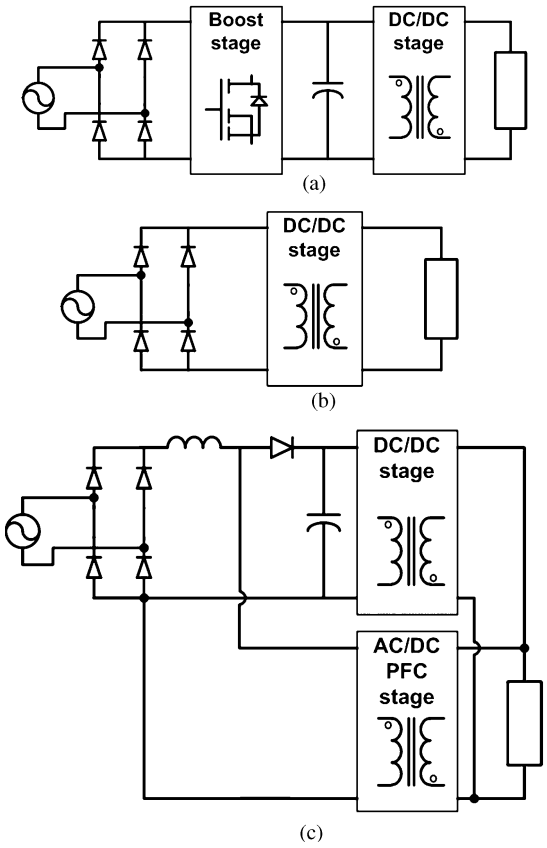

Fig. 1. Possible PFC schemes.

II. Single- and Two- Stage PFC Schemes

Fig. 1 shows the possible two-stage and single-stage PFC schemes. Both boost converter and flyback converters are suitable for the PFC applications. A two-stage scheme shown in Fig. 1(a) is mainly employed for the switching power supplies

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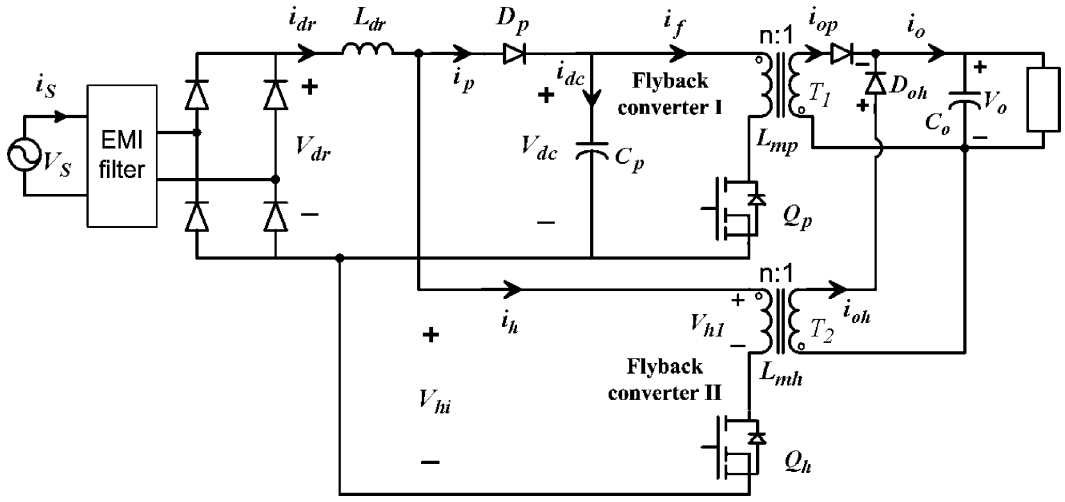

Fig. 2. Proposed parallel-connected single-stage PFC scheme with two flyback converters.

since the boost stage can offer good input power factor with low total harmonic distortion (THD) and regulate the dc-link voltage and the dc/dc stage is able to obtain fast output regulation without low frequency ripple due to the regulated dc-link voltage [10]. These two power conversion stages are controlled separately. However, two-stage scheme suffers from higher cost, complicated control, low-power density, and lower efficiency.

For low power applications, where cost is a dominant issue, a single-stage scheme using the flyback converter [Fig. 1(b)] is more attractive than a two-stage scheme due to the following advantages.

1) Simplified power stage and control circuit (low parts count, low-cost design).
2) Provides isolation and multi-output.
3) Start-up and short circuit protection is done by a single switch.
4) Higher cost electrolytic capacitor in two-stage scheme can be replaced by a small-size film capacitor.
5) No output filter inductor is necessary.

A single-stage scheme [Fig. 1(b)], on the other hand, cannot provide good performance in terms of ride-through or hold-up time since it mainly regulates input current with rectified voltage input and also output voltage is normally too small to provide hold-up time. Therefore, most of flyback converters need a large electrolytic capacitor at the output terminal to reduce the second harmonic ripple. But its transient response is still poor. The limitation of the flyback PFC is the output power level and the high breakdown voltage is required for the switch. When the output power increases, both voltage and current stress increase. Due to the high ripple currents the flyback is less efficient than other designs. That is why the two-stage scheme is more attractive for higher power rating.

At higher power levels, since it may be beneficial to parallel two or more flyback converters rather than using a single higher power unit, a parallel-connected scheme is proposed as shown in Fig. 1(c). This approach can offer fast output voltage regulation and high efficiency. The flyback converter-I with dc/dc stage can offer good output voltage regulation due to the pretty dc input voltage and the flyback converter-II with ac/dc PFC stage fulfills input current regulation to obtain highly efficient power factor. The advantages of the proposed approach are as follows.

1) This scheme offers good input power factor and output regulation.
2) Input inductor and dc-link capacitor can be smaller.
3) The power rating of flyback converter-I is lower than that of two-stage structure due to low dc-link voltage and lower current rating.
4) The diode reverse recovery losses can be minimized due to the tailed operating mode in diode current.

III. Operation of the Proposed Topology

Fig. 2 shows the proposed parallel-connected PFC scheme which employs a diode rectifier, dc-link capacitor, and two flyback converters. The function of a flyback converter-I with an electrolytic capacitor is to support output voltage regulation. A flyback converter-II fulfills the function of power factor correction by making input current sinusoidal and regulating dc-link voltage. The operation of the flyback converter-II is given in this paragraph considering that the flyback converter-I operates ideally. The converter-II operates with continuous conduction mode in both an input inductor and a flyback transformer. The dc-link voltage V_{dc} in this scheme can be lower than other schemes as

$$V_{dc}^{*} = \sqrt{2}V_s. \tag{1}$$

The transfer function of the flyback converter is expressed by defining a conversion ratio M as the ratio of the dc output voltage to the input voltage

$$M = \frac{V_o}{V_{dr}} = \frac{D}{n(1-D)} \tag{2}$$

where, D is the duty ratio of the switch Q_h, $n(= \mathrm{Np}/Ns)$ is defined as the ratio of Np to Ns, and Np and Ns denote the number of turns of primary and secondary side, respectively. The operational waveforms are shown in Fig. 3. To analyze the

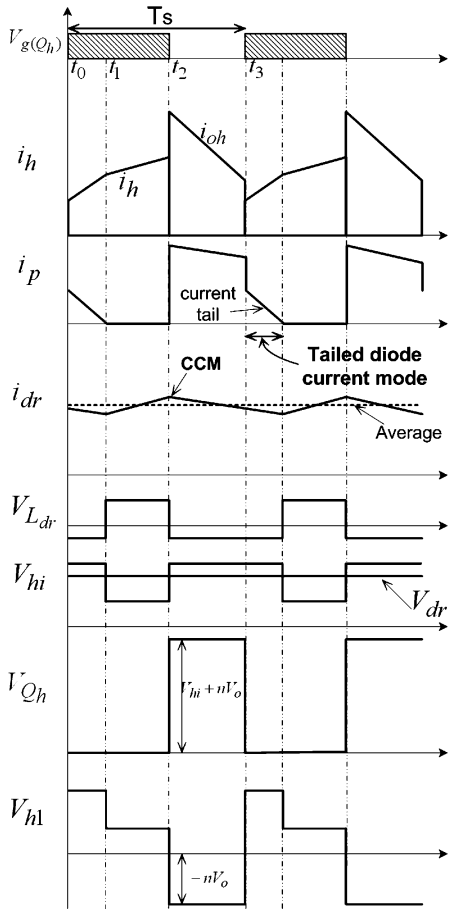

Fig. 3. Operational waveforms of the proposed topology.

circuit parameters, basic equations for voltages and currents are given by

$$i_{dr} = i_p + i_h, \tag{3}$$

$$V_{L_{dr}} = L_{dr}\frac{di_{dr}}{dt}, \tag{4}$$

$$V_{hi} = V_{dr} - V_{L_{dr}}, \tag{5}$$

$$V_{h1} = V_{hi} - V_{Q_h} \tag{6}$$

where, i_{dr}, i_p, and i_h are the rectified, flyback converter-I, and converter-II input currents on dc side. V_{Ldr}, V_{hi}, V_{dr}, V_{h1}, V_{Qh}, and V_o are the input inductor, flyback converter-II input, rectified input, transformer primary winding, switch, and output voltages, respectively. Since the two input currents, i_p and i_h, are interleaved, input current, i_{dr}, ripple can be significantly reduced. The operational sequences are as follows.

$t_0 - t_1$: The current of flyback transformer does not flow simultaneously in both windings. When the switch Q_h is turned on at t_0, V_{Qh} becomes zero and diode D_{oh} is turned off with a reverse bias. The voltage across the diode D_{oh} equals to $V_o + V_{hi}/n$. Energy, $0.5L_{mh}I^2$, is charged in the magnetic field in the primary winding of the flyback transformer. Primary current, i_h, ramps up from the remaining magnetizing current and reaches i_{dr} with the slope (V_{hi}/L_{mh}), i_p decreases with a slow current tail, and i_{dr} slowly decreases until i_p reaches zero.

t_1–t_2: The primary current increases by $V_{dr}/(L_{mh}+L_{dr})$.

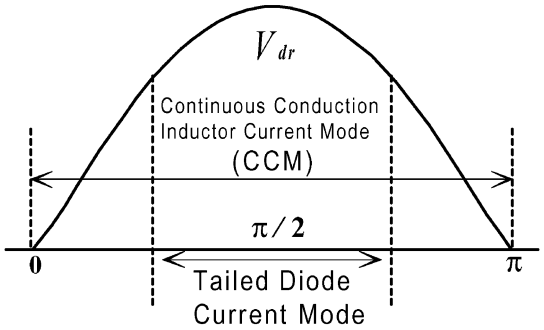

Fig. 4. Operation modes in input inductor and diode current.

$t_2 - t_3$: When the switch Q_h is turned off, D_{oh} is turned on with forward bias. The current in the primary winding ceases to flow. The stored energy is transferred to the secondary winding. At this time, the switch voltage, V_{Qh}, becomes $V_{hi}+nV_o$, i_p becomes i_{dr} and decreases depending on input voltage, and the secondary current i_{oh} decreases with the slope (n^2V_o/L_{mh}).

The current slope through the magnetizing inductor when the switch Q_h is turned off is given as

$$\Delta i_{mh} = -\frac{nV_o}{L_{mh}}T_{off} \tag{7}$$

where, T_{off} is the turn-off time. Similarly, the change of the flyback converter-II input current i_p through a diode is

$$\Delta i_p = -\frac{V_{dc} - v_{dr}}{L_{dr}}T_{off}. \tag{8}$$

Based on two slopes of i_{mh} and i_p, the tailed diode current mode in which the diode current has current tail is defined as shown Fig. 4 when the slope of i_{mh} is greater than that of i_p

$$v_{dr} > \frac{L_{mh}V_{dc} - nV_oL_{dr}}{L_{mh}}. \tag{9}$$

In continuous conduction input inductor current mode, when the MOSFET Q_h is switched on, the diode D_p is forced into reverse recovery at a high rate of change in the diode current i_p. In this tailed mode operation, however, the diode current slowly decreases so that the reverse recovery effect can be minimized.

To analyze the flyback converter-II operation, an open loop duty ratio is obtained from (2) as

$$D_{open,h} = \frac{nV_o}{v_{dr} + nV_o} \tag{10}$$

where, input voltage $v_{dr} = \sqrt{2}V_s\,|\sin\omega t|$. Assuming two input currents of each converter have the waveforms shown in Fig. 5, two currents depend on the duty ratio from (10)

$$i_h = \frac{T_{on}i_{dr}}{T_s} = D \cdot i_{dr} \tag{11}$$

$$i_p = (1 - D) \cdot i_{dr} \tag{12}$$

where, input current $i_{dr} = \sqrt{2}I_s\,|\sin\omega t|$.

Therefore, two currents can be obtained

$$i_h = \frac{\sqrt{2}nV_oI_s\,|\sin\omega t|}{\sqrt{2}V_s\,|\sin\omega t| + nV_o} \tag{13}$$

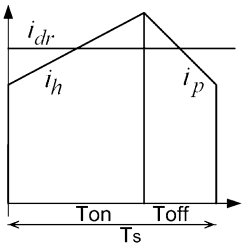

Fig. 5. Current waveforms in switching period.

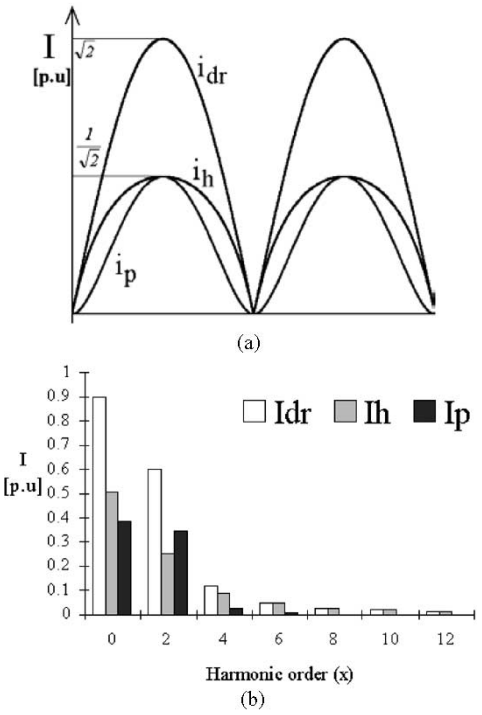

Fig. 6. Input current analysis ($I_{dr,rms} = 1$ [p.u], $I_{,h,rms} = 0.55$ [p.u], $I_{,p,rms} = O.46$ [p.u]).

$$i_p = \sqrt{2} I_s \left|\sin \omega t\right| \left\{ 1 - \frac{nV_o}{\sqrt{2} V_s \left|\sin \omega t\right| + nV_o} \right\} = \sqrt{2} I_s \left|\sin \omega t\right| - i_h. \tag{14}$$

Fig. 6 shows those current waveforms and harmonic components. Now, instantaneous powers through the diode D_p and the transformer T2 are calculated by using the input inductance and the magnetizing inductance

$$P_{p,pu} = \frac{L_{mh} + L_{dr}}{2L_{mh} + L_{dr}} \text{ [p.u]} \tag{15}$$

$$P_{h,pu} = \frac{L_{mh}}{2L_{mh} + L_{dr}} \text{[p.u]} \tag{16}$$

where, L_{mh} and L_{dr} denote the magnetizing inductance of T2 and input inductance, respectively, and the input total power $P_{in,pu} = P_{p,pu} + P_{h,pu} = 1$ [p.u]. On the other hand, by employing the open loop duty ratio $D_{open,h}$, two instantaneous powers can be derived by

$$P_p = V_{dc} \cdot i_p = \sqrt{2} V_s \left[\sqrt{2} I_s \left|\sin \omega t\right| - i_h \right] \tag{17}$$

$$P_h = P_{in} - P_p \tag{18}$$

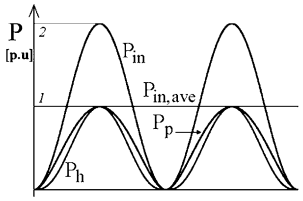

Fig. 7. Instantaneous powers (Pp: 0.547 [{\hbox{ p.u}}], Ph: 0.453 [{\hbox{ p.u}}], Pin: total power).

where, $P_{in} = V_s I_s \{1 - \cos 2\omega t\}$. The instantaneous powers are shown in Fig. 7. The relations between two inductances and two input average powers of two converters are expressed as

$$\frac{L_{mh} + L_{dr}}{L_{mh}} = \frac{P_{p,ave}}{P_{h,ave}} \tag{19}$$

$$L_{dr} = L_{mh} \left\{ \frac{P_{p,ave}}{P_{h,ave}} - 1 \right\}. \tag{20}$$

The output currents of the two flyback transformers are given by turns ratio

$$i_{op} = n \cdot i_f \qquad i_{oh} = n \cdot i_h. \tag{21}$$

Since the output load current i_o may contain only dc and switching frequency components, the harmonic contents for the primary current of the flyback converter-I is expressed as

$$i_o = i_{op} + i_{oh} = \frac{V_s I_s}{V_o}, \tag{22}$$

$$i_{f,x} = i_{h,x} \tag{23}$$

where, $x(= 2, 4, 6, \text{etc.})$ is harmonic order. From (23), the dc-link capacitor current can be estimated as a second harmonic

$$i_{dc,2} = -(i_{p,2} + i_{h,2}) \cos 2\omega t. \tag{24}$$

Therefore, the voltage ripple of the dc-link capacitor is obtained as

$$V_{dc,ripple} = -\frac{i_{p,2} + i_{h,2}}{2\omega C_p} \sin 2\omega t \tag{25}$$

where, C_p is the capacitance of the dc-link capacitor.

IV. Converter Controls

To control the proposed approach, two control stages are required for PFC and output voltage regulation as shown in Fig. 8. Flyback converter-II is regulated by a conventional PFC controller which consists of inner input current loop and outer dc-link voltage to obtain high power factor [Fig. 8(a)]. DC-link voltage is $1.414^* V_s$, which is better to reduce the voltage across drain-source of MOSFET Q_p [11]. Based on the PFC controller, a feed-forward control block is added to improve input current shape. Since the open loop duty ratio $D_{open,h}$ of the converter-II is calculated from (10), the final duty ratio for the switch gate input is obtained as

$$D_h = D_{open,h} + D_{pi} \tag{26}$$

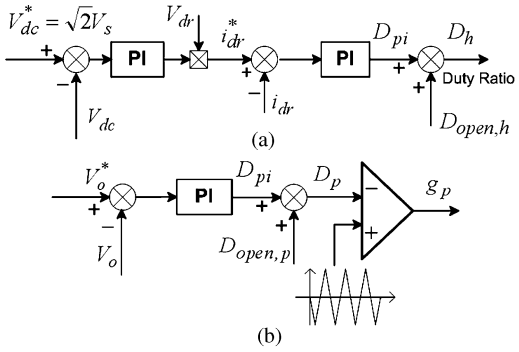

Fig. 8. Control block diagrams.

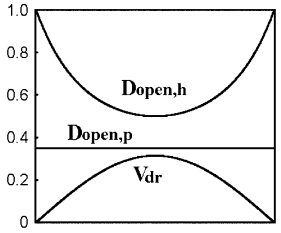

Fig. 9. Open loop duty ratios for two flyback converters.

where, D_{pi} is the closed loop duty ratio obtained from PI current controller. The output D_{pi} of the PI current regulator containing a small amount of variations provides the correction to the final duty ratio. On the other hand, output voltage V_o control is achieved by flyback converter-I. Fig. 8(b) shows a simple PI voltage controller with a open loop duty ratio $D_{open,p}$ which is calculated similarly to $D_{open,h}$ in terms of power ratings of each converter

$$D_{open,p} = \frac{nV_oP_{p,pu}}{V_{dc} + nV_oP_{p,pu}}. \tag{27}$$

Final duty ratio D_p is obtained by adding the duty ratio D_{pi} from controller with $D_{open,p}$. Two open loop duty ratios are plotted in Fig. 9. The output voltage control response is much faster than single stage scheme since two converters are employed for separate control function.

V. Design Example

The proposed PFC circuit is designed according to the following parameters.

Total output power (Po) $= 200$ [W] $= 1$ [p.u].
Input voltage (Vs) $= 120$ [V] $= 1$ [p.u].
Output voltage (Vo) $= 48$ [V] $= 0.4$ [p.u].
Input current (Is) $= 200/120 = 1.67$ [A] $= 1$ [p.u].
Base impedance (Zb) $= 120/1.67 = 72[\Omega] = 1$ [p.u].
Line frequency $= 60$ [Hz]
Switching frequency $= 37$ [kHz].
Output dc capacitance (Co) $= 1$ [$/hboxmF$] $= 27$ [p.u].
Transformer turns ratio $= 3.5{:}1$.

Flyback Converter-I

Power rating $= 109.4$ [W] $= 0.547$ [pu].
Magnetizing inductance (Lmp) $= 0.5$ [mH].
DC capacitance (Cp) $= 660$ [uF] $= 17.9$ [p.u].
DC-link voltage (Vdc) $= 169$ [Vdc] $= 1.414$ [p.u].

TABLE I
Comparison Between Two-Stage PFC and the Proposed Scheme (200 W, 48 Vdc)

	Two-stage PFC scheme	**Parallel PFC scheme**
Input inductance (Ldr)	1.5mH	0.3mH
Dc-link capacitor rating	220V	169V
PFC switch rating (Qh)	0.8A/220V	0.8A/340V
PFC diode (Dp)	0.9A/220V	0.9A/169V
Reverse recovery loss on Dp	High	Small
Transformer rating[p.u]	1[p.u]	About 1.1[p.u]
Dc/dc converter power rating	0.9A,220V,200W	0.7A,169V,118W
Dc/dc switch rating (Qp)	0.9A/440V	0.7A/340V
Output diode currents	4.2A	4.5A
Output capacitor rating	48V	48V
Total efficiency	80%	86%

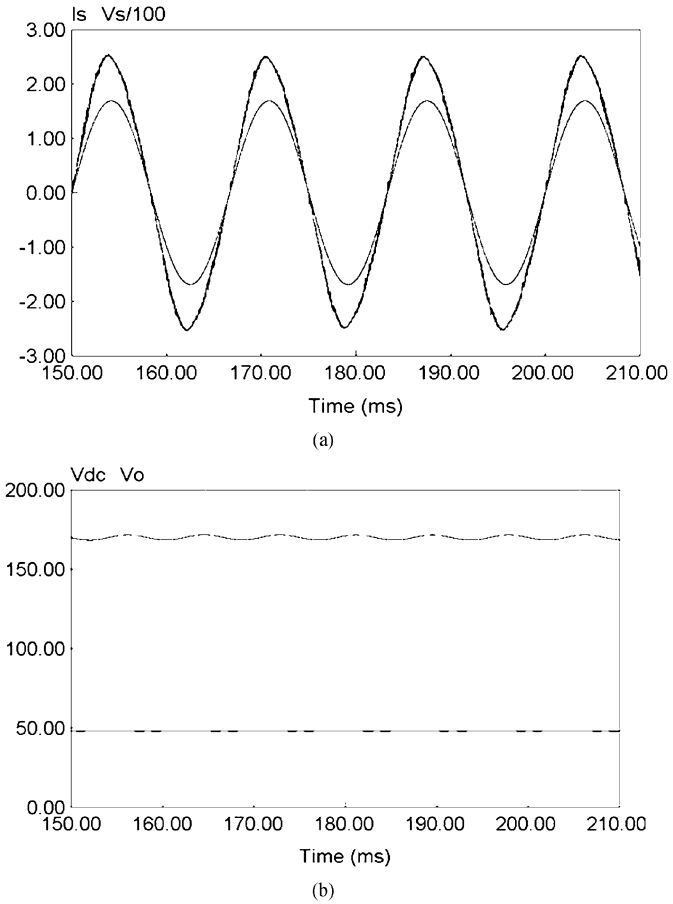

Fig. 10. Simulation results of the proposed approach.

Flyback Converter-II

Power rating $= 90.6$ [W] $= 0.453$ [p.u].
Magnetizing inductance (Lmp) $= 1.2$ [mH].

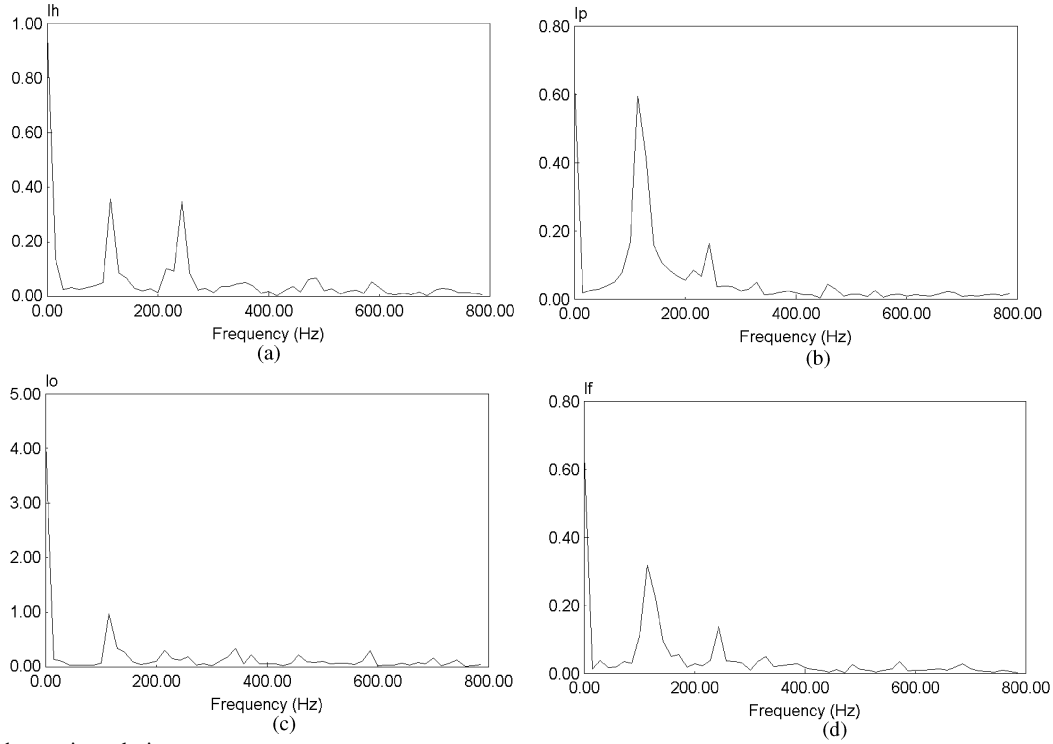

Fig. 11. Current harmonic analysis.

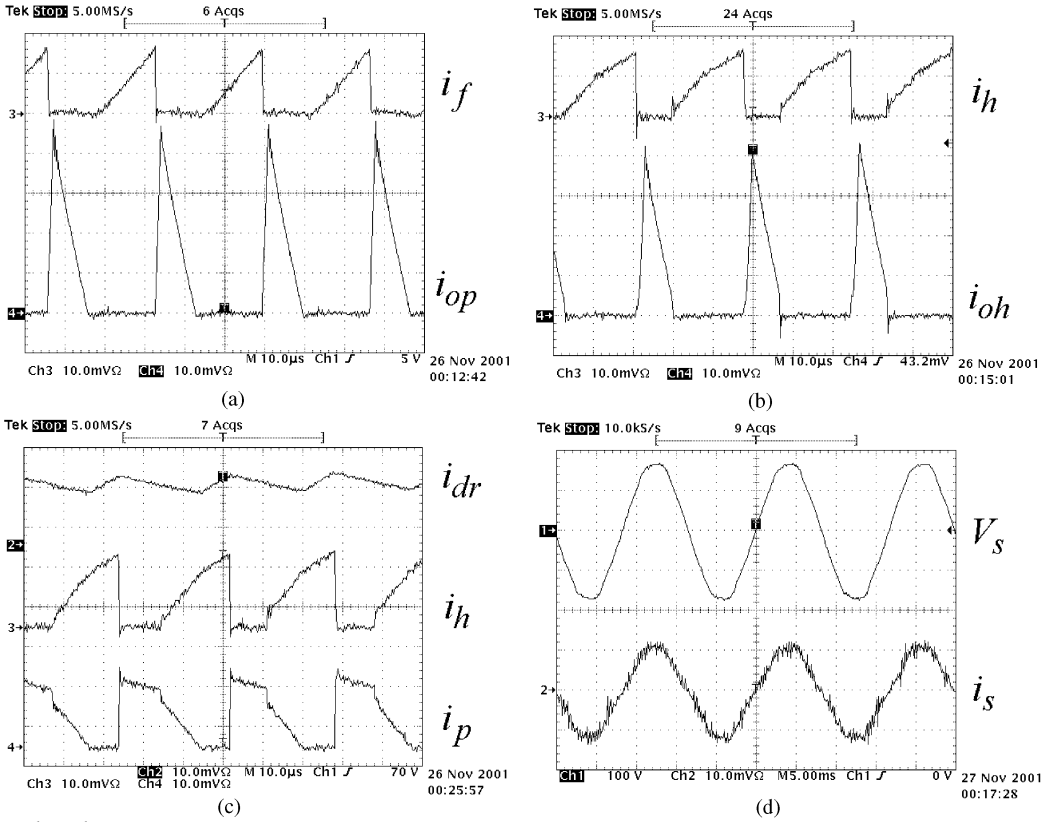

Fig. 12. Experimental results.

The input inductance L_{dr} is calculated from (20)

$$L_{dr} = 0.0012 \times \left\{ \frac{0.547 - 0.453}{0.453} \right\} = 249 \text{ [uH]}$$
$$\approx 300 \text{ [uH]} = 0.16 \text{ [p.u]}. \quad (28)$$

Now, we can evaluate the proposed approach comparing with the general two-stage scheme employing PFC boost converter and dc/dc stage. In two-stage, the input inductance is $L_{dr} + L_{mh} = 1.5$ [mH], dc-link voltage is much higher than 1.414* Vs, the power rating of dc/dc stage is 1 [{\hbox{ p.u}}], and the

diode reverse recovery loss is critical due to CCM. On the other hand, the proposed scheme provides small input inductor since the inductor current depends on $L_{dr} + L_{mh}$, dc-link voltage is smaller so that the voltage stress on the switch of the flyback converter-I is less, the power rating of dc/dc stage is a bit higher than average power P_p due to lower harmonic components, and the diode reverse recovery loss is minimized because of the tailed diode conduction mode. The comparison between two-stage and the proposed scheme is summarized in Table I. For the two-stage scheme, it is assumed that dc-link voltage is 220 V, continuous conduction inductor current mode, and the expected efficiency is 80% (91% PFC stage, 88% dc/dc stage efficiencies).

VI. Simulation and Experimental Results

The simulation results of the proposed topology are shown in Fig. 10. Unity power factor and tight output voltage (48 V) regulation can be achieved. The dc-link voltage is $1.414^{*}\mathrm{Vs} = 169$ V, and the voltage ripple of the dc-link is 3.4 V which mainly depends on the dc-link capacitance. Fig. 11 shows the analysis of the circuit currents. The currents i_h and i_p are similar to those of the two-stage scheme. The primary side current of flyback converter-I has 2^{rd} and fourth harmonics due to the harmonics on the flyback converter-II. Two control systems are implemented by using TI-DSP, TMS320LF2407 just to prove the proposed scheme. Experimental results from prototype circuit are shown in Fig. 12. Flyback converter-I has DCM operation while converter-II operates with CCM. In the diode current, current tail is appeared when the diode is turned off. 5% input current THD and 86% efficiency are obtained.

VII. Conclusion

A parallel-connected single phase power factor correction (PFC) topology using two flyback converters has been proposed. It has been shown that output voltage regulation is achieved by dc/dc stage and the input power factor correction is achieved by ac/dc PFC stage. These two power stages have 55% and 45% power sharing, respectively. The proposed approach offers the following advantages: smaller size passive components, lower voltage-ampere rating of dc/dc stage, and higher efficiency. Simulation and experimental results demonstrate the capability of the proposed scheme.

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