A Partial-Current-Steering Biphasic Stimulation Driver for Vestibular Prostheses

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***Abstract*—This paper describes a novel partial-current-steering stimulation circuit for implantable vestibular prostheses. The drive hardware momentarily delivers a charge-balanced asymmetric stimulus to a dummy load before steering towards the stimulation electrodes. In this fashion, power is conserved while still gaining from the benefits of current steering. The circuit has been designed to be digitally programmable as part of an implantable vestibular prosthesis. The hardware has been implemented in AMS 0.35 μm 2P4M CMOS technology.**

***Index Terms*—Artificial electrical stimulation, biphasic, bipolar, continuous interleave sampling, current-steering, neural stimulation, neuroprosthetic, vestibular prosthesis.**

I. Introduction

ARTIFICIAL electrical stimulation, a methodology becoming increasingly accepted in the medical community, is providing engineers and medical professionals a reliable method to interface to neural tissue. Neural prostheses are already benefitting those with profound hearing loss, cardiac arrythmia, loss of muscular function, hand grasp, foot drop, bladder control, and soon those with loss of vision. A key component in such systems is the neural interface and stimulation drive hardware. Reliability and robustness are paramount, and ensuring good efficiency and minimizing neural fatigue ensures long-lasting rehabilitation.

Restoring the sensation of inertia in individuals with balance-related impairments is achievable through development of an artificial vestibular prosthesis, based on the cochlear implant paradigm. The inner ear's vestibular system provides cues about self-motion and help stabilize vision during movement. Damage to this system can result in dizziness, imbalance, blurred vision, and instability in locomotion, a leading cause of death in the elderly. Restoration of balance can, therefore, be achieved by bypassing a dysfunctional element in the vestibular pathway using artificial stimulation. A vestibular prosthesis would incorporate miniature (MEMS-based) inertia sensors, suitable sensor interfacing circuits, a semicircular canal processor and stimulation driver. Research in developing artificial vestibular prostheses has recently gained much momentum, with a number of groups [1]–[3] implementing discrete electronics for inertia sensing, processing, and neural stimulation.

This work aims to implement an integrated hardware solution towards a single chip semicircular canal stimulator based on techniques used within cochlear prosthetics. This paper presents a novel CMOS-based integrated circuit for artificial neural stimulation as part of an implantable vestibular prosthesis. The paper is organized as follows—Section II provides some theoretical background regarding stimulation parameters, while Section III outlines the system architecture. Section IV describes the implementation at circuit level and Section V presents the measured results. Finally, Section VI summarizes and discusses the various features of the presented work.

II. Stimulation Theory

Typically, in electrical neural stimulation, a minimum of two electrodes are used to produce a nerve activation current. The pair can be used in a monopolar (shared reference electrode) or a bipolar (individual electrode pairs) configuration [4]. For applications requiring greater activation selectivity, the bipolar scheme is preferred because each pair generates a more localized field (compared to monopolar) [5], [6]. However, bipolar stimulation schemes typically consume higher power due to increased shunting currents. Stimulus pulse parameters include frequency, amplitude and duration. The former affects the smoothness of perceived sensation and needs to be adjusted to prevent neural fatigue. The latter two parameters affect the strength of the neural response and alter the charge injected. Another issue to consider is the stimulus drive mechanism, i.e., by what means the stimulus is delivered to the target site. The three methods are: voltage-mode, current-mode, and charge-mode [7]. Although different systems may be based on different mechanisms, we consider this to be an implementation issue; as the underlying goal is to deliver (and then remove) a well-defined charge packet.

As established by [8], in order to avoid harmful electrochemical processes, the stimulus waveform has to be biphasic. In such a waveform the first pulse causes activation, followed by a second one with opposite polarity to balance the charge delivered by the first [9]. However, it has been reported [10] that two opposite pulses back to back could act to prevent the generation of an action potential, or could require more energy to produce an action potential. To overcome this, a short time delay needs to be introduced between the pulses. This delay allows the action

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potential to propagate away from the stimulation site before the electrode recovers the injected charge. Additionally, using an extended anodic pulse with reduced amplitude can compensate for charge distribution and thus reduce fatigue. The various aspects of the waveform profile are discussed in [11].

III. System Overview

This system implements a 3-channel biphasic current-mode stimulation drive with digitally programmable signal conditioning for a fully-implantable vestibular prosthesis [12] using a bipolar electrode configuration. Due to the close proximity between adjacent stimulation sites, the system incorporates a continuous interleave sampling (CIS) strategy to minimize crosstalk. This strategy involves sequencing the stimulation waveforms between the different channels such that only one is active at any given time. Furthermore, we have chosen to implement an asymmetric (but charge-balanced biphasic) waveform profile, to match natural neurophysiological response, thus reducing fatigue of neural tissue. Although in general, CIS stimulation strategy utilizes symmetrical stimulation pulses, with same duration of positive and negative pulses, we have chosen to utilize an asymmetrical stimulation pulses with 1:4 ratio. This implementation is limited in that fewer channels can be utilized for interleaved stimulation, however, in the case of the vestibular prosthesis, the maximum number of required channels is limited to just 5, i.e. at the nerve endings of the three semicircular canals and two otolith organs.

It should be mentioned that although extensive multipurpose stimulators [13]–[21] have been developed, we have elected to implement a simpler variant as the vestibular implant requires to incorporate additional hardware (including MEMS and electronics) in as small as possible space. For the purposes of this application, the telemetry link is not operated continually to stream the stimulation data onto the device (self-motion information is generated on chip) but rather in a one-off cycle simply to programme the stimulation channel characteristics.

The chosen charge-delivery methodology is current-mode, as this is the least effected by stimulation target impedance variation. Additionally, the system includes a short-duration current steering phase, to avoid charge-buildup, and therefore glitching at turn-on and turn-off, while reducing power consumption compared to traditional current-steering systems [22]. A study [23] recently reported that using current steering techniques can additionally be considered for increased spectral resolution. Finally, as an added precaution, once each CIS cycle, all the stimulation electrodes are grounded, such that any residual charge that may have accumulated (due to device mismatch, electrode variation, etc.) is removed, although this is expected to be at least three orders of magnitude lower than the stimulus.

The target stimulation profile and current-steering methodology used is illustrated in Fig. 1. For one clock cycle before and after each stimulation phase, the current is steered towards a dummy load, such to achieve a smooth transition, thus minimizing charge buildup and spiking. Additionally, the current magnitude is scaled with ratio 4:1 between cathodic and anodic pulses. Conversely, the pulse lengths are scaled 1:4, respectively, to maintain charge balance. The corresponding current

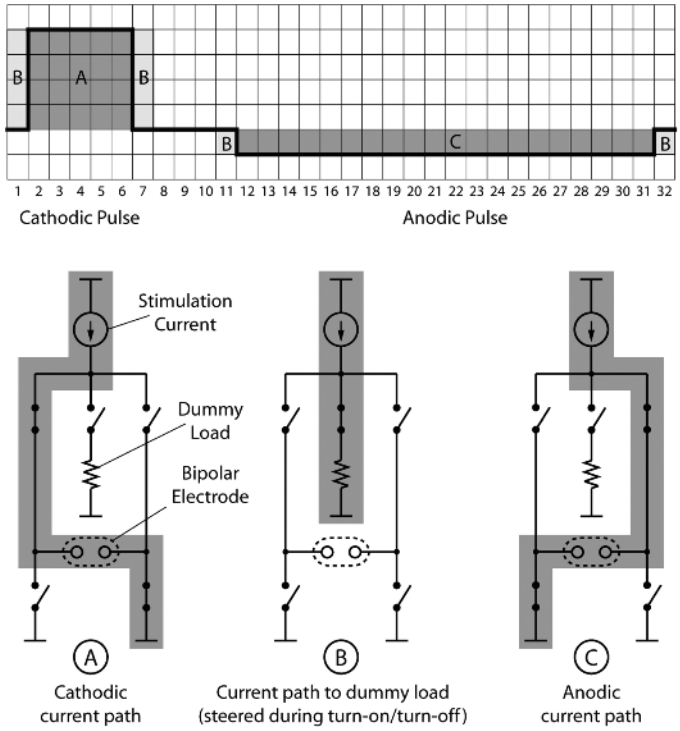

Fig. 1. Stimulation profile (top) with annotated current-path for corresponding phases.

paths flowing through the drive switches are also shown (circuit details are given later). Another feature is that there exists a short pause between cathodic and anodic pulses.

IV. Circuit Implementation

The top-level system schematic is shown in Fig. 2. This shows the 3-channel stimulation drive incorporating a CIS strategy [24], based on a modular design architecture, similar to [25]. The implementation and purpose of the various sub-blocks will be discussed in the following subsections.

A. Stimulus Conditioning Circuit

The stimulation current levels required for a patient to just about perceive a sensation (stimulation threshold) varies quite significantly from patient to patient or even from electrode site to electrode site within the same end-organ, in our case the vestibule. This greatly depends on the number of surviving neurons and the proximity of the electrodes to the nerves. Similarly, the maximum comfortable stimulation level also has a large variability. However, in all cases, the dynamic range between the minimum threshold and the maximum comfortable level is quite low, for example, in the cochlear ranging typically from 6 to 20 dB. Hence, good fitting is important if the most is to be made of the limited dynamic range of the patient. Consequently, for each stimulation channel, digital settings have been included for programmability [19], [25], [26] of: 1) offset (3-bit); 2) gain (4-bit); and 3) threshold (3-bit). These are intended to: 1) remove any static (operating point) offset caused by process variation and/or device mismatch in preceding hardware; 2) amplify the input stimulus such that the dynamic range is maximized for

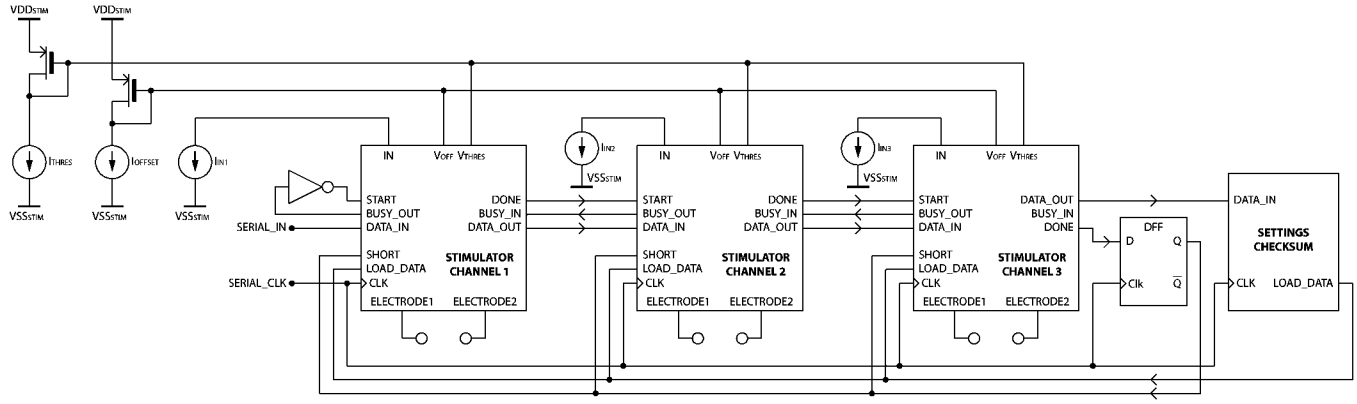

Fig. 2. Top level circuit schematic for the 3-channel electrical stimulation circuit. The modular scheme allows for additional channels to be easily incorporated within the CIS strategy.

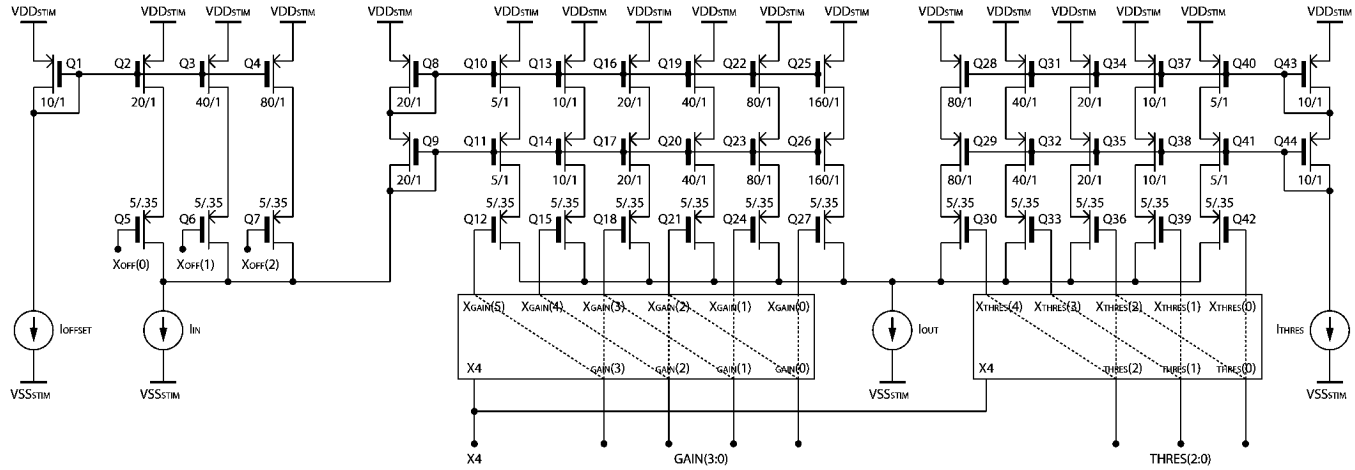

Fig. 3. Current-mode mirror network to condition the stimulation current. Programmability includes 3-bit offset compensation (for tuning out mismatch-related offset), 4-bit gain control and 3-bit stimulus threshold (for fitting patients threshold of sensation). Additionally, two input multiplexers are required to further scale $(\times 4)$ the threshold and gain during the cathodic phase to produce a correctly scaled asymmetric waveform. This is implemented for each stimulation channel. All devices shown are high-V_T (thick oxide).

a particular channel/patient; and 3) provide the baseline stimulation to match the onset of sensation of the patient. The fitting circuits consist of digitally controlled variable-width current mirrors, as shown in Fig. 3. The current mirror network produces a stimulation current given by

$$I_{CA} = 4 \cdot I_{AN} = M_T \cdot I_T + M_G \cdot (I_{IN} - M_O \cdot I_O) \quad (1)$$

where I_{CA} and I_{AN} are the cathodic and anodic current magnitudes, I_{IN} is the input current, I_T and I_O are the threshold and offset bias currents (corresponding to 1 LSB) and M_T, M_O, and M_G are the threshold (0–7), offset (0–7), and gain (0–15) discrete (digital) multipliers. Additionally, during the cathodic phase, both the threshold and gain inputs (digital) are shifted 2-bits to the left, thus scaling the currents $(\times 4)$.

For a stimulus (biphasic pulse) period of 32 clock cycles, the charge injected (i.e. for 5 clock cycles at 4× amplitude) and removed (i.e. for 20 clock cycles at 1× amplitude) during each stimulation phase is given by

$$Q = \frac{20}{f_{Clk}} \cdot I_{AN} \quad (2)$$

where Q is the stimulus charge and f_{Clk} is the clock frequency.

Cycling this stimulus at the CIS refresh rate, gives the following net charge transfer rate:

$$Q/t = \frac{\frac{20}{f_{Clk}} \cdot I_{AN}}{\frac{32}{f_{Clk}} \cdot N_{CH} + 1 \cdot} \quad (3)$$

where N_{CH} is the number of CIS stimulation channels and the $+1$ term is to include the *SHORT* phase.

B. Patient Data Loading Circuit

In order to implement a feasible totally-implantable prosthesis, the requirement for digitally programmability is paramount. One challenge in achieving such functionality is the scheme used for data transmission and recovery. Typically, medical implants use inductive schemes whereby patient settings data is encoded onto a carrier signal that is inductively coupled through the skin, to the subcutaneously implanted device where the data can be recovered [27], [28]. Implementing robust hardware to extract patient settings data from a continuous bitstream requires: 1) a temporary settings (shift) register and method to precisely align the incoming bitstream to patient settings register; 2) a method to reliably initiate a parallel load from serial input to patient settings register; and 3) data

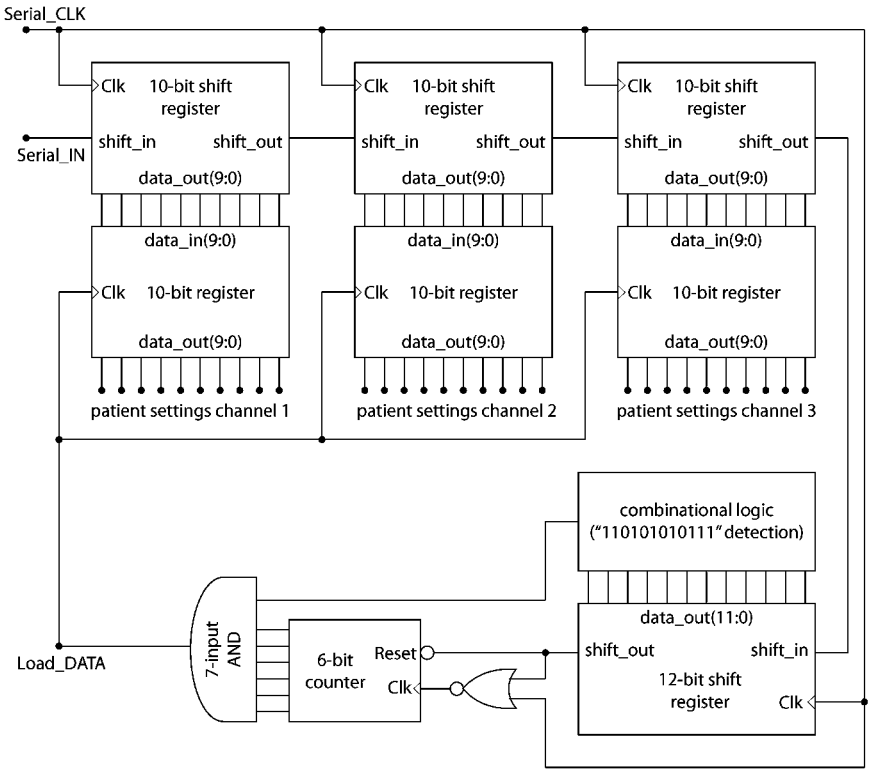

Fig. 4. State machine for loading and storing patient settings using a single bitstream (to be recovered from inductive telemetry).

redundancy and error correction. The design implemented in this system is shown in Fig. 4 (adopted from [25]). This work however, does not include hardware for data redundancy and error correction. It is envisaged that this can be implemented within the data recovery circuits using standard coding techniques, eg. hamming coding, parity check-bits, etc.

The hardware for loading the patient tuning data can be divided into two sections; the registers that are specific to each channel, and the state machine for determining when a parallel-register-load occurs. This is illustrated in Fig. 4. The input serial data stream passes through a serial shift register into the state machine to check for the start sequence. Once the start sequence is detected, this signifies the data within the serial registers are perfectly aligned with the patient settings register and a parallel register load can occur. These input and patient registers are repeated (and cascaded) for each channel, i.e. within a 3-channel system, each register would be of $3 \times [3 - \text{bit(offset)} + 4 - \text{bit(gain)} + 3 - \text{bit(threshold)}] = 30 - \text{bit length}$. The state machine, appended to the end of the *combined* shift-register interrogates the incoming bitstream to match a multi-bit *START-SEQUENCE* chosen to be: 111010101011. Finally, a ripple counter increments for every "0" received, and reset whenever a "1" is received, thus checking for the occurrence of 64 successive 0's. The *LOAD-DATA* signal is therefore asserted when both these conditions are met, i.e. the patient settings bitstream starts with 64 0's followed by the *START-SEQUENCE*. The purpose of the 64 0's is to flush the serial shift register prior to loading the patient settings, thus to ensure a partial data set cannot trigger a parallel register load.

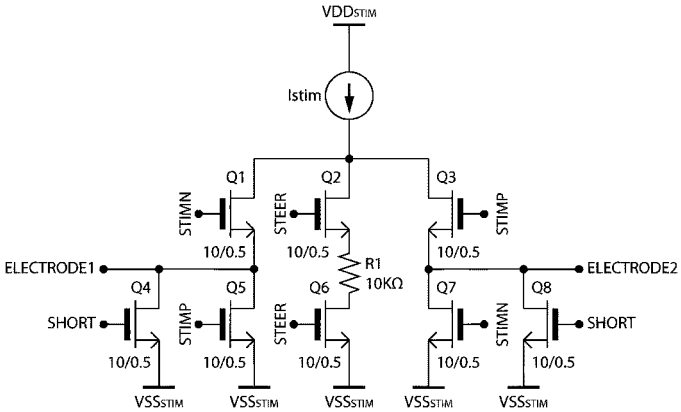

Fig. 5. Circuit schematic for H-bridge with current steering (to/from dummy load) during turn-on/turn-off transitions. Dummy load (R1) is chosen to match that of the stimulation electrodes and neural tissue ($\approx 10\ \text{k}\Omega$).

C. CIS Biphasic Waveform Generation Circuit

The CIS generator is the last of the signal conditioning blocks that directly interfaces with the electrodes, via blocking capacitors. The CIS generator converts the output of the patient dynamic range mapping circuits into non-overlapping biphasic pulses. A top-level block diagram of the CIS generator has been shown in Fig. 2. As there are three channels in the illustrated system, there are three output driver cells making up the CIS generator. Each output driver cell includes a biphasic waveform generation circuit, each of which includes a serial shift register such that the stimulation control propagates down the cascade. At the end of the chain (i.e. after the last channel)

an extra flip-flop has been added so that it can provide an extra pulse that shorts all electrodes to ground, as to remove any residual charge. This is required to make absolutely sure that no DC charge accumulates on the blocking capacitors, reducing voltage compliance. Alternatively, techniques are being developed [29]–[32] to avoid requiring blocking capacitors, for example, using charge metering [20], [30], feedback DAC calibration [31] and voltage monitoring [21], [32].

The biphasic waveform (shown previously in Fig. 1) is generated using a state machine; requiring a clock 32× higher than the CIS clock. The state machine is based on a 32-bit serial shift register, passing a single-bit token to trigger the various events, using RS-latches specifically arranged to capture the individual phases. For example, the anodic phase has been predefined to start on clock cycle 12 and end after clock cycle 31. All the bits from within this serial shift register are NOR'ed and the result is fed round the loop to the input. This technique guarantees robustness as any extra active bits in the register are flushed out after the first cycle. Beyond that the circuit can only have one active flip-flop as it will only generate a new token once there are none in the register.

These digital control signals generated above (after being level-shifted to stimulation supply voltage), feed the current control switches to form the H-bridge, shown in Fig. 5, the functioning of which has been previously illustrated in Fig. 1. In this, Q1 and Q7 drive the cathodic pulse, devices Q3 and Q5 drive the anodic pulse, devices Q2 and Q6 drive the dummy load (steering), and devices Q4 and Q8 are used to ground the stimulation electrodes, during the short/reset phase.

D. Integrated Circuit

The prototype chip was fabricated in AMS 0.35 μm 2P4M CMOS technology with a die size of 1.5 mm×0.9 mm. A microphotograph and floorplan of the complete chip is shown in Fig. 6.

The padring has been organized into two sections, a 3.3-V digital section for telemetry inputs (5 bondpads at top) and a 10-V analog section (using thick oxide devices) for the current-mode inputs and stimulation outputs (15 bondpads along sides and bottom). Although the power saved in having a lower voltage logic supply is negligible (together with the added complication of level shifting), this was chosen such that when the battery supply is low, all the other supplies are cut off to prevent complete discharge. Furthermore, in the event that the registry power is completely cut off, on power up the system resets the registry's contents to ensure that the system comes up in a safe state, i.e., all outputs are set to zero.

V. Measured Results

The circuit was biased using off-chip current sources (Keithley models 2602 and 6221) on a custom PCB test platform. Bias currents are set to $I_{\mathrm{LSB-THRESHOLD}} = 15\ \mu$A and $I_{\mathrm{LSB-OFFSET}} = 150$ nA, allowing for an input current range of 0–10 μA to provide the output within the desired range.

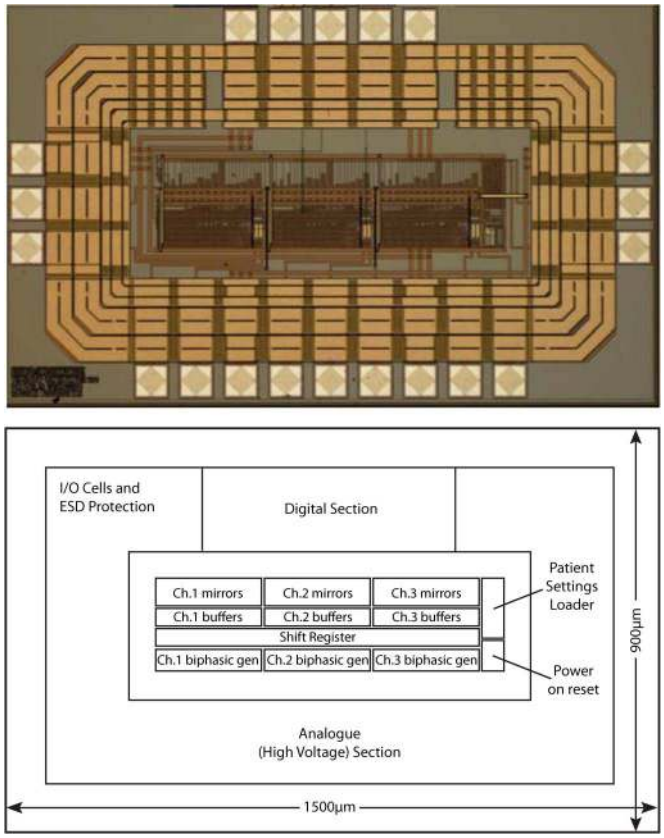

Fig. 6. Chip microphotograph and floorplan for the 3-channel stimulation circuit.

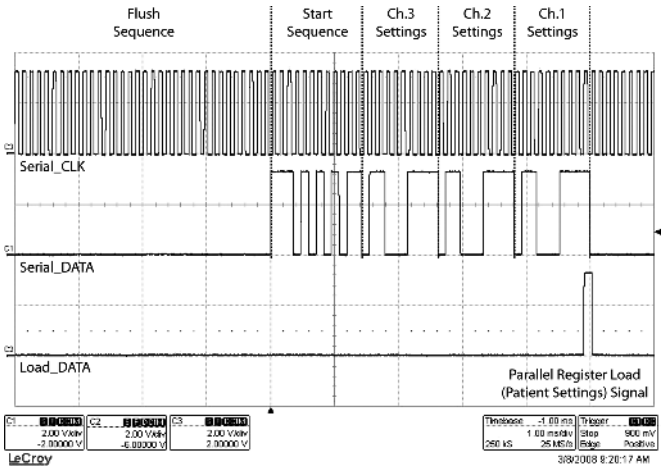

Fig. 7. Measured response of the LOAD-DATA signal on an input serial data stream. In the example, the patient settings data on all channels have been selected to have maximum gain and threshold and zero offset correction.

A. Loading Patient Settings

The patient settings, i.e. serial bitstream and clock is generated (in the format previously described in Section IV-B) using an off-the-shelf microcontroller. This confirms the correct operation of the state machine, illustrated in Fig. 7, where it can be seen that the circuit issues a LOAD-DATA signal after complete transmission of the settings data.

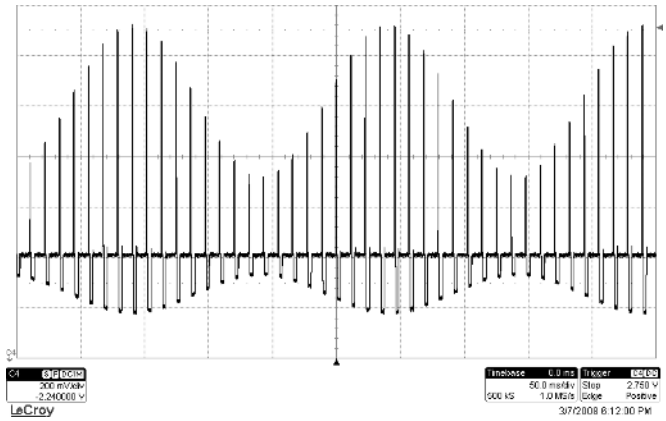

Fig. 10. Measured stimulation profile of a channel with a 5-Hz sinusoidal input stimulus.

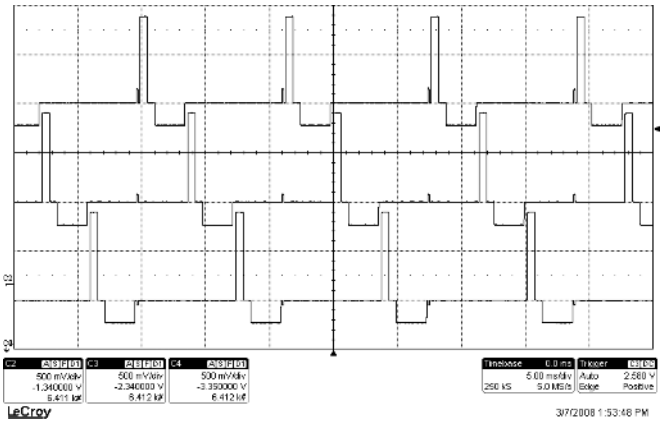

Fig. 8. Measured stimulation output of the three channels illustrating the CIS sequencing and biphasic (asymmetric, charge-balanced) waveform profile.

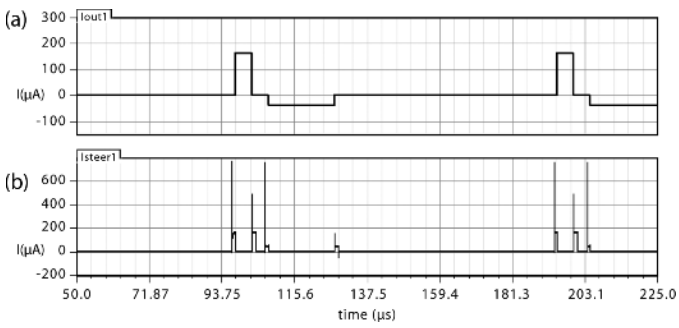

Fig. 9. Transient simulation results illustrating the current-steering technique. Shown are: (a) stimulation current delivered to electrode and (b) current steered through the dummy load.

B. Stimulation Output

Measurements are taken of the circuit's output current delivered to a 10 kΩ load through a 100 nF blocking capacitor. This effectively resembles a high-pass response with $f_{3\,\mathrm{dB}} = 159$ Hz. The measured stimulation outputs (at maximum threshold with zero input) are shown in Fig. 8. The three biphasic waveforms are sequenced to the intended CIS strategy and the *SHORT* pulse (leading each CIS cycle) illustrates the removal of any residual charge. Furthermore, the clean turn-on/turn-off transitions show that the chosen (partial) current-steering approach is operating as intended.

The internal operation of the current steering to overcome the turn-on and turn-off glitches can be illustrated through the simulation results, shown in Fig. 9. This clearly shows how the glitches are dissipated within the on-chip dummy loads.

The measured stimulation waveform for a sinusoidal (5 Hz) input current of 10 μA (ptp) is shown in Fig. 10. This illustrated the effect of the threshold signal to offset the input stimulation signal.

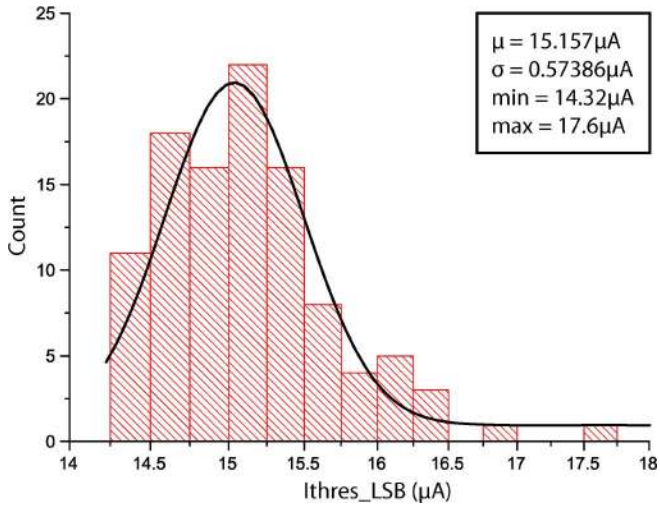

Fig. 11. Measured variation in threshold linearity for $I_{thres} = 15\ \mu$A normalized to 1 LSB.

TABLE I
TARGET DESIGN SPECIFICATIONS

CMOS Technology	AMS 0.35μm 2P4M CMOS
Supply Voltage	3.3V (logic), 10V (stimulation)
Die Area	1.5mm×0.9mm (including I/O pads)
Device Count	6946
Number of Channels	3
Stimulation Strategy	Continuous Interleave Sampling
Stimulation Pulse Type	Biphasic Pulse Amplitude Modulated
Threshold Resolution	3-bit (Max. 105μA)
Gain Resolution	4-bit (Max. 630μA)
Stimulation Current	0 to 735μA
Pulse Width	25 to 100μs/phase∗
Static Current Consumption	19.847μA†

∗By tuning system clock, †Excluding stimulation drive

C. Process Variation

At design time, statistical Monte Carlo simulations had been performed to ensure monotonicity in the patient settings, i.e., so that any inaccuracies in current magnitudes due to technology/process/mismatch variations remain below 1/2 LSB. For this, the current mirror device sizes have been selected such that a 1/2 LSB current variation corresponds to $> 3\sigma$. The measured nonlinearity in threshold stimulus (i.e., variation in 1 LSB) is in agreement with the intended design specifications, shown in Fig. 11. The measured current variation, normalized to 1 LSB

TABLE II
COMPARISON WITH OTHER WORK

Reference	[15]	[16]	[18]	[20]	This work
Year	1999	1999	2005	2007	2008
Technology	Mietec 2μm	NTE 1.2μm	TSMC 0.35μm	0.18μm	AMS 0.35μm
Supply	12V	1999	3.3V	3.3V	3.3/10V
Die Area	3×4mm	16mm^2	1.98×2.17mm	3.2×2.8mm	1.5×0.9mm
Channels	4	4	2	4×4 (per unit)	3
Output Range	2mA	0.7-6.3mA range[1]	1.75mA	18-140μA range[1]	0-735μA range[2]
Signal Resolution	8-bit	6-bit	5-bit	5-bit	current input, 48dB[3]
Time Resolution	255μs	10-2550μs	0.1-2ms	variable (per channel)	25-100μs
Stimulus Type	bipolar	bipolar	bipolar	bi- or monopolar	bipolar
Stimulus Waveform	asymm. biphasic	arbitrary	symm. mono/bi-phasic	symm. biphasic	asymm. biphasic
Stimulus Mismatch	25nC (5%)	-	-	2%	0.5%
Charge Balancing	4.7nF block. cap.	-	-	I/V monitoring[4]	100nF block. cap.

[1] 2-bit per ch. range selection, [2] 10-bit per ch. dynamic range (DR) mapping, [3] minimum DR, [4] 8-bit stimulation I/V monitoring/compensation

ranged from 14.32 to 17.6 μA, tested on all 3 channels over 10 dies.

D. Power Consumption

The power consumption is largely dominated by the stimulation supply and thus largely dependant on patient settings. The total static current consumption has been measured to be 19.847 μA (for $I_{\text{thres}} = 15\,\mu$A and $I_{\text{offset}} = 150$ nA). This consists of a 4.667-μA portion consumed by the logic supply and 15.15 μA by the analog supply (in biasing the current mirrors).

E. System Specifications

These are given in Table I.

VI. CONCLUSION

In this paper, we have presented the an integrated circuit for artificial electrical stimulation of neural tissue within the inner ear for stimulation of the vestibular organ.

This system includes three (modular) stimulation channels, each with full digital programmability, sequenced using the CIS stimulation strategy and can be easily expanded to include more channels. We have focused on achieving good reliability and robustness, specifically to ensure long-term stability, be minimally invasive and guaranteeing that patient calibration settings are uploaded in a safe manner. To this goal, we have implemented a novel current-steering scheme to avoid charge-buildup-related stimulation artifacts. This has designed to ensure all stimulation transitions are smooth but sharp while maintaining good power efficiency, compared to traditional current-steer systems. Moreover, the system has been designed to generate an asymmetric, charge-balanced waveform to maximize neural response to electrical stimulus whilst minimizing fatigue of neural tissue. A comparison of this work with other neural stimulator chips is listed in Table II.

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