A Passive Design Scheme to Increase Rectified Power of Piezoelectric Energy Harvesters

***Abstract*—Piezoelectric vibration energy harvesting is becoming a promising solution to power wireless sensors and portable electronics. While miniaturizing energy harvesting systems, rectified power efficiencies from miniaturized piezoelectric transducers (PT) are usually decreased due to insufficient voltage levels generated by the PTs. In this paper, a monolithic PT is split into several regions connected in series. The raw electrical output power is kept constant for different connection configurations as theoretically predicted. However, the rectified power following a full-bridge rectifier (FBR), or a synchronized switch harvesting on inductor (SSHI) rectifier, is significantly increased due to the higher voltage/current ratio of series connections. This is an entirely passive design scheme without introducing any additional quiescent power consumption and it is compatible with most of state-of-the-art interface circuits. Detailed theoretical derivations are provided to support the theory and the results are experimentally evaluated using a custom MEMS PT and a CMOS rectification circuit. The results show that, while a PT is split into 8 regions connected in series, the performance while using a FBR and a SSHI circuit is increased by 2.3× and 5.8×, respectively, providing an entirely passive approach to improving energy conversion efficiency.**

***Index Terms*—Energy harvesting, piezoelectric transducers, full-bridge rectifier, synchronized switch harvesting on inductor (SSHI).**

I. Introduction

In the past decade, piezoelectric vibration energy harvesting has shown its promising ability to power wireless sensor nodes by transducing environmental kinetic vibration energy into electricity [1]–[4]. Fig. 1 shows a widely used cantilevered piezoelectric transducer (PT) [5]–[7]. The device consists of a piezoelectric material sandwiched by two electrode layers standing on a substrate; a proof mass is usually added at the free end to adjust the resonance frequency and increase output power [8]–[11]. The raw output power of a typical PT varies between 100's nW and 100's μW depending on the scale, structure and piezoelectric material. Although this power is able to power some low-power electronic devices, it cannot be directly used as it is a very unstable AC energy source. The actual usable power significantly depends on the conversion efficiency of rectification circuits employed [12], [13].

The most widely used rectifier for a PT is a full-bridge rectifier (FBR), which employs four passive diodes connected between the PT and an energy storage capacitor [5]. The circuit diagram and associated waveforms are shown in Fig. 2. While the PT is vibrating, it can be modeled as a current source I_P in parallel with a capacitor C_P. The inherent capacitor C_P is formed by the top and bottom electrode layers of the PT. An energy storage capacitor C_S is connected at the output to store the rectified DC power. The waveform shows that, in order to

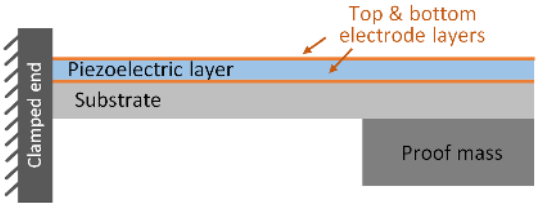


Fig. 1: A cantilevered piezoelectric harvester.

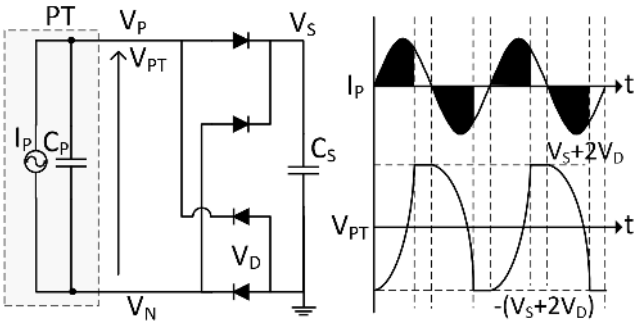


Fig. 2: Full-bridge rectifier and associated waveforms.

overcome the voltage threshold set by the FBR and transfer energy into C_S, the voltage across the PT (V_{PT}) needs to attain either $V_S + 2V_D$ or $-(V_S + 2V_D)$, where V_S is the voltage across C_S and V_D is the forward voltage drop of the diodes. After each half period of vibration, the polarization of V_{PT} alters; hence, some generated energy is wasted to flip V_{PT} from $V_S + 2V_D$ to $-(V_S + 2V_D)$, or vice-versa. The wasted part is illustrated in the figure with black areas. After V_{PT} is flipped and it attains one of the two thresholds, the remaining energy generated in this half period can be transferred into C_S. In order to overcome the threshold, the open-circuit voltage amplitude generated by the PT, noted as V_{OC}, needs to be higher than $V_S + 2V_D$ so that the power conversion efficiency of the FBR is not zero. This condition can be expressed as:

$$V_{OC} > V_S + 2V_D \tag{1}$$

This is the condition for a FBR starts to start operating. If (1) is not satisfied, all generated energy by the PT is wasted in continually flipping V_{PT} and the power efficiency in this case is zero. Even if it is marginally satisfied, the efficiency can be extremely low as most of energy is wasted. The open-circuit amplitude, V_{OC}, is proportional to the applied excitation level if the PT is vibrating in the linear range. When the PT is implemented in a place with weak excitation, V_{OC} can be too low to satisfy the condition in (1). Especially, when a MEMS PT is employed, V_{OC} can be as low as a few 100's mV under low and noisy excitation levels. In this case, the

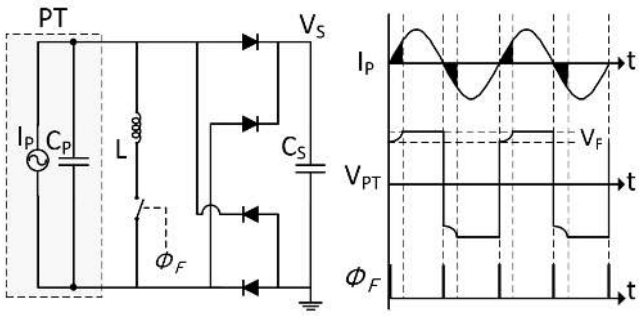


Fig. 3: SSHI rectifier and associated waveforms.

power extraction efficiency of a FBR is zero when the voltage V_S goes to the level of V_{OC}.

Recently, many active rectifiers have been proposed to increase the power rectification performance [14]–[28]. The synchronized switch harvesting on inductor (SSHI) rectifier is one of the most efficient interface circuits designed to synchronously flip the voltage V_{PT} to reduce the energy loss due to voltage flipping [29]–[34]. Fig. 3 shows the circuit diagram and associated waveforms of a SSHI rectifier. A SSHI circuit employs an inductor to form a RLC oscillation loop to flip the voltage V_{PT} at each zero-crossing moment of I_P. While a zero-crossing moment of I_P is detected, a pulse ϕ_F is generated to close the RLC loop for a certain time duration. The voltage V_{PT} is then flipped from $\pm(V_S + 2V_D)$ to $\mp(V_S + 2V_D)$ with a loss of V_F, as illustrated in the figure. As the closed RLC loop helps flip V_{PT}, wasted energy (shown by black areas) is decreased; hence, energy conversion efficiency is significantly increased compared to a passive FBR [35]. However, active interface circuits introduce issues on complexity, stability, cold-startup and extra cost compared to passive FBRs. Hence, a topology to achieve comparable power efficiency of reported active rectifiers is needed while employing a passive FBR instead of a active rectifier.

In this paper, a new topology is proposed to passively improve the power extraction performance of FBRs to achieve comparable performance compared to state-of-the-art active rectification circuits (such as SSHI), without employing any additional component or circuit. Furthermore, if this topology is co-integrated with a SSHI circuit, the performance of the SSHI circuit can be further improved. The scheme is presented in the next section and theoretical modeling of the topology is given in Section III. A MEMS harvester is used for experimental validation in Section IV and a conclusion is provided in the last section.

II. Proposed Topology

In this section, the concept underlying the proposed topology is presented. For piezoelectric transducers used in energy harvesting systems, the top and bottom electrode layers are usually designed to be monolithic, as shown in Fig. 1. In this paper, the electrode layers are split into several, say n, equal regions, as illustrated in Fig. 4. As the resulting n electrode regions stay on a common substrate with a common proof mass, while the PT is vibrating, the voltage signals generated

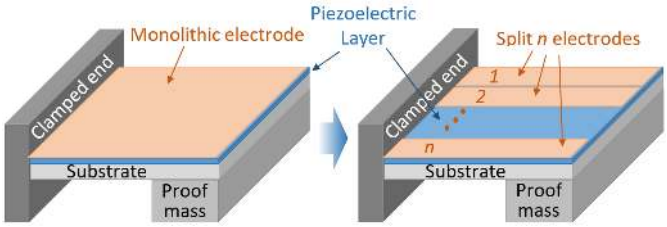


Fig. 4: Splitting a monolithic electrode layer into n regions.

in the n regions are with the same amplitude, frequency and phase. Therefore, the n regions can be electrically connected in series and the resulting open-circuit voltage is increased by n. Higher open-circuit voltage generated from the PT make it easier to overcome the thresholds set by following rectification circuits; hence, the rectified power is significantly increased. Some previous works on electrode segmentation have been reported recently; however, they were focused on splitting the electrode orthogonality along the strain line to analyze strain distribution and power in different regions [36]–[38]. The following section will focus on modeling a PT with n split electrode regions. The theoretical modeling shows that the rectified power while the electrode is split into 8 regions is increased by 2.5× and 11× for a FBR and a SSHI circuit, respectively. It is worth mentioning that this series configuration is a purely passive design method, which does not employing any additional active or passive components or circuits, to increase the rectified power. Hence, this new approach can be employed together with state-of-the-art interface circuits.

III. Modeling

A. Raw electrical power

The raw output power from a PT is analyzed in this section. The raw output power means the power consumed in a resistive load connected with the PT with the impedance matching. Fig. 5 shows the equivalent circuit diagram of a monolithic PT, a parallel-connected n-region PT and a series-connected n-region PT, from top to bottom respectively. Assuming the gaps between adjacent electrode regions are negligible and the effect of these gaps to vibration amplitude and frequency is also negligible, a monolithic PT can be regarded as a parallel-connected n-region PT.

As a first step, the monolithic model is analyzed. While the PT is excited, I_P and C_P are the current source and the internal capacitance for the monolithic model. The current source can be expressed as $I_P = I_0 \sin(\omega t)$, where $\omega = 2\pi f_P$ and f_P is the excitation frequency. Hence, the total charge generated by the PT in a half period (T/2) can be calculated, which is expressed as:

$$Q_{total} = \int_0^{\frac{T}{2}} I_0 \sin \omega t \mathrm{d}t = \frac{2I_0}{\omega} \tag{2}$$

Assuming the PT is operated as an open circuit, all generated charge Q_{total} flows into C_P. Therefore, the open-circuit zero-to-peak voltage amplitude is calculated as:

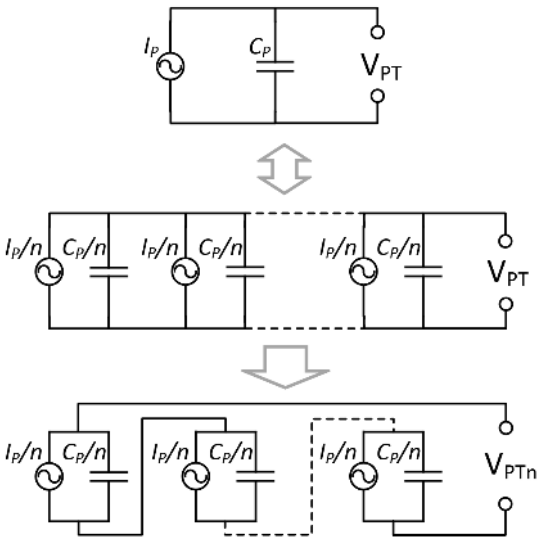


Fig. 5: Equivalent circuit of a monolithic PT and n-region series-connected PT.

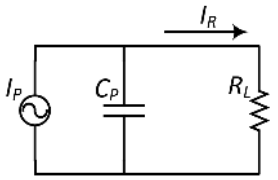


Fig. 6: Load resistor connected to a monolithic PT.

$$V_{OC} = \frac{1}{2}\frac{Q_{total}}{C_P} = \frac{I_0}{\omega C_P} \tag{3}$$

In order to measure the raw output power generated from a PT, a variable load resistor, R_L, is connected to the PT, as shown in Fig. 6. The resistance R_L is varied to match the internal impedance of the PT in order to find the peak output power consumed in the R_L. While a resistor R_L is connected to a monolithic PT, the current amplitude in R_L can be expressed as:

$$I_R(j\omega) = I_0 \frac{Z_C}{Z_C + R_L} = \frac{I_0}{1 + j\omega R_L C_P} \tag{4}$$

Hence, the output power consumed in the resistor R_L can be calculated as:

$$\begin{aligned} P_R &= |\frac{1}{2} I_R^2 R_L| = \frac{I_0^2}{2} |\frac{R_L}{(1 + j\omega R_L C_P)^2}| \\ &= \cdots = \frac{I_0^2}{2} \frac{1}{\frac{1}{R_L} + \omega^2 C_P^2 R_L} \end{aligned} \tag{5}$$

The output power P_R attains its peak while $R_L = \frac{1}{\omega C_P}$. Hence, the raw output power of a monolithic model is:

$$P_{R(max)} = \frac{I_0^2}{4\omega C_P} \tag{6}$$

After the electrode layer is split into n equal regions, the area of one region is $1/n$ of the monolithic area. Therefore,

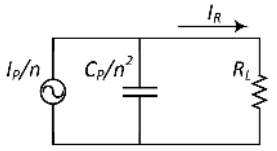


Fig. 7: Load resistor connected to a PT with n-region electrode in series.

the current source and inherent capacitance for each individual region can be expressed as I_P/n and C_P/n, respectively. While the n regions are electrically connected in series, the equivalent current source and inherent capacitance for the resulting PT are I_P/n and C_P/n^2, respectively. Hence, the open-circuit voltage amplitude becomes:

$$V_{OC-n} = \frac{1}{2}\frac{Q_{total}/n}{C_P/n^2} = \frac{n}{2}\frac{Q_{total}}{C_P} = nV_{OC} \tag{7}$$

The subscript n represents the n-region series-connected model. It can be seen that the open-circuit voltage is increased by n times compared to the monolithic model. However, the current is decreased by n times to I_P/n. If a variable resistor R_L is connected to this series model, as shown in Fig. 7, similar derivations can be performed for this series model. The current amplitude in R_L can be expressed as:

$$I_{R-n}(j\omega) = \frac{I_0}{n}\frac{Z_C}{Z_C + R_L} = \frac{I_0 n}{n^2 + j\omega R_L C_P} \tag{8}$$

Hence, the output power consumed in the resistor R_L for this n-region model can be calculated as:

$$\begin{aligned} P_{R-n} &= |\frac{1}{2} I_R^2 R_L| = \frac{I_0^2}{2} |\frac{n^2 R_L}{(n^2 + j\omega R_L C_P)^2}| \\ &= \cdots = \frac{I_0^2}{2} \frac{1}{\frac{n^2}{R_L} + \frac{\omega^2 C_P^2 R_L}{n^2}} \end{aligned} \tag{9}$$

The peak output power consumed in R_L is achieved while $R_L = \frac{n^2}{\omega C_P}$ and the peak power is calculated as:

$$P_{R-n(max)} = \frac{I_0^2}{4\omega C_P} \tag{10}$$

Comparing the results obtained in (6) and (10), the output power is exactly the same and it does not depend on the number n. Hence, the series configuration does not help increase the raw output power consumed in an impedance-matched resistive load. While keeping the raw power unchanged, output voltage is increased by n by sacrificing the output current by n. A rectification circuit is needed for AC-to-DC conversion and the power efficiency of such a circuit determines the usable rectified power. The re-distribution between voltage and current of series configurations is extremely useful to increase the extracted power while using some particular rectification circuits. For example, while a full-bridge rectifier (FBR) is employed, as shown in Fig. 2, the circuit starts to extract energy while $V_{OC} > V_S + 2V_D$ is satisfied. In order to achieve the maximum power point (MPP) of a FBR, V_{OC} should be at around $2(V_S + 2V_D)$. Assuming V_S is

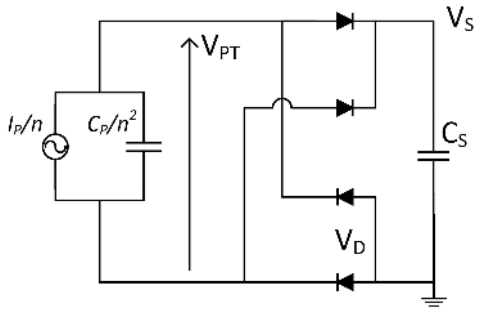


Fig. 8: Full-bridge rectifier with a n-series PT.

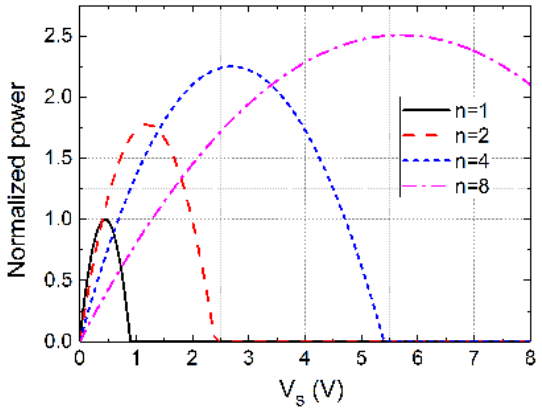


Fig. 9: Normalized theoretical output power using a FBR with different series stages.

around 3 V and $V_D = 0.3$ V, the MPP is achieved while $V_{OC} = 7.2$ V, which is equivalent to a peak-to-peak voltage of 14.4 V. This high open-circuit voltage can possibly be attained for macroscopic PTs under high excitation levels. However, for MEMS (microelectromechanical systems) harvesters, it is extremely hard to attain since the peak-to-peak voltage from a MEMS harvester usually varies between 100's mV and a few V. Therefore, series configuration can be useful to improve power efficiency of rectification circuits and the derivations will be performed in the following parts.

B. Full-bridge rectifier

Assuming the electrode is split into n regions, the corresponding current source and inherent capacitance are I_P/n and C_P/n^2, as previous explained. The number n can be any positive integer. While $n = 1$, the analyzed model is a monolithic model without splitting the electrode. The equivalent circuit diagram when a full-bridge rectifier (FBR) is employed is shown in Fig. 8. In a half period of I_P, the total generated charge can be expressed as:

$$Q_{tot(n)} = \int_0^{\frac{T}{2}} \frac{I_0}{n} \sin \omega t \mathrm{d}t = \frac{2I_0}{n\omega} \tag{11}$$

As previously explained and shown in the waveforms in Fig. 2, a certain amount of charge is wasted in flipping the voltage V_{PT} between $\pm(V_S+2V_D)$ and $\mp(V_S+2V_D)$. Hence, assuming the condition in (1) is satisfied, the remaining charge that can be transferred into C_S after flipping V_{PT} is calculated as:

$$Q_{FBR(n)} = Q_{tot(n)} - 2(V_S + 2V_D)\frac{C_P}{n^2} \tag{12}$$

As the open-circuit voltage amplitude, V_{OC}, generated in one individual region is given in (7), the above equation be rewritten as:

$$Q_{FBR(n)} = 2C_P(\frac{V_{OC}}{n} - \frac{V_S + 2V_D}{n^2}) \tag{13}$$

Assuming the voltage increase in C_S is very small compared to V_S, the energy transferred into C_S in this half period is:

$$E_{FBR(n)} = V_S Q_{FBR(n)} = 2C_P V_S(\frac{V_{OC}}{n} - \frac{V_S + 2V_D}{n^2}) \tag{14}$$

Hence, the average rectified power in this half period is:

$$P_{FBR(n)} = \frac{E_{FBR(n)}}{T/2} = 4f_P C_P V_S(\frac{V_{OC}}{n} - \frac{V_S + 2V_D}{n^2}) \tag{15}$$

Setting the derivative of the above equation to 0, it can be found that $P_{FBR(n)}$ achieves its maximum power while V_S equals to an optimal voltage expressed as:

$$V_{S,opt} = \frac{n}{2}V_{OC} - V_D \tag{16}$$

Then the maximum output power of a FBR can be expressed as:

$$P_{FBR(n),max} = 4f_P C_P(\frac{V_{OC}}{2} - \frac{V_D}{n})^2 \tag{17}$$

The power shown in (17) is the maximum power obtained using a FBR with the proposed split-electrode method. It can be seen that the proposed method increases the output power by decreasing the effect introduced by the forward voltage drop of diodes. Although discrete diodes have lower V_D values, they occupy large board area to be implemented. While system miniaturization becomes one of the key design considerations for wireless sensor networks, diodes are widely integrated on-chip with other rectification and power management circuits to minimize the system size. However, on-chip Schottky diodes usually have higher forward voltage drop compared to discrete diodes. Hence, the proposed method is extremely useful while on-chip diodes are employed since V_D for on-chip Schottky diodes is usually around 0.3 V.

Assuming the open-circuit voltage $V_{OC} = 1.5$ V and the voltage drop of the diodes is $V_D = 0.3$ V, the normalized power expressed in (15) can be plotted in a range of V_S. The results are shown in Fig. 9. The diode voltage drop, $V_D = 0.3$ V, is experimentally measured using the FBR in the following experiment section to keep the consistency between simulations and measurements. While $n = 1$ where the electrode is not split (or split electrodes connected in parallel), the peak power in this case is normalized to 1. While the electrode is split into 8 regions connected in series ($n = 8$), the rectified power is increased by 2.5× compared

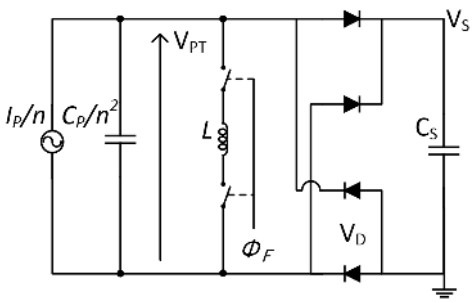


Fig. 10: SSHI rectifier with a n-series PT.

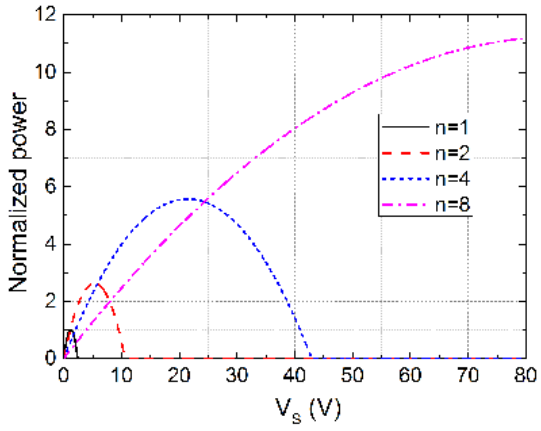


Fig. 11: Normalized theoretical output power using a SSHI with different series stages.

to the monolithic model. In addition, the MPP is attained at a higher V_S value to accommodate loads requiring higher supply voltages.

C. SSHI rectifier

After studying the performance of a FBR, this section analyzes the rectified power for different series configurations while a SSHI interface circuit is employed. Similar to the previous section, the electrode of the PT is assumed to be split into n equal regions connected in series. Hence, the resulting current source and inherent capacitance are I_P/n and C_P/n^2, respectively. Fig. 10 shows a SSHI interface circuit connected with this n-region PT. The SSHI circuit employs a RLC loop to flip V_{PT} in a half pseudo-period with a loss V_F. Hence, before the flipping, $V_{PT} = \pm(V_S + 2V_D)$; after the flipping, $V_{PT} = \mp(V_S + 2V_D) \pm V_F$. The loss in a half pseudo-period can be expressed as:

$$V_F = (V_S + 2V_D)(1 - e^{-\frac{\pi}{\sqrt{\frac{4Ln^2}{R^2C_P} - 1}}}) = (V_S + 2V_D)\eta_F \quad (18)$$

where R is the total resistance in the RLC loop, which consists of the DC resistance of the inductor, the ON resistance of switches and other parasitic resistance in wires and contacts. Detailed derivations of this voltage loss ratio can be found in [30]. The factor η_F is the voltage loss ratio expressed as (19):

$$\eta_F = 1 - e^{-\frac{\pi}{\sqrt{\frac{4Ln^2}{R^2C_P} - 1}}} \quad (19)$$

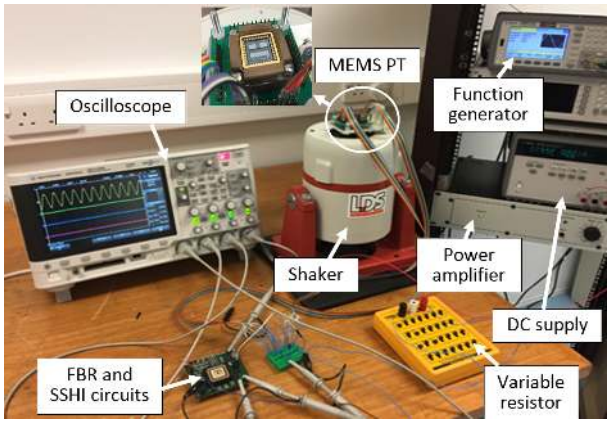


Fig. 12: Experimental setup.

The total charge generated in the current source in a half period has been calculated in (11). After a certain amount of charge is wasted to compensate the flipping loss V_F, the remaining charge that can be transferred into C_S is expressed as:

$$Q_{SSHI(n)} = Q_{tot(n)} - V_F\frac{C_P}{n^2} = C_P(\frac{2V_{OC}}{n} - \frac{V_F}{n^2}) \quad (20)$$

Assuming the voltage increase in C_S is small, energy transferred into C_S is:

$$E_{SSHI(n)} = V_S Q_{SSHI(n)} = C_P V_S(\frac{2V_{OC}}{n} - \frac{V_F}{n^2}) \quad (21)$$

Hence, the average rectified power by a SSHI circuit is:

$$P_{SSHI(n)} = \frac{E_{SSHI(n)}}{T/2} = 2f_P C_P V_S(\frac{2V_{OC}}{n} - \frac{V_F}{n^2}) \quad (22)$$

Setting the derivative of the above equation to 0, it can be found that $P_{SSHI(n)}$ achieves its maximum power while V_S equals to an optimal voltage expressed as:

$$V_{S,opt} = \frac{n}{\eta_F}V_{OC} - V_D \quad (23)$$

Then the maximum output power of a SSHI rectifier can be expressed as:

$$P_{SSHI(n),max} = 2\eta_F f_P C_P(\frac{V_{OC}}{\eta_F} - \frac{V_D}{n})^2 \quad (24)$$

Assuming the open-circuit voltage $V_{OC} = 1.5\,\text{V}$, the voltage drop of the diodes is $V_D = 0.3\,\text{V}$ and the flipping loss $\eta_F = 0.5$ for $n = 1$, the normalized power expressed in (22) can be plotted in a range of V_S. Fig. 11 shows the normalized output power while the peak value for $n = 1$ is normalized to 1. It can be seen that the output power is significantly increased while the electrode is split into more regions connected in series. For $n = 8$, the power is increased by $11\times$ compared to the monolithic electrode model and the MPP is attained at $V_S = 80\,\text{V}$.

Comparing the results shown in Fig. 9 and Fig. 11, series configurations show higher performance improvement in the

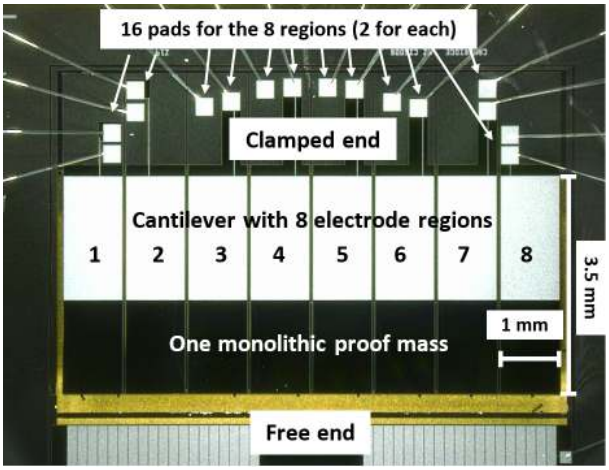


Fig. 13: Optical micrograph of MEMS piezoelectric harvester with 8 regions.

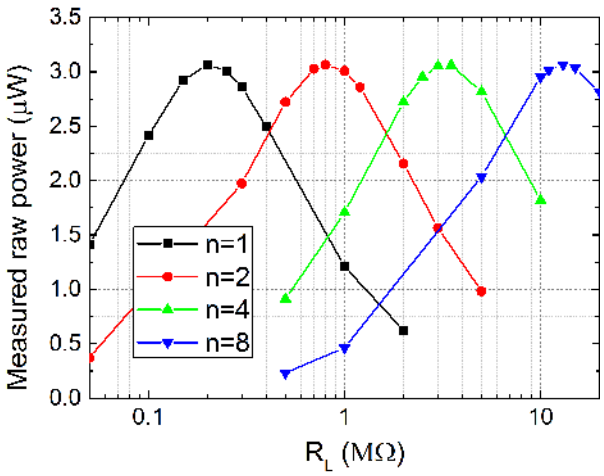


Fig. 14: Measured raw electrical power consumed in a resistive load for different series configurations.

SSHI circuit compared to the FBR. This is because the voltage flipping loss, expressed as (19), is significantly decreased while n goes larger. In the assumptions of Fig. 11, η_F is assumed to be 0.5 for $n = 1$. While n goes to 2, 4 and 8, the value η_F is decreased to 0.267, 0.138 and 0.07, respectively. Hence, more efficient voltage flipping helps further increase the performance of series models. In the next section, experiments are performed to evaluate the performance improvement using series configurations with a MEMS piezoelectric harvester and CMOS rectification circuits.

D. Power efficiency analysis

The power conversion efficiency of a rectifier is given by the ratio between the output power and the input power of the rectifier, which can be expressed as $\eta_{RECT} = P_O/P_{IN}$. In order to analyze the power efficiencies with the proposed method for full-bridge (FB) and SSHI rectifiers, P_O and P_{IN} need to analyzed.

For FB and SSHI rectifiers, while the electrode of the PT is split into n regions connected in series, the optimal V_S values are expressed in (16) and (23), which are $\frac{n}{2}V_{OC} - VD$ and $\frac{n}{\eta_F}V_{OC} - V_D$ for FB and SSHI rectifiers, respectively. Hence, the input voltage values of the two rectifiers are $\frac{n}{2}V_{OC}$ and $\frac{n}{\eta_F}V_{OC}$ respectively, which are n times higher than the case of $n = 1$ for both FBR and SSHI. Since the current generated by the n-region PT and flowing into rectifiers is decreased by n times, the input power, P_{IN} for both FB and SSHI rectifiers does not change for different n values. However, according to (17) and (24), it can be seen that the output power of FBR and SSHI rectifiers is increased at higher n values. Since the power efficiency is expressed as $\eta_{RECT} = P_O/P_{IN}$, the power efficiencies of the proposed scheme ($n > 1$) for both FB and SSHI rectifiers are increased compared to conventional PTs with monolithic electrodes ($n = 1$) since P_O is increased while P_{IN} keeps constant.

IV. Experiments

The proposed connection topology was experimentally validated and the experimental setup is shown in Fig. 12. During

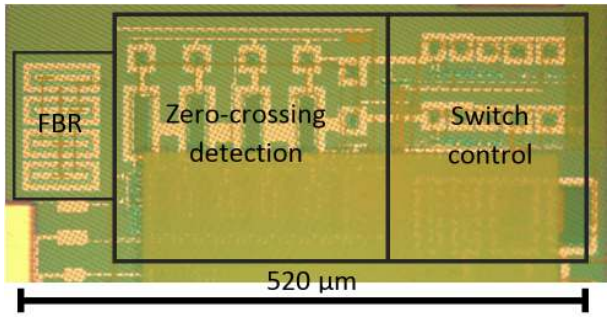


Fig. 15: Optical micrograph of FBR and SSHI circuits in CMOS process.

the measurements, a custom MEMS cantilevered piezoelectric transducer (PT) was fabricated and placed on a shaker (LDS V406 M4-CE), which was excited at the natural frequency of the MEMS PT at 220 Hz. The shaker is driven by an excitation signal from a function generator (Agilent 33250A 80 MHz) and amplified by a power amplifier (LDS PA100E). A DC power supply (Agilent E3647A) was employed to provide a 1.5 V supply to the SSHI circuit.

A microphoto of the MEMS PT is shown in Fig. 13. The size of the cantilever is $8\,\mathrm{mm} \times 3.5\,\mathrm{mm}$. The electrodes of this cantilever is split into 8 regions, as shown in the figure; hence, the width of one electrode is around $1\,\mathrm{mm}$. A common proof mass is located at the free end to ensure that the voltage signals generated by the 8 regions are approximately at the same amplitude, frequency and phase. The size of the monolithic proof mass is $8\,\mathrm{mm} \times 1.5\,\mathrm{mm}$. For each region, there are 2 pads for top and bottom electrodes; hence, 16 pads in total for 8 regions. As there are 8 regions for this particular PT, the number n can be equal to 1, 2, 4 or 8 in this implementation. This design is suitable for MEMS mass-production as the electrode is split during the layout design stage and no additional manual operation is required.

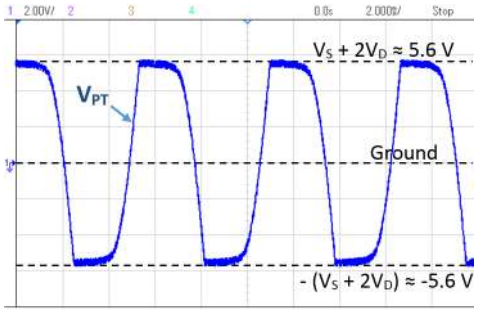


Fig. 16: Measured waveform of a FBR ($V_S = 5\,\mathrm{V}$, $V_{OC} = 1.5\,\mathrm{V}$, $n = 4$).

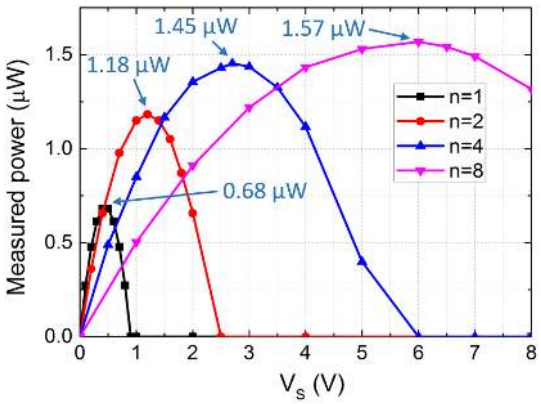


Fig. 17: Measured output power using a FBR ($V_{OC} = 1.5\,\mathrm{V}$, $V_D = 0.3\,\mathrm{V}$).

A. Raw electrical power

In order to measure the raw output power, the PT is connected with a variable resistor. The excitation acceleration level is turned to 1 g and the open-circuit zero-to-peak voltage amplitude generated from the PT is around $V_{OC} = 1.5\,\mathrm{V}$. This V_{OC} is the voltage while the 8 regions are connected in parallel; hence, equivalent to a large monolithic electrode without being split. The inherent capacitance, C_P, with 8 regions connected in parallel is measured to be $3.52\,\mathrm{nF}$. The measurements were performed for different series configurations for n = 1, 2, 4 and 8. When all the 8 regions are electrically connected in parallel or in series, this corresponds to the cases for $n = 1$ and $n = 8$, respectively. The $n = 2$ connection is formed by connecting left four regions in parallel and right four regions in parallel and then connecting these two parts in series. Similarly, electrodes can be connected together for the case $n = 4$. The measured output power for different connection configurations is shown in Fig. 14. It can be seen that the peak power for different n values are almost at the same level; however, they are attained for different load resistance values. Fig. 14 shows that the four MPPs are achieved while R_L is at around $0.2\,\mathrm{M\Omega}$, $0.8\,\mathrm{M\Omega}$, $3\,\mathrm{M\Omega}$ and $12\,\mathrm{M\Omega}$, respectively. These results closely match the calculations in Section III-A, where the matched load resistor is found to be n^2 times higher for the n-series PT. These results prove that different connection configurations do not change the raw AC output power; they only change the internal impedance of the PT (or voltage/current ratio from the PT), which results into different load resistor values to match the internal impedance. While this section proves the unchanged AC output power, the next two sections show the performance enhancement of rectified DC power.

B. Full-bridge rectifier

The MEMS PT is tested with an on-chip full-bridge rectifier (FBR) in this section. Fig. 15 shows the chip micrograph of the FBR and the SSHI circuit, which will be used in the next experiment. The circuit is implemented in a $0.18\,\mu\mathrm{m}$ high-voltage (HV) CMOS process. The active area of the FBR is less than $0.02\,\mathrm{mm}^2$, which consists of four on-chip Schottky-barrier diodes. The measured forward voltage drop of the diodes is around $0.3\,\mathrm{V}$.

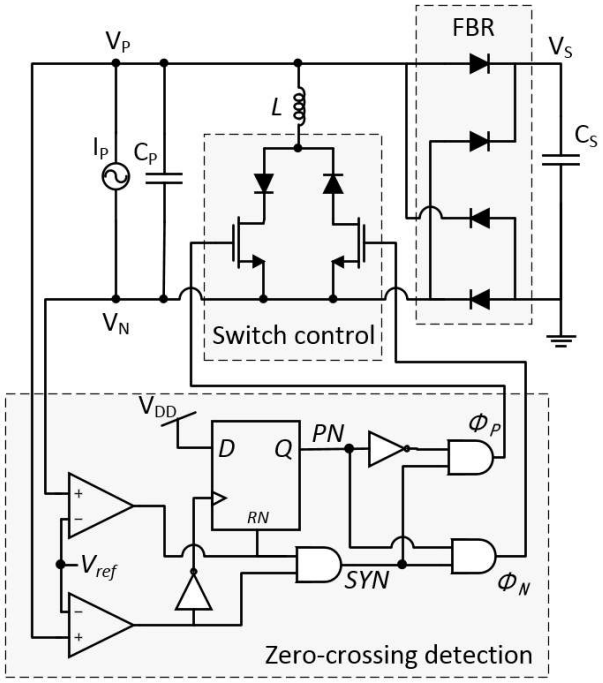
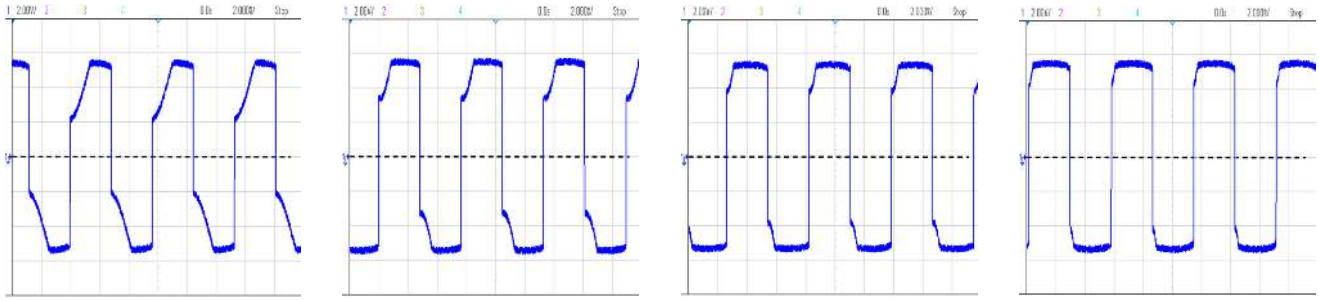


Fig. 18: Circuit implementation of the SSHI circuit.

In the experiments with a FBR, the excitation acceleration is set at 1 g ($V_{OC} = 1.5$). The measured waveform of the voltage across the PT, V_{PT}, is shown in Fig. 16. It can be seen that V_{PT} needs to attain either $V_S + 2V_D$ or $-(V_S + 2V_D)$ to transfer energy into the storage capacitor C_S. The voltage V_S is set to $2\,\mathrm{V}$ and the $n = 4$ configuration is used in order to show an operating FBR. If $n = 1$ is used for this high V_S, the measured waveform for V_{PT} will be a simple sine wave around the ground since it cannot overcome the threshold set by the FBR. Hence, smaller n configurations only work for lower V_S and the proposed series configurations are able to work for higher V_S values.

Fig. 17 shows the measured output power extracted by a FBR using different series configurations. The measurement on a particular V_S value is performed by charging C_S from its current V_S to a value slightly higher. The power is calculated with the energy increased in C_S divided by the time elapsed



(a) $n = 1$ (b) $n = 2$ (c) $n = 4$ (d) $n = 8$

Fig. 19: Measured transient waveforms of V_{PT} for different series configurations ($V_S = 5\,\mathrm{V}$, $V_D = 0.3\,\mathrm{V}$).

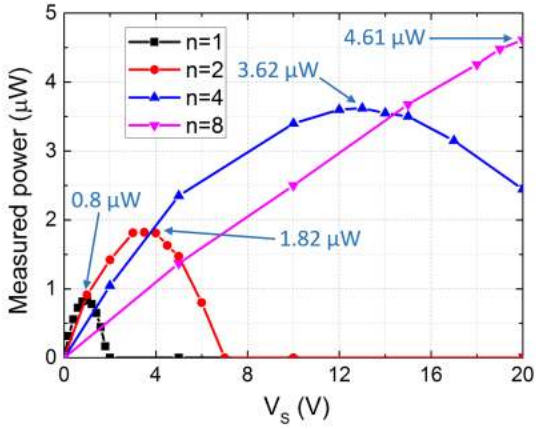


Fig. 20: Measured output power using SSHI circuit ($V_{OC} = 1.5\,\mathrm{V}$, $V_D = 0.3\,\mathrm{V}$).

for charging. According to these results, the n = 2, 4 and 8 configurations increase the output by 1.7×, 2.1× and 2.3×, respectively, compared to $n = 1$. In additional, the MPPs for n = 2, 4 and 8 configurations are achieved at higher V_S values. These results closely match the theoretical calculations and show the evident performance improvement of the proposed topology.

Although the raw AC output power is not changed for different connection configurations in section IV-A, the high voltage/current ratio generated from the PT with a larger number of n, in this section, is experimentally proved to increase the performance while using a FBR. This DC power improvement is obtained without employing any additional circuit or component; hence, with no extra cost or complexity of the system. Besides improving the performance of FBRs, the next section shows the experimental results to prove the performance enhancement with a SSHI rectifier.

C. Bias-flip rectifier

This section presents the measured results of the MEMS PT using a SSHI circuit implemented in a CMOS process. The optical micrograph of the circuit is shown in Fig. 15 and the circuit implementation is presented in Fig. 18. The SSHI circuit used here is a conventional simplified bias-flip rectifier [30], [32], [33]. Since the aim of this paper is not on the SSHI circuit itself, but to present the series configuration topology and show how it improves output power, design details of the circuit are not presented. The SSHI circuit is only designed to be operational without additional features, such as self-powering, cold-startup, MPP tracking, etc. This simplified SSHI circuit consists of a FBR, a zero-crossing detection block and a switch control block. The inductor is implemented off-chip with the value of $1\,\mathrm{mH}$. The active chip area of the SSHI circuit including the FBR is around $0.1\,\mathrm{mm}^2$. The zero-crossing detection block aims to detect the zero-crossing moment of I_P and this is the moment to start flipping V_{PT}. When I_P is close to zero, the diodes of the FBR are just about to turn OFF. At this instance, one of V_P and V_N is at $-V_D$ and it begins to increase. Hence, two continuous-time comparators are employed to compared V_P and V_N with a reference voltage V_{ref}, which is set slightly higher than $-V_D$ to find the moment when V_P or V_N begins to increase from $-V_D$. The output of the two comparators are ANDed and a synchronous signal, SYN, is generated for each zero-crossing moment of I_P. The signal PN indicates the polarization of V_{PT} before it is flipped. The two outputs of this block are ϕ_P and ϕ_N, which drives the switches in the switch control block. These two signals selectively copy SYN according to PN. The switch control block read ϕ_P and ϕ_N to close the RLC loop to flip V_{PT}. As the SSHI circuit is only designed to experimentally validate the performance improvement of the proposed series topology; hence, the transistor-level circuit implementations are not presented in detail in this paper. Some good examples on implementing highly-efficient SSHI circuits have been presented in [29], [30], [32], [33].

Fig. 19 shows the measured waveforms of V_{PT} for different series configurations. As mentioned in Section III-C, the voltage flip loss ratio is expressed as $\eta_F = 1 - e^{-\frac{\pi}{\sqrt{\frac{4Ln^2}{R^2C_P}-1}}}$; hence, a higher value of n (more electrode regions connected in series) significantly decreases η_F. This can be well observed from Fig. 19. While $n = 1$, the flip loss is around 50% and this value is decreased to near 20% for $n = 8$. The improved voltage flipping can further increase the performance of the proposed series configurations.

Fig. 20 shows the measured output power extracted using the SSHI circuit for different series configurations. The figure shows that for $n = 1$, the maximum power is around $0.8\,\mu\mathrm{W}$. The maximum power is increased to $1.82\,\mu\mathrm{W}$, $3.62\,\mu\mathrm{W}$ and $4.61\,\mu\mathrm{W}$ for n = 2, 4 and 8, respectively. Therefore, the

TABLE I: Performance comparison with state-of-the-art

Reference	Technique	Piezoelectric transducer	Piezoelectric capacitance	Frequency	Inductor	Performance enhancement
[29]	Bias-flip (SSHI)	Mide V22B	18 nF	225 Hz	820 μH	4
[20]	PSCE	Mide V22B	19.5 nF	173 Hz	10 mH	2.1
[28]	SSHI	Custom MEMS	8.5 nF	155 Hz	470 μH	2.5
[14]	SECE	Q220-A4304YB	52 nF	60 Hz	560 μH	3
[25]	SSHI	Mide V21B	26 nF	134 Hz	3.3 mH	4.4
This work	Passive FBR	Custom MEMS with split-electrode	3.52 nF	220 Hz	None	1.7 - 2.3
	SSHI				1 mH	2.3 - 5.8

performance compared to $n = 1$ is improved by 2.3×, 4.5× and 5.8× respectively. It can also be seen that the MPP is not attained for $n = 8$ because the thick-oxide MOSFETs used in the CMOS process can tolerate up to 20 V drain-source voltage. Hence, the power can only be measured for V_S up to 20 V. However, the theoretical results, shown in Fig. 11, imply that if V_S can be higher, the extracted power could be further increased.

Table I shows the performance comparisons with state-of-the-art interface circuits for piezoelectric energy harvesting. The results for this work are split into two parts: with a passive FBR and with a SSHI circuit. The performance enhancement figures (the last column) for this work vary in a range according to the split electrode number n. For example, the figures 1.7 for FBR and 2.3 for SSHI are measured while $n = 1$; the figures 2.3 for FBR and 5.8 for SSHI are measured while $n = 8$. The results show that while the electrode is split into 8 regions connected in series ($n = 8$), the performance enhancement while using a passive FBR achieves 2.3×, which is comparable to the reported active interface circuits. Compared to reported interface circuits, the proposed scheme does not employ any active rectification circuit, which significantly reduces the system complexity, volume and cost. When the proposed scheme is co-integrated with an active SSHI rectifier, the system shows higher performance enhancement (5.8× while $n = 8$) compared to state-of-the-art active rectification circuits.

V. Conclusion

In this paper, a series configuration topology is proposed, where the monolithic electrode layer of a piezoelectric energy harvester is split into several equal regions connected in series. The theoretical modeling shows that series configurations do not increase the raw output power, which is consumed in an impedance-matched resistive load, from a piezoelectric transducer (PT). However, it reconfigures the distribution between the voltage and current generated from the PT to make the generated energy easily overcome thresholds set by following rectification circuits; hence the rectified power is significantly increased.

A MEMS PT with 8 electrode regions is fabricated to evaluate the theory. With equal 8 regions, the series stage number n can be set to 1, 2, 4 or 8, respectively. In order to measure the rectified power by a FBR and a SSHI circuit, a $0.1\,\mathrm{mm}^2$ CMOS circuit is designed and integrated with the MEMS PT for measurements. The measured results show that, for $n = 8$, the rectified power is increased by 2.3× for a FBR and 5.8× for a SSHI circuit, compared to the monolithic electrode model ($n = 1$). Compared to state-of-the-art interface circuits designed for piezoelectric energy harvesting, the topology proposed in this paper is a purely passive method to increase overall performance. Since no additional component or circuit is employed, this method can be employed together with most passive (FBR) or active (SSHI) rectification circuits to further increase the performance without introducing more power consumption or instabilities into the system. In the experiments, the value of n is chosen as 1, 2, 4 and 8 because the PT designed for this work consists of 8 electrode regions. Once a PT is designed, fabricated and implemented, it is difficult to change the electrode configuration. However, the number n can be any positive integer, which should be defined during the PT design stage with considerations of the environmental vibration conditions. Theoretically, output power can be increased with a large number n; however, a larger n number results in higher V_S voltage to attain the maximum power point. Hence, the preferred operating V_S voltage should also be considered while choosing a suitable n number.

References

[1] S. P. Beeby, M. J. Tudor, and N. M. White, "Energy harvesting vibration sources for microsystems applications," *Measurement Science and Technology*, vol. 17, no. 12, p. R175, 2006.

[2] R. L. Harne and K. W. Wang, "A review of the recent research on vibration energy harvesting via bistable systems," *Smart Materials and Structures*, vol. 22, no. 2, p. 023001, 2013.

[3] D.-S. Kwon, H.-J. Ko, M.-O. Kim, Y. Oh, J. Sim, K. Lee, K.-H. Cho, and J. Kim, "Piezoelectric energy harvester converting strain energy into kinetic energy for extremely low frequency operation," *Applied Physics Letters*, vol. 104, no. 11, p. 113904, 2014.

[4] A. Harb, "Energy harvesting: State-of-the-art," *Renewable Energy*, vol. 36, no. 10, pp. 2641–2654, 2011.

[5] G. D. Szarka, B. H. Stark, and S. G. Burrow, "Review of power conditioning for kinetic energy harvesting systems," *IEEE Trans. Power Electron.*, vol. 27, DOI 10.1109/TPEL.2011.2161675, no. 2, pp. 803–815, 2012.

[6] P. D. Mitcheson, E. M. Yeatman, G. K. Rao, A. S. Holmes, and T. C. Green, "Energy harvesting from human and machine motion for wireless electronic devices," *Proc. IEEE*, vol. 96, DOI 10.1109/JPROC.2008.927494, no. 9, pp. 1457–1486, 2008.

[7] M. Belleville, H. Fanet, P. Fiorini, P. Nicole, M. J. M. Pelgrom, C. Piguet, R. Hahn, C. Van Hoof, R. Vullers, M. Tartagni, and E. Cantatore, "Energy autonomous sensor systems: Towards a ubiquitous sensor technology," *Microelectronics Journal*, vol. 41, DOI http://dx.doi.org/10.1016/j.mejo.2010.01.009, no. 11, pp. 740–745, 2010.

[8] G. Tang, B. Yang, J.-q. Liu, B. Xu, H.-y. Zhu, and C.-s. Yang, "Development of high performance piezoelectric d33 mode mems vibration energy harvester based on pmn-pt single crystal thick film," *Sensors and Actuators A: Physical*, vol. 205, no. 0, pp. 150–155, 2014.

[9] N. Elvin and A. Erturk, *Advances in energy harvesting methods*. Springer Science & Business Media, 2013.

[10] M. Han, Q. Yuan, X. Sun, and H. Zhang, "Design and fabrication of integrated magnetic mems energy harvester for low frequency applications," *J. Microelectromech. Syst.*, vol. 23, DOI 10.1109/JMEMS.2013.2267773, no. 1, pp. 204–212, 2014.

[11] N. Rezaei-Hosseinabadi, A. Tabesh, and R. Dehghani, "A topology and design optimization method for wideband piezoelectric wind energy harvesters," *IEEE Transactions on Industrial Electronics*, vol. 63, DOI 10.1109/TIE.2015.2499248, no. 4, pp. 2165–2173, 2016.

[12] C. M. A. Lopes and C. A. Gallo, "A review of piezoelectrical energy harvesting and applications," in *2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE)*, DOI 10.1109/ISIE.2014.6864799, pp. 1284–1288, Jun. 2014.

[13] A. Khaligh, Z. Peng, and Z. Cong, "Kinetic energy harvesting using piezoelectric and electromagnetic technologies 2014;state of the art," *IEEE Trans. Ind. Electron.*, vol. 57, DOI 10.1109/TIE.2009.2024652, no. 3, pp. 850–860, 2010.

[14] M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A nanopower synchronous charge extractor ic for low-voltage piezoelectric energy harvesting with residual charge inversion," *IEEE Transactions on Power Electronics*, vol. 31, DOI 10.1109/TPEL.2015.2417352, no. 2, pp. 1263–1274, 2016.

[15] S. Du and A. A. Seshia, "An inductorless bias-flip rectifier for piezoelectric energy harvesting," *IEEE Journal of Solid-State Circuits*, vol. 52, DOI 10.1109/JSSC.2017.2725959, no. 10, pp. 2746–2757, 2017.

[16] A. Romani, M. Filippi, and M. Tartagni, "Micropower design of a fully autonomous energy harvesting circuit for arrays of piezoelectric transducers," *IEEE Trans. Power Electron.*, vol. 29, DOI 10.1109/TPEL.2013.2257856, no. 2, pp. 729–739, 2014.

[17] M. Shim, J. Kim, J. Jung, and C. Kim, "Self-powered 30uw-to-10mw piezoelectric energy-harvesting system with 9.09ms/v maximum power point tracking time," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, DOI 10.1109/ISSCC.2014.6757490, Conference Proceedings, pp. 406–407.

[18] H. Shen, H. Ji, J. Qiu, Y. Bian, and D. Liu, "Adaptive synchronized switch harvesting: A new piezoelectric energy harvesting scheme for wideband vibrations," *Sensors and Actuators A: Physical*, vol. 226, DOI http://dx.doi.org/10.1016/j.sna.2015.02.008, pp. 21–36, 2015.

[19] L. M. Miller, A. D. T. Elliott, P. D. Mitcheson, E. Halvorsen, I. Paprotny, and P. K. Wright, "Maximum performance of piezoelectric energy harvesters when coupled to interface circuits," *IEEE Sensors Journal*, vol. 16, DOI 10.1109/JSEN.2016.2546684, no. 12, pp. 4803–4815, 2016.

[20] T. Hehn, F. Hagedorn, D. Maurath, D. Marinkovic, I. Kuehne, A. Frey, and Y. Manoli, "A fully autonomous integrated interface circuit for piezoelectric harvesters," *IEEE Journal of Solid-State Circuits*, vol. 47, DOI 10.1109/JSSC.2012.2200530, no. 9, pp. 2185–2198, 2012.

[21] G. Shi, Y. Xia, Y. Ye, L. Qian, and Q. Li, "An efficient self-powered synchronous electric charge extraction interface circuit for piezoelectric energy harvesting systems," *Journal of Intelligent Material Systems and Structures*, p. 1045389X15624796, 2016.

[22] J. Sankman and M. Dongsheng, "A 12-uw to 1.1-mw aim piezoelectric energy harvester for time-varying vibrations with 450-na iq," *IEEE Trans. Power Electron.*, vol. 30, DOI 10.1109/TPEL.2014.2313738, no. 2, pp. 632–643, 2015.

[23] S. Du, Y. Jia, and A. A. Seshia, "An efficient inductorless dynamically configured interface circuit for piezoelectric vibration energy harvesting," *IEEE Transactions on Power Electronics*, vol. 32, DOI 10.1109/TPEL.2016.2587757, no. 5, pp. 3595–3609, 2017.

[24] D. Kwon and G. A. Rincon-Mora, "A single-inductor 0.35 um cmos energy-investing piezoelectric harvester," *IEEE Journal of Solid-State Circuits*, vol. 49, DOI 10.1109/JSSC.2014.2342721, no. 10, pp. 2277–2291, 2014.

[25] D. A. Sanchez, J. Leicht, F. Hagedorn, E. Jodka, E. Fazel, and Y. Manoli, "A parallel-sshi rectifier for piezoelectric energy harvesting of periodic and shock excitations," *IEEE Journal of Solid-State Circuits*, vol. 51, DOI 10.1109/JSSC.2016.2615008, no. 12, pp. 2867–2879, 2016.

[26] D. A. Sanchez, J. Leicht, E. Jodka, E. Fazel, and Y. Manoli, "A 4uw-to-1mw parallel-sshi rectifier for piezoelectric energy harvesting of periodic and shock excitations with inductor sharing, cold start-up and up to 681extraction improvement," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, DOI 10.1109/ISSCC.2016.7418059, Conference Proceedings, pp. 366–367.

[27] X.-D. Do, H.-H. Nguyen, S.-K. Han, D. S. Ha, and S.-G. Lee, "A self-powered high-efficiency rectifier with automatic resetting of transducer capacitance in piezoelectric energy harvesting systems," *IEEE Trans. VLSI Syst.*, vol. 23, DOI 10.1109/TVLSI.2014.2312532, no. 3, pp. 444–453, 2015.

[28] E. E. Aktakka and K. Najafi, "A micro inertial energy harvesting platform with self-supplied power management circuit for autonomous wireless sensor nodes," *IEEE Journal of Solid-State Circuits*, vol. 49, DOI 10.1109/JSSC.2014.2331953, no. 9, pp. 2017–2029, 2014.

[29] Y. K. Ramadass and A. P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE Journal of Solid-State Circuits*, vol. 45, DOI 10.1109/JSSC.2009.2034442, no. 1, pp. 189–204, 2010.

[30] S. Du, Y. Jia, C. D. Do, and A. A. Seshia, "An efficient sshi interface with increased input range for piezoelectric energy harvesting under variable conditions," *IEEE Journal of Solid-State Circuits*, vol. 51, DOI 10.1109/JSSC.2016.2594943, no. 11, pp. 2729–2742, 2016.

[31] L. Wu, X. D. Do, S. G. Lee, and D. S. Ha, "A self-powered and optimal sshi circuit integrated with an active rectifier for piezoelectric energy harvesting," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, DOI 10.1109/TCSI.2016.2608999, no. 3, pp. 537–549, 2017.

[32] L. Shaohua and F. Boussaid, "A highly efficient p-sshi rectifier for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 30, DOI 10.1109/TPEL.2015.2422717, no. 10, pp. 5364–5369, 2015.

[33] J. Liang and W.-H. Liao, "Improved design and analysis of self-powered synchronized switch interface circuit for piezoelectric energy harvesting systems," *IEEE Trans. Ind. Electron.*, vol. 59, DOI 10.1109/TIE.2011.2167116, no. 4, pp. 1950–1960, 2012.

[34] P. Gasnier, J. Willemin, S. Boisseau, G. Despesse, C. Condemine, G. Gouvernet, and J. J. Chaillout, "An autonomous piezoelectric energy harvesting ic based on a synchronous multi-shot technique," *IEEE Journal of Solid-State Circuits*, vol. 49, DOI 10.1109/JSSC.2014.2325555, no. 7, pp. 1561–1570, 2014.

[35] A. Badel, D. Guyomar, E. Lefeuvre, and C. Richard, "Efficiency enhancement of a piezoelectric energy harvesting device in pulsed operation by synchronous charge inversion," *Journal of Intelligent Material Systems and Structures*, vol. 16, no. 10, pp. 889–901, 2005.

[36] S. Du, Y. Jia, S.-T. Chen, C. Zhao, B. Sun, E. Arroyo, and A. A. Seshia, "A new electrode design method in piezoelectric vibration energy harvesters to maximize output power," *Sensors and Actuators A: Physical*, vol. 263, DOI http://dx.doi.org/10.1016/j.sna.2017.06.026, pp. 693–701, 2017.

[37] P. Kodali, A. Krishna, R. Varun, M. Prasad, and S. Sambandan, "Segmented electrodes for piezoelectric energy harvesters," *IEEE Electron Device Letters*, vol. 35, DOI 10.1109/LED.2014.2305447, no. 4, pp. 485–487, 2014.

[38] R. Kashyap, T. R. Lenka, and S. Baishya, "A model for doubly clamped piezoelectric energy harvesters with segmented electrodes," *IEEE Electron Device Letters*, vol. 36, DOI 10.1109/LED.2015.2496186, no. 12, pp. 1369–1372, 2015.