A Passive Soft-Switching Snubber for PWM Inverters

Fang Z. Peng, *Senior Member, IEEE*, Gui-Jia Su, *Senior Member, IEEE*, and Leon M. Tolbert, *Senior Member, IEEE*

***Abstract*—This paper presents a regenerative passive snubber circuit for pulse-width modulation (PWM) inverters to achieve soft-switching purposes without significant cost and reliability penalties. This passive soft-switching snubber (PSSS) employs a diode/capacitor snubber circuit for each switching device in an inverter to provide low dv/dt and low switching losses to the device. The PSSS further uses a transformer-based energy regenerative circuit to recover the energy captured in the snubber capacitors. All components in the PSSS circuit are passive, thus leading to reliable and low-cost advantages over those soft-switching schemes relying on additional active switches. The snubber has been incorporated into a 150 kVA PWM inverter. Simulation and experimental results are given to demonstrate the validity and features of the snubber circuit.**

***Index Terms*—EMI, PSSS, PWM, soft switching inverters.**

I. Introduction

TO REDUCE switching stresses, losses, and electromagnetic interference (EMI), soft-switching techniques have been developed for power converters since the 1970s [1]. There are many topologies of soft-switching inverters [1]–[10], such as resonant dc link, resonant snubber, and zero-current transition inverters [8]. Soft-switching inverters can be grouped into two main categories: resonant dc link and resonant snubber. The resonant dc link provides zero dc-link voltage or current intervals to all phase legs during switching instants, whereas the resonant snubber diverts current from and/or provides zero-voltage intervals to each main device at switching instants. The active clamped resonant dc link converter [1] and the auxiliary quasiresonant dc link converter [2], [10] are examples of resonant dc link inverters. Auxiliary resonant snubber inverters such as the auxiliary resonant commutated pole (ARCP), zero-voltage transition, and resonant snubber inverters [9] belong to the second resonant snubber category.

However, all existing soft-switching inverters use additional active devices to achieve soft-switching, thus increasing costs and control complexity and decreasing reliability. Prior to the soft-switching technology, the RCD snubber circuit that consists of a resistor (R), capacitor (C), and diode (D), as shown in Fig. 1, had been widely used in PWM inverters to reduce switching stresses and EMI. The traditional RCD snubber is lossy and bulky, and it is difficult to apply to high-frequency switching PWM inverters because the losses in the snubber increase proportionally with the switching frequency.

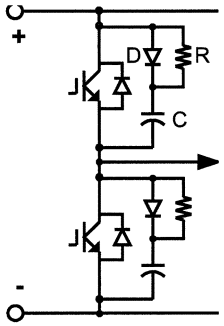


Fig. 1. Inverter phase leg with RCD snubbers.

This paper presents a regenerative passive snubber circuit for PWM inverters that is able to achieve the aforementioned soft-switching objectives without significantly increasing the cost. This passive soft-switching snubber (PSSS) employs a snubber circuit consisting of diodes and capacitors for each phase leg to provide low dv/dt and low switching losses to the switching devices. The PSSS further uses a transformer-based energy regenerative circuit to recover the energy captured in the snubber capacitors. All components in the PSSS circuit are passive, making it reliable and low in cost. The snubber has been applied to a 150 kVA PWM inverter. Simulation and experimental results are given to demonstrate the validity and features of the snubber circuit.

II. PSSS Circuit and Operating Principle

Fig. 2(a) shows the proposed PSSS circuit, which consists of a diode/capacitor soft-switching snubber (SSS) circuit for each phase leg, and an energy recovery circuit shared among all the phase legs, as illustrated in Fig. 2(b) for a three-phase inverter application. The SSS circuit includes a snubber diode, $\mathrm{D_{Sp}}$, and a snubber capacitor, $\mathrm{C_{Sp}}$, for the upper main device, $\mathrm{S_p}$, and, symmetrically, $\mathrm{D_{Sn}}$ and $\mathrm{C_{Sn}}$ for the lower main device, $\mathrm{S_n}$. The functions of the snubber diodes, $\mathrm{D_{Sp}}$ and $\mathrm{D_{Sn}}$, and snubber capacitors, $\mathrm{C_{Sp}}$ and $\mathrm{C_{Sn}}$, are very similar to those of the traditional RCD snubber. They are, however, arranged differently so that both snubber capacitors are connected to the midpoint of the phase leg. Because the upper and lower main devices always operate complementarily to each other during normal PWM operation, the sum of both snubber capacitors' voltages should remain constant and equal to the dc link voltage, which is further

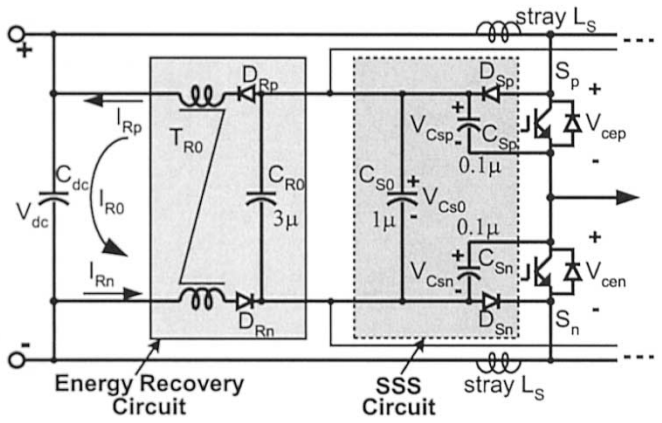
Manuscript received May 3, 2002; revised October 13, 2003. This paper was presented at the Power Electronic Specialists Conference (PESC'02), Cairns Australia, June 23–27, 2002. This work was supported by Oak Ridge National Laboratory, UT-Battelle, LLC, for the U.S. Department of Energy under Contract DE-AC05-00OR22725. Recommended by Associate Editor F. Blaabjerg.

F. Peng is with the Department of Electrical and Computer Engineering, Michigan State University, East Lansing, MI 48826-1226 USA (e-mail: fzpeng@egr.msu.edu).

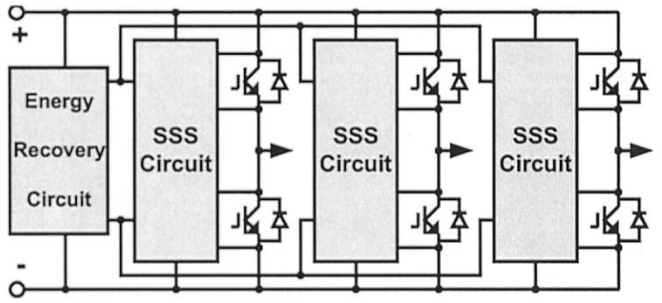
G.-J. Su is with the Power Electronics and Electric Machinery Research Center, Oak Ridge National Laboratory, Oak Ridge, TN 37831-6472 USA (e-mail: sugj@ornl.gov).

L. M. Tolbert is with the Department of Electrical and Computer Engineering, The University of Tennessee, Knoxville, TN 37996-2100 USA and is also with the Oak Ridge National Laboratory, Oak Ridge, TN 37831-6472 USA (e-mail: tolbert@utk.edu).

Digital Object Identifier 10.1109/TPEL.2003.823204



(a)



(b)

Fig. 2. PSSS circuit for an inverter phase leg. (a) Proposed PSSS circuit for an inverter phase leg. (b) Arrangement of a three-phase inverter with the PSSS circuits.

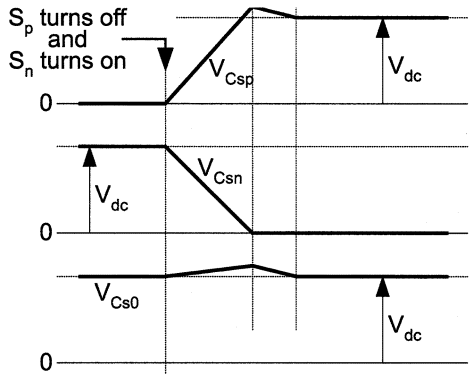


Fig. 3. Voltage waveforms at a switching instant showing the operating principle.

guaranteed by a larger snubber bus capacitor, C_{S0}, connected across the two snubber capacitors.

Fig. 3 shows the operating waveforms during S_p turn-off and S_n turn-on. Assuming the IGBT of S_p is conducting the load current, turning off S_p will divert the current into the snubber circuit, charging the snubber capacitor C_{Sp} through the snubber diode D_{Sp} and discharging C_{Sn} through C_{S0}. Therefore, V_{CSp} increases and V_{CSn} decreases as shown in Fig. 3, whereas voltage, V_{Cs0}, remains almost constant.

The energy recovery circuit that is shared by all the snubber circuits includes a capacitor, C_{R0}, two diodes, D_{Rp} and D_{Rn}, and a transformer, T_{R0}. The transformer, T_{R0}, makes I_{Rp} equal to I_{Rn} so that a recovery current, I_{R0}, flows into the dc link capacitor, C_{dc}. The two diodes, D_{Rp} and D_{Rn}, guarantee the energy recovery current (power) flows in one direction, i.e., from the snubber back to the dc link. The power (or current) rating of the energy recovery circuit for a three-phase inverter, P_R, is determined by the snubber capacitance, $C_S(= C_{Sp} = C_{Sn})$; voltage across the large snubber capacitor, V_{Cs0}, which is only slightly higher than the dc link voltage, V_{dc}; inverter switching frequency, f_{sw}; stray inductance, L_s; square of the decrease in the dc link current over each switching instance, $\Delta I^2_{dc(k)}$; and fundamental frequency, f_m, according to

$$P_R = 6C_S V^2_{Cs0} f_{sw} + f_m L_s \sum_k \left(\Delta I^2_{dc(k)}\right). \quad (1)$$

A detailed analysis of the circuit can be performed based on operation modes given in Fig. 4. To simplify the analysis, as shown in the equivalent circuit in Fig. 4(a), the energy recovery circuit is omitted; it will be discussed later. The switching process from an upper switch carrying the load current to the lower diode is first described, and the process from an upper diode conducting the load current to the lower switch is then explained. Operation modes in the reversal of the two processes can be analogously derived.

Mode 0+, Fig. 4(b): An initial mode in which switch S_p is conducting the load current, i_L. An inductive load is considered, and the load current remains constant during the switching process.

Mode 1, Fig. 4(c): S_p is turned off. The load current is diverted to the snubber capacitors, C_{Sp} and C_{Sn} through the snubber diode, D_{Sp}. The current thus charges C_{Sp} and discharges C_{Sn}.

Mode 2, Fig. 4(d): When the voltage of C_{Sp}, V_{Csp}, increases to the dc source voltage, V_{Cs0}, and the voltage of C_{Sn}, V_{Csn} decreases to zero, the diodes, D_{Sn} and D_n start conducting, clamping V_{Csn} to zero. The current flowing in the stray inductance is also decreasing.

Mode 3, Fig. 4(e): The current flowing in the stray inductance decreases to zero, and the energy stored in the stray inductance is transferred to the snubber capacitor. The diode, D_n, carries the load current. Switch S_n can be turned on under zero voltage. During this mode, as the voltage across the capacitor, C_{S0}, becomes higher than the dc source voltage, the energy recovery circuit starts to transfer energy from the capacitor back to the dc source.

Mode 4, Fig. 4(f): Switch S_n is turned on in Mode 1 before C_{Sp} is fully charged and C_{Sn} discharged. Besides the load current, an additional charging/discharging current is generated through S_n, accelerating the charging/discharging process. At the end of the process, if the current following through C_{Sp} is bigger than the load current, the operation of the circuit proceeds to Mode 5. Otherwise, it falls back to Mode 2.

Mode 5, Fig. 4(g): Because the charging current following through C_{Sp} is bigger than the load current, the surplus is carried by switch S_n. The charging current starts to decrease because V_{Csp} is slightly higher than the dc source voltage, V_{Cs0}. Once the charging current drops below the load current, the operation of the circuit proceeds to Mode 2 and eventually settles at Mode 3.

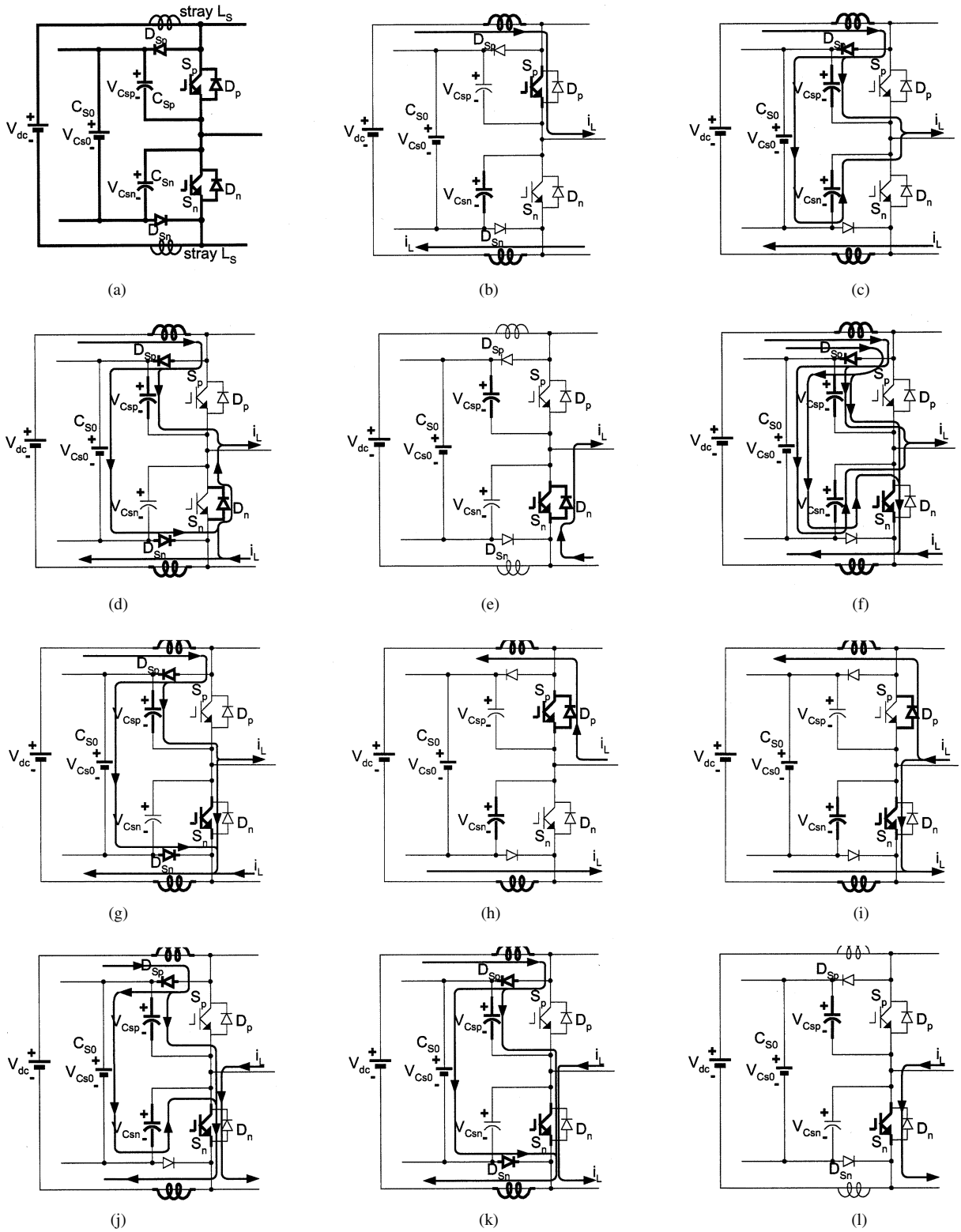


Fig. 4. Operating modes. (a) Equivalent circuit of the snubber circuit during switching. (b) Mode 0+: S_p is on and conducting load current. (c) Mode 1: S_p is turned off, charging C_{sp} and discharging C_{sn}. (d) Mode 2: D_{Sn} and D_n clamp V_{Csn} to zero voltage and carry current. (e) Mode 3: D_n carries the load current and S_n is turned on. (f) Mode 4: S_n is turned on in Mode 1 before C_{sp} is fully charged and C_{sn} fully discharged. Turning on S_n accelerates the charge (C_{sp}) and discharge (C_{sn}) process. (g) Mode 5: C_{sn} is fully discharged. S_n carries a portion of the charging current. (h) Mode 0-: S_p is on while D_p is conducting the load current. (i) Mode 6: S_n is turned on; thus a portion of the load current is diverted from D_p to S_n. (j) Mode 7: When load current is completely diverted to S_n, D_p turns off and a process of charging C_{sp} and discharging C_{sn} starts. (k) Mode 8: When C_{sn} is fully discharged, the charging current starts to decrease. (l) Mode 9: The charging current has decreased to zero, and the energy stored in the stray inductance has been transferred to the snubber capacitor C_{sp}.

Mode 0-, Fig. 4(h): Another initial mode in which switch S_p is on but the diode D_p is conducting the load current, i_L. Again, an inductive load is considered and the load current remains constant during the switching process.

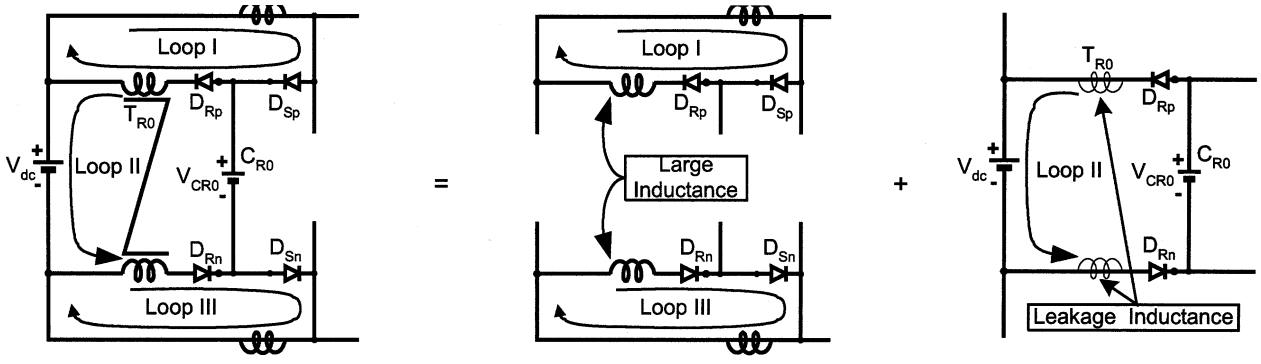


Fig. 5. Operating principle of the energy recovery circuit. (a) Equivalent circuit of the energy recovery circuit. (b) The transformer acts as a large inductance to Loops I and III to minimize circulating current. (c) The transformer has zero (or minimal leakage) inductance toward Loop II to maximize energy recovery current and efficiency.

Mode 6, Fig. 4(i): $\mathrm{S_n}$ is turned on, so a portion of the load current is diverted from $\mathrm{D_p}$ to $\mathrm{S_n}$. The current following through $\mathrm{S_n}$ increases as the current through the stray inductance and the diode $\mathrm{D_p}$ decreases.

Mode 7, Fig. 4(j): When load current is completely diverted to $\mathrm{S_n}$, $\mathrm{D_p}$ turns off and a process of charging $\mathrm{C_{sp}}$ and discharging $\mathrm{C_{sn}}$ starts.

Mode 8, Fig. 4(k): When $\mathrm{C_{sn}}$ is fully discharged and clamped at zero voltage, the charging current starts to decrease. During this mode, as the voltage across the capacitor $\mathrm{C_{S0}}$ becomes higher than the dc source voltage, the energy recovery circuit starts to transfer energy from the capacitor back to the dc source.

Mode 9, Fig. 4(l): The charging current has dropped to zero, and the energy stored in the stray inductance has been transferred to the snubber capacitor $\mathrm{C_{sp}}$.

Fig. 5 indicates the operating principle of the energy recovery circuit. This circuit has three current loops as illustrated in Fig. 5(a). Loop I includes the stray inductance of the positive dc link, the diodes $\mathrm{D_{Sp}}$ and $\mathrm{D_{Rp}}$, and one of the transformer windings. Loop II is the energy recovery path and consists of the diodes $\mathrm{D_{Rp}}$ and $\mathrm{D_{Rn}}$, the capacitor $\mathrm{C_{R0}}$, the dc source, and the transformer. Loop III is the negative counterpart of loop I and includes the stray inductance of the negative dc link, the diodes $\mathrm{D_{Sn}}$ and $\mathrm{D_{Rn}}$, and the other transformer winding. The transformer is connected like a common mode choke and thus presents a large inductance to Loops I and III, as illustrated in Fig. 5(b), to minimize the loop circulating currents. On the other hand, only the leakage inductance of the transformer is seen in loop II, as indicated in Fig. 5(c), thus maximizing the energy recovery current and efficiency.

III. Simulation and Experimental Results

Fig. 6 shows simulation waveforms of the three-phase PSSS inverter prototype, where I(RLa) is phase a load current, Vsan is phase a lower device voltage, and Viab is the inverter output voltage between phase a and b. The snubber circuit parameters are shown in Fig. 2, with the dc voltage $V_{dc} = 330$ V and stray inductance $L_s = 1\ \mu$H. The turn-on and turn-off waveforms of Vsan clearly show that dv/dt is reduced and voltage overshoot is clamped at well below 400 V.

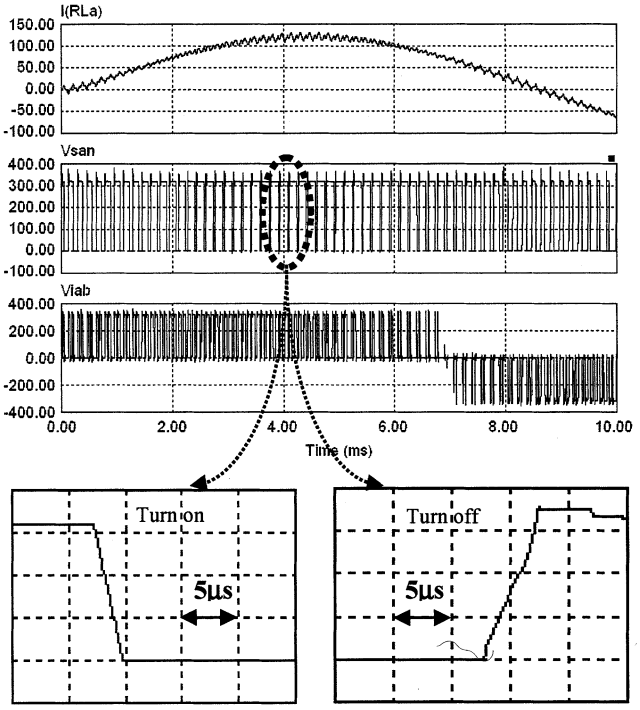


Fig. 6. Simulation waveforms showing phase-a load current, phase-a lower device voltage, and inverter output voltage between phase-a and -b.

Fig. 7 shows a photo of a 150 kVA three-phase PSSS inverter prototype. No dc bus planes were employed, greatly simplifying the dc bus structure. A toroidal magnet was used as the transformer core. As a well-known technique, today's inverters use sophisticated laminated buses to suppress voltage spikes and to reduce switching loss. As power ratings go up, laminated buses become a great challenge due to cost and physical size and distance. The PSSS circuit provides an alternative to the solution.

Fig. 8 shows experimental waveforms of the prototype, where Vcep and Vcen are the voltage across the upper and lower switches of a phase leg, respectively, and $\mathrm{I_{Rp}}$ and $\mathrm{I_{Rn}}$ represent the energy recovery currents in the transformer windings. The turn-off dv/dt is well suppressed at around 300 V/μs, which is much lower than in a hard-switched PWM inverter, whose dv/dt can easily be higher than 3000 V/μs even

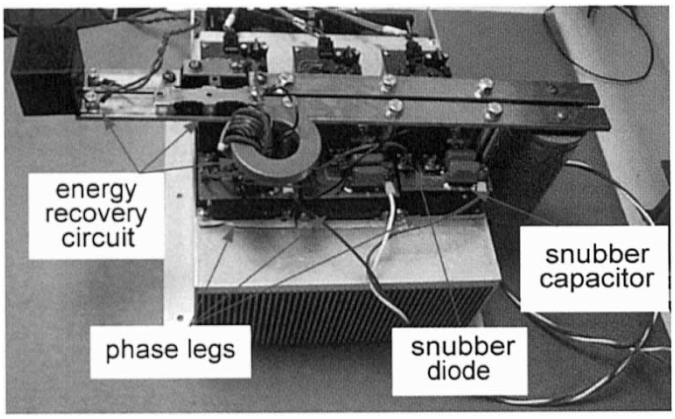


Fig. 7. Photo of a 150 kVA PSSS inverter prototype.

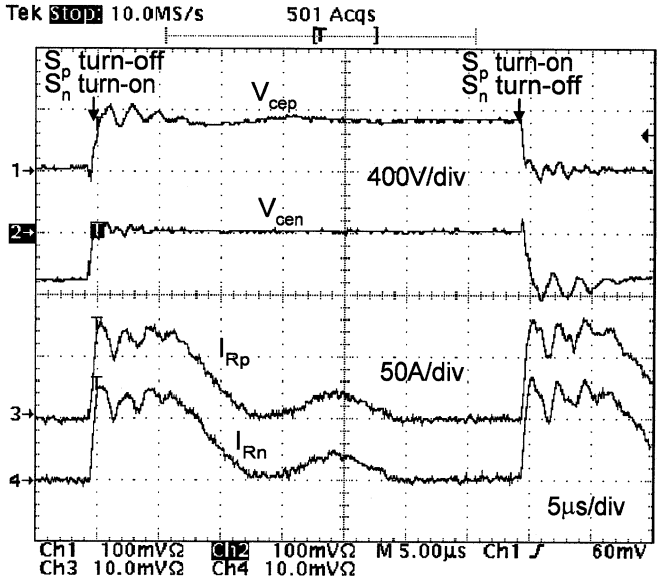


Fig. 8. Experimental waveforms.

with sophisticated laminated busbars. During each switching, a pulse current on $\mathrm{I_{Rp}}$ and $\mathrm{I_{Rn}}$ sends snubber energy back to the dc link capacitor, $\mathrm{C_{dc}}$.

Fig. 9 shows a comparison of voltage and current switching waveforms for the prototype inverter with the PSSS circuit [Fig. 9(a)] and with this circuit replaced with a 4.7 μF bus snubber capacitor on each phase [Fig. 9(b)]. First, the inverter had no laminated dc bus, and with the dc electrolytic capacitors located 20 cm away from the mid phase leg of the inverter, it would not be operable without snubber circuits because of unacceptable voltage spikes. Therefore, a relatively large 4.7 μF bus snubber capacitor was added to each phase leg of the "standard" inverter, making the total capacitance 14.1 μF more than twice that employed in the PSSS circuit. Even with a much larger capacitance, the "standard" inverter generates a higher spike voltage at the turn-on of the switch Sp as revealed in Fig. 9(c). Secondly, note that the time scale of Fig. 9(a) is five times that of Fig. 9(b), which indicates that the PSSS circuit greatly reduced dv/dt to five times smaller than the traditional inverter. As a result, the EMI was reduced, which can be observed from ringing of the load current i_a. Another observation from the waveforms [Fig. 9(a)] of the PSSS inverter is that the dv/dt at turn-on was greater than that at turn-off and greater than the simulation results [Fig. 6(b)]. The reason is because the actual stray inductance of the dc bus is smaller than the 1 μH used in the simulation. The turn-on dv/dt is determined by the stray inductance and snubber capacitance, which will be detailed in the next section. Fig. 10 shows inverter output voltage waveforms and the current drawn from a RL load. Fig. 11 shows the efficiency of the overall inverter with the PSSS compared to that of the "standard" inverter with conventional bus snubber capacitors. The overall efficiency had no appreciable difference between the two cases. That is because the stray inductance from the electrolytic capacitor was relatively small (0.2 μH estimated for 20 cm distance) and was well decoupled by the large 4.7 μF bus snubber capacitor connected to each phase leg of the "standard" inverter. Switching loss is mostly determined by the stray inductance from the closest capacitor to the switch.

IV. PSSS Circuit Design and Considerations

A. Snubber Circuit Design

As discussed in Sections II and III, the dv/dt and di/dt are determined by the snubber capacitance C_S and stray inductance L_s and partially by the load current. The highest dv/dt happens in Modes 4 and 7 when the dc link forms a resonant circuit through the stray inductance and snubber capacitor. For Modes 4 and 7, the upper snubber capacitor voltage V_{Csp} can be expressed as

$$V_{Csp}(t) = V_{Cs0} - (V_{Cs0} - V_{Csp}(0))\cos(\omega t) + \frac{I_{Ls}(0)}{\omega C_S}\sin(\omega t) \tag{2}$$

where V_{Cs0} is almost a constant that equals the dc voltage as shown in Fig. 3, $V_{Csp}(0)$ is the initial voltage of the upper snubber capacitor, $I_{Ls}(0)$ is the initial current through the stray inductor, and $\omega = 1/\sqrt{(2L_s)C_s}$ is the resonant frequency.

The load current affects the initial voltage of the upper capacitor, $V_{Csp}(0)$, and initial current, $I_{Ls}(0)$. The dv/dt from (2) is obtained as

$$\frac{d}{dt}V_{Csp}(t) = \omega\left(V_{Cs0} - V_{Csp}(0)\right)\sin(\omega t) + \frac{I_{Ls}(0)}{C_S}\cos(\omega t). \tag{3}$$

As can be seen from (3), if the snubber capacitance is properly designed so that the dv/dt contributed by the initial current is contained, the highest dv/dt occurs at $\omega t = \pi/2$ when the load current is zero, which results in zero initial voltage and current. The highest dv/dt, equal to ωV_{Cs0}, is therefore determined by the resonance frequency of $2L_S$ and C_S, ω. The highest di/dt also occurs in Modes 4 and 7, which can be expressed as

$$\frac{di}{dt} = \frac{V_{Cs0}}{2L_s}. \tag{4}$$

Therefore, it is obvious that the stray inductance and snubber capacitor are employed to limit both dv/dt and di/dt. Given target

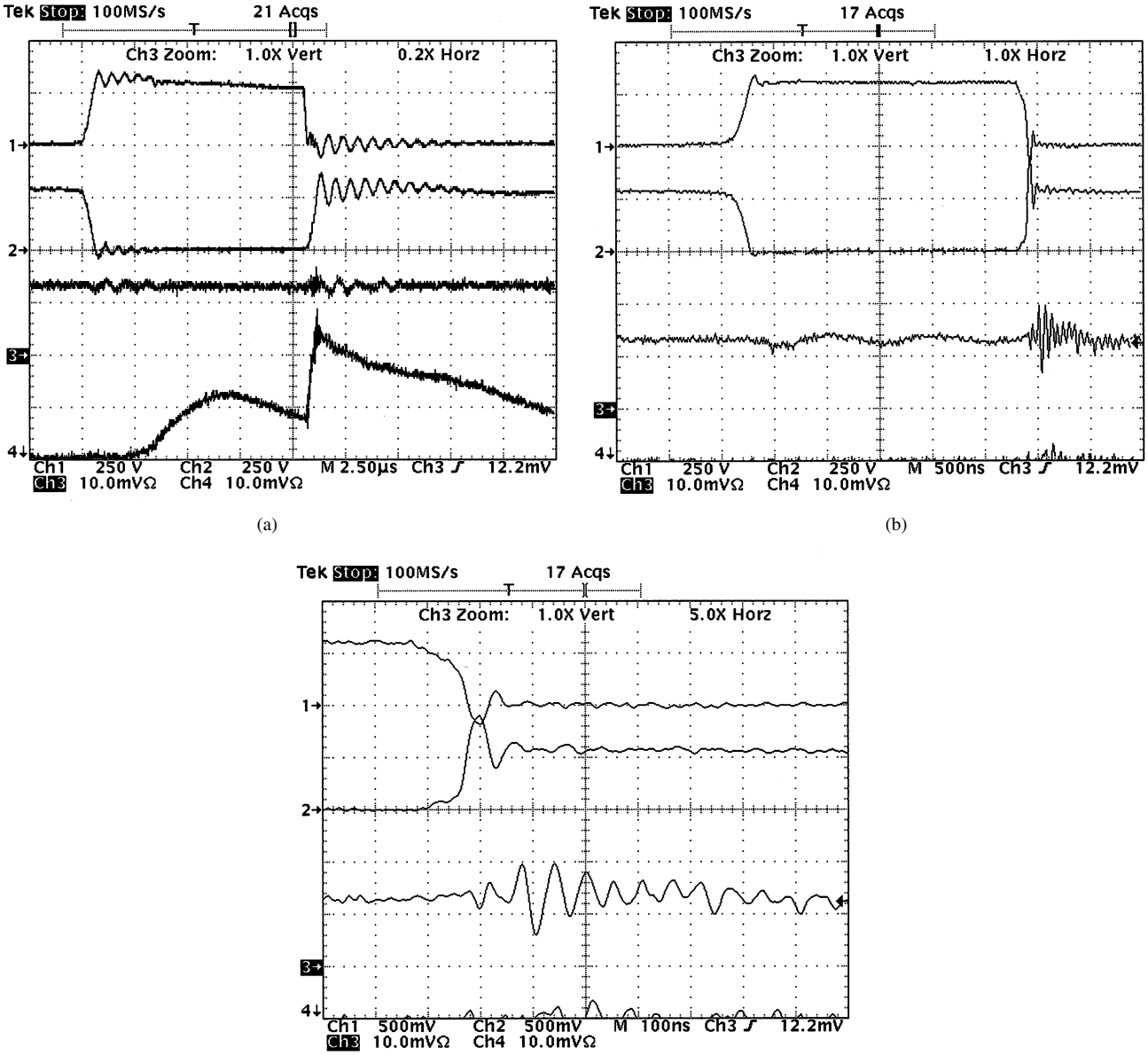


Fig. 9. Comparison of switching waveforms: (a) with the PSSS. Ch1: V_{aCEP}, 250 V/div; Ch2: V_{aCEN}, 250 V/div; Ch3: i_a, 100 A/div; Ch4: I_{Rn}, 50 A/div; time, 2.5 μs/div, (b) "standard" inverter with 4.7 μF bus snubber capacitor on each phase. Ch1: V_{aCEP}, 250 V/div; Ch2: V_{aCEN}, 250 V/div; Ch3: i_a, 100 A/div; time, 0.5 μs/div, and (c) a zoom-up of (b) to reveal a higher spike voltage generated at the turn-on of the upper switch. Time: 0.1 μs/div.

numbers for dv/dt and di/dt, snubber capacitance and stray inductance can be determined. The rule of thumb for estimating the stray inductance is 1 μH per 1-meter of conductor length.

B. Energy Recovery Circuit Design: Rating and Efficiency

The average power to be recovered through the energy recovery circuit, expressed in (1), includes two terms. The first term is related to the energy stored in the snubber capacitors, and the second term is related to the energy recovered from the stray inductance over a fundamental cycle. While the latter, denoted as $P_{R(Ls)}$, depends on the load current, I_{Lrms}, and switching sequences, it may be approximated by the following equation (the complete derivation can be found in Appendix I) for a three-phase inductive load, provided that the switching frequency is significantly higher than the fundamental frequency and any switching instance completes before the next one starts so that they do not interfere with each other

$$P_{R(Ls)} \approx 4.31 L_s I_{Lrms}^2 f_{sw}. \tag{5}$$

Total recovered power for the prototype at a load current of 250 Arms can be calculated by

$$\begin{aligned} P_R &= \left(6\times 0.1\ \mu\,\mathrm{F}\times(400\ \mathrm{V})^2 + 4.31\times 1\ \mu\,\mathrm{H}\times 250^2\right)\times 10\ \mathrm{kHz} \\ &= 3654\ \mathrm{W}. \end{aligned} \tag{6}$$

This power has to be recovered through the recovery circuit, comprising the transformer, $\mathrm{T_{R0}}$, and diodes, $\mathrm{D_{Rp}}$ and $\mathrm{D_{Rn}}$,

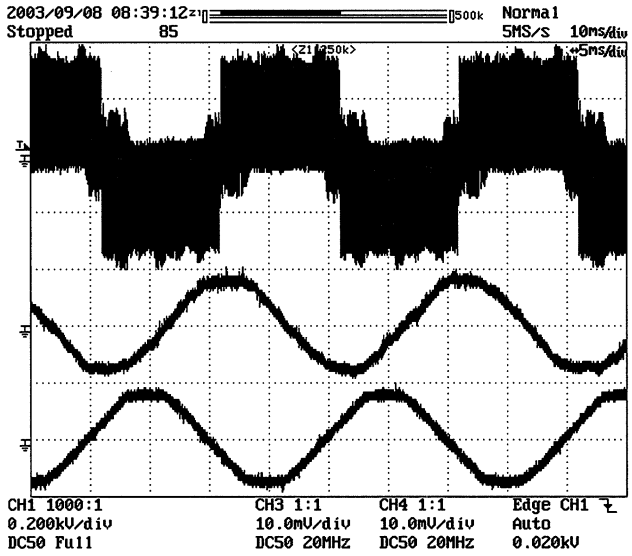


Fig. 10. Inverter output waveforms. From top to bottom: v_{ab}, 200 V/div; i_c, 200 A/div; i_b, 200 A/div, Time: 5 ms/div.

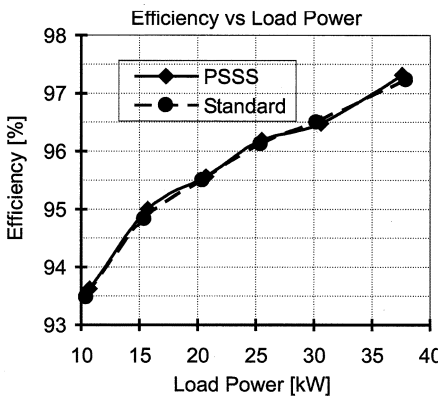


Fig. 11. Efficiency comparison chart. Load power is varied by adjusting the modulation index with a fixed $R - L$ load.

back to the dc source. Fig. 8 shows the recovery current waveforms, $\mathrm{I_{Rp}}$ and $\mathrm{I_{Rn}}$, at each switching instant. Therefore, the average recovery current is

$$I_{R\_avg} = \frac{P_R}{V_{dc}} = \frac{3654\ \mathrm{W}}{330\ \mathrm{V}} = 11\ \mathrm{A}. \tag{7}$$

The transformer and the diodes can be designed by this average recovery current. Assuming the voltage drop across each diode is V_D and the winding resistance is R_t, the power loss and energy recovery efficiency of the circuit can be approximately expressed as

$$P_{loss} \approx 2I_{R\_avg}^2 R_t + 2V_D I_{R\_avg}, \tag{8}$$

$$\eta = 1 - \frac{P_{loss}}{P_R}. \tag{9}$$

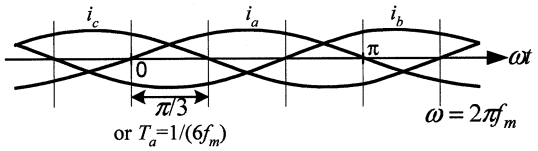


Fig. 12. Three-phase load current, divided into six sections over one fundamental period.

For the prototype, the recovery efficiency was calculated to be 97% by using measured currents as shown in Fig. 8 and assuming $R_t = 0.3\,\Omega$ and $V_D = 1.0$ V.

V. Conclusion

The presented PSSS circuit has the following features:

- employs only passive components;
- requires no additional control;
- allows any PWM schemes;
- eliminates dc bus plane layout;
- utilizes stray inductance;
- reduces dv/dt and di/dt;
- lowers total inverter cost and improves reliability.

The PSSS provides a viable alternative to existing soft-switching inverters. The PSSS is especially suited for silicon carbide (SiC) device inverters because SiC diodes have no or minimal reverse recovery current, which reduces dv/dt uniformly at both turn-on and turn-off to further soften the switching.

Appendix I

Estimation of energy recovered from the stray inductance.

Assume energy needs to be recovered only when a phase leg is switched from a current carrying switch to a diode. It is further assumed that the time between two consecutive switching instances is long enough that they do not interfere with each other. Fig. 12 shows the three-phase load current, which can be divided into six sections over one fundamental period. The energy recovered over the first section can be calculated by

when phase a switching:
$E_{R(Ls)\_a} = L_s \sum_{k=1}^{m} (i_{b(k)}^2 - i_{c(k)}^2)$;

when phase b switching:
$E_{R(Ls)\_b} = L_s \sum_{k=1}^{m} i_{b(k)}^2$;

when phase c switching:
$E_{R(Ls)\_c} = L_s \sum_{k=1}^{m} (i_{b(k)}^2 - i_{a(k)}^2)$;

where $m = f_{sw}/(6f_m)$, respectively.

The total recovered energy is

$$E_{R(Ls)} = L_s \sum_{k=1}^{m} \left(3i_{b(k)}^2 - i_{a(k)}^2 - i_{c(k)}^2\right).$$

The average power is thus

$$
\begin{aligned}
P_{R(Ls)} &= \frac{1}{T_a} L_s \sum_{k=1}^{m} \left(3i_{b(k)}^2 - i_{a(k)}^2 - i_{c(k)}^2 \right) \\
&= 6 f_m L_s \sum_{k=1}^{m} \left(3i_{b(k)}^2 - i_{a(k)}^2 - i_{c(k)}^2 \right) \\
&= 6 f_m f_{sw} L_s \sum_{k=1}^{m} \left(3i_{b(k)}^2 - i_{a(k)}^2 - i_{c(k)}^2 \right) \frac{1}{f_{sw}} \\
&\approx f_{sw} L_s \left[6 f_m \int_0^{\frac{1}{(6 f_m)}} \left(3i_{b(t)}^2 - i_{a(t)}^2 - i_{c(t)}^2 \right) dt \right] \\
&= f_{sw} L_s \frac{3}{\pi} \int_0^{\frac{\pi}{3}} \left(3i_{b(\omega t)}^2 - i_{a(\omega t)}^2 - i_{c(\omega t)}^2 \right) d\omega t \\
&= \frac{3 f_{sw} L_s}{\pi} \int_0^{\frac{\pi}{3}} \left(3i_{b(\omega t)}^2 - 2i_{a(\omega t)}^2 \right) d\omega t \\
&= \frac{3 f_{sw} L_s (\sqrt{2} I_{Lrms})^2}{\pi} \\
&\quad \times \int_0^{\frac{\pi}{3}} \left[3 \sin^2 \left(\omega t - \frac{2\pi}{3} \right) - 2 \sin^2 (\omega t) \right] d\omega t \\
&= f_{sw} L_s I_{Lrms}^2 \left[1 + \frac{6\sqrt{3}}{\pi} \right] \\
&= 4.31 f_{sw} L_s I_{Lrms}^2
\end{aligned}
$$

REFERENCES

[1] D. M. Divan, "Static power conversion method and apparatus having essentially zero switching losses and clamped voltage levels," U.S. Patent 4 864 483, Sept. 5, 1989.

[2] R. W. A. A. DeDonker and J. P. Lyons, "Auxiliary quasi-resonant dc link inverter," U.S. Patent 5 172 309, Dec. 15, 1992.

[3] H. K. Lauw and R. S. Zedwick, "Voltage clamped parallel resonant inverter with controllable duty cycle," U.S. Patent 5 559 685, Sept. 24, 1996.

[4] D. M. Divan and G. Venkataramanan, "Comparative evaluation of soft switching inverter topologies," *EPE Firenze*, 1991.

[5] T. A. Lipo and D. M. Divan, "Resonant links: a new family of inverter topologies for solid state power conversion," in *Proc. ABB Symp. Power Semicond. Devices Circuits*, Sept. 26–27, 1991.

[6] J. S. Lai and B. K. Bose, "An improved resonant DC link inverter for induction motor drives," in *Proc. IEEE Ind. Applicat. Soc. Annu. Meeting*, 1988, pp. 742–758.

[7] T. G. Habetler and D. M. Divan, "Performance characterization of a new discrete pulse modulated current regulator," in *Proc. IEEE Ind. Applicat. Soc. Annu. Meeting*, 1988, pp. 395–405.

[8] H. Mao, F. C. Lee, X. Zhou, and D. Borojevic, "Improved zero-current transition inverter for high power applications," in *Proc. IEEE Ind. Applicat. Soc. Annu. Meeting*, 1996, pp. 1145–1152.

[9] J. S. Lai, R. W. Young Sr., G. W. Ott, Jr., J. W. McKeever, and F. Z. Peng, "A delta configured auxiliary resonant snubber inverter," in *Proc. IEEE Ind. Applicat. Soc. Annu. Meeting*, 1995, pp. 2618–2624.

[10] F. Z. Peng and D. J. Adams, "An auxiliary quasiresonant tank soft-switching inverter," in *Proc. IEEE Ind. Applicat. Soc. Annu. Meeting*, Rome, Italy, Oct. 8–12, 2000, pp. 2397–2403.

Fang Z. Peng (M'92–SM'96) received the B.S. degree in electrical engineering from Wuhan University, China, in 1983 and the M.S. and Ph.D. degrees in electrical engineering from Nagaoka University of Technology, Japan, in 1987 and 1990, respectively.

He was with Toyo Electric Manufacturing Company, Ltd., Tokyo, Japan, from 1990 to 1992, as a Research Scientist, was engaged in research and development of active power filters, flexible ac transmission systems (FACTS) applications and motor drives. From 1992 to 1994, he worked with Tokyo Institute of Technology as a Research Assistant Professor, initiated a multilevel inverter program for FACTS applications and a speed-sensorless vector control project. From 1994 to 2000, he worked for Oak Ridge National Laboratory (ORNL), as a Research Assistant Professor at the University of Tennessee, Knoxville, from 1994 to 1997, and was a Staff Member, Lead (principal) Scientist of the Power Electronics and Electric Machinery Research Center, ORNL, from 1997 to 2000. In 2000, he joined Michigan State University, East Lansing, as an Associate Professor of the Department of Electrical and Computer Engineering. He is currently a specially invited Adjunct Professor of Zhejiang University, China. He holds over 10 patents.

Dr. Peng received the 1996 First Prize Paper Award and the 1995 Second Prize Paper Award of Industrial Power Converter Committee in the IEEE/IAS Annual Meeting, the 1996 Advanced Technology Award of the Inventors Clubs of America, Inc., the International Hall of Fame; the 1991 First Prize Paper Award in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, the 1990 Best Paper Award in the Transactions of the IEE of Japan, and the Promotion Award of Electrical Academy. He has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 1997 and Chair of Technical Committee for Rectifiers and Inverters, IEEE Power Electronics Society.

Gui-Jia Su (M'94–SM'01) received the B.S. degree in electrical power system engineering from Wuhan University (formerly Wuhan University of Hydraulic and Electrical Engineering), Wuhan, China, in 1985, and the M.S. and Ph.D. degrees in electrical engineering from Nagaoka University of Technology, Nagaoka, Japan, in 1989 and 1992, respectively.

He was an Assistant Professor from 1992 to 1995 at Nagaoka University of Technology. From 1995 to 1998, he was with Sanken Electrical Co., Ltd., Kawagoe, Japan, where he has engaged in research and development of uninterruptible power supply, sensorless PM motor drive, and power factor correction for single- and three-phase rectifiers. In 1998, he started working in the Power Electronics and Electric Machinery Research Center (PEEMRC), Oak Ridge National Laboratory, Knoxville, TN, as a Research Scientist with the Oak Ridge Associated Universities. He joined ORNL in 2000 as a Staff Member and is currently a Senior R&D Staff Member. He holds the position of Lead Engineer of power electronics in PEEMRC, National Transportation Research Center (a joint center of ORNL and the University of Tennessee). His current research interests include high power dc/dc converter, inverter, motor drive, and power electronics system packaging and thermal management for electric/hybrid electric vehicle applications. He holds four patents.

Dr. Su received the IEEE Industrial Electronics Society IECON'01 Best Presentation Award in 2001 and the IEEE IAS Industrial Drive Committee Third Prize Paper Award in 1993.

Leon M. Tolbert (S'89–M'91–SM'98) received the B.E.E., M.S., and Ph.D. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta.

He joined the Engineering Division, Lockheed Martin Energy Systems, in 1991 and worked on several electrical distribution projects at the three U.S. Department of Energy plants in Oak Ridge, TN. In 1997, he became a Research Engineer in the Power Electronics and Electric Machinery Research Center, Oak Ridge National Laboratory, Knoxville, TN. In 1999, he was appointed Assistant Professor in the Department of Electrical and Computer Engineering, University of Tennessee, Knoxville. He is an Adjunct Participant at the Oak Ridge National Laboratory and conducts joint research at the National Transportation Research Center (NTRC). He does research in the areas of electric power conversion for distributed energy sources, motor drives, multilevel converters, hybrid electric vehicles, and application of SiC power electronics.

Dr. Tolbert received the National Science Foundation CAREER Award and the 2001 IEEE Industry Applications Society Outstanding Young Member Award. He is an Associate Editor of the IEEE POWER ELECTRONICS LETTERS and a Registered Professional Engineer in the state of Tennessee.