A Phase-Locked Loop Reference Spur Modelling using Simulink

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***Abstract*— Phase-Locked Loops (PLLs) are a commonly used module in frequency synthesizers as part of RF transceivers. Simulating these modules is very time consuming. Therefore, a number of approaches to evaluate the performance of these modules through high level behavioural modelling are developed, where the focus is on the random noise aspect of these modules. In this paper, we introduce charge pump and Phase/Frequency Detector (PFD) non-idealities in the integer-N PLL behavioural model to estimate the periodic noise, which is also known as reference spurs. In addition, the effect of the VCO gain, loop filter order and loop bandwidth on the reference spurs level are taken into consideration. The proposed model was implemented in Simulink and showed less than $\pm 3\%$ error when compared to transistor level simulations from Cadence Spectre. Using this approach a 10 time improvement in simulation speed was achieved compared to transient analysis from Cadence Spectre.**

I. Introduction

A Phase-Locked Loop (PLL) based frequency synthesizer is one of the important circuit modules in RF transceivers. The module provides a reference frequency for a mixer to translate a baseband signal to an RF signal on the transmitter side, and from an RF signal to a baseband signal on the receiver side. The PLL module consists of a Voltage-Controlled Oscillator (VCO), frequency divider, Phase/Frequency Detector (PFD), charge pump (CP) and low pass filter (LPF) as shown in Figure 1.

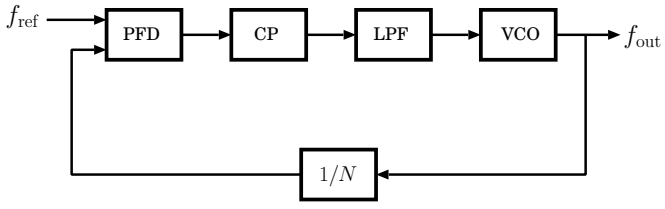

Fig. 1. Phase-Locked Loop

The PFD compares the divided output signal, f_{out} to a reference clock, f_{ref}. The phase error between these signals is converted into a voltage using the charge pump and filtered using the low pass filter, then feed as a control signal to the VCO to adjust it's output frequency accordingly.

Two types of PLL architectures are commonly used in RF transceivers, namely an integer-N PLL and fractional-N PLL. As the name state, an integer-N PLL, the output signal frequency is an integer multiple of the reference frequency. While for a fractional-N PLL, the output frequency is a fraction of the reference signal frequency. The choice between these architectures is based on frequency planning needed by the transceiver. The presented model is aimed at the integer-N architecture for a 60 GHz transceiver [1].

The PLL performance is based on the noise seen at its output. There are two types of noise, random noise and periodic noise. Random noise is also known as phase noise, while periodic noise for integer-N architecture is called reference noise, which at a specified offset frequency from a carrier frequency.

The noise performance at the PLL output depends on the loop bandwidth. A large loop bandwidth helps to improve the close-in band noise. Furthermore, large loop bandwidth reduces the PLL settling time. However, a small loop bandwidth is required to suppress the reference spurs. Therefore, a trade-off between the loop bandwidth, maximum noise level and maximum settling time in a PLL has to be considered.

Reference spurs are a serious issue in RF transceivers. A spur can degrade the signal-to-noise-ratio in data reception and transmission. This spur is caused by non-idealities in the PFD and charge pump circuits. These non-idealities are discussed in Section II. In the literature, a number of approaches have been devised to eliminate or minimize the non-idealities in these circuits to minimize the reference spurs [2]–[5]. However, the affect of non-idealities on the reference spur have not been modelled. In this paper, we investigate the effect of these non-idealities generated from the circuit level and demonstrate how they influence the reference spurs. Conducting such evaluation at the transistor level would take a very long simulation time. Therefore, we present a behavioural model to reduce the simulation time while considering the dominant non-idealities with minimal impact on the performance estimation accuracy.

The contribution of this paper is to include the modelling of PFD and charge pump non-idealities in the PLL Simulink behavioural model. These non-idealities are introduced to model the reference spurs in the integer-N PLL. By using the proposed behaviour model, effect of the VCO gain, loop filter and loop bandwidth on the reference spurs can be investigated at a fraction of the time needed to do full transistor level simulation.

In Section II, the reference spurs and its sources are dis-

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cussed, in Section III the PLL linear model and its implementation in Simulink are discussed. The effect of the PFD and charge pump circuit non-idealities, combined with the PLL parameters on the reference spurs are discussed in IV, this is then followed by conclusion in Section V.

II. REFERENCE SPURS

The main contributions to the reference spurs in an integer-N PLL are PFD delay, charge pump switching delay, charge pump current leakage, charge pump current mismatch, charge injection and charge sharing [6], [7]. Figure 2 shows commonly used PFD and charge pump circuits in PLL design.

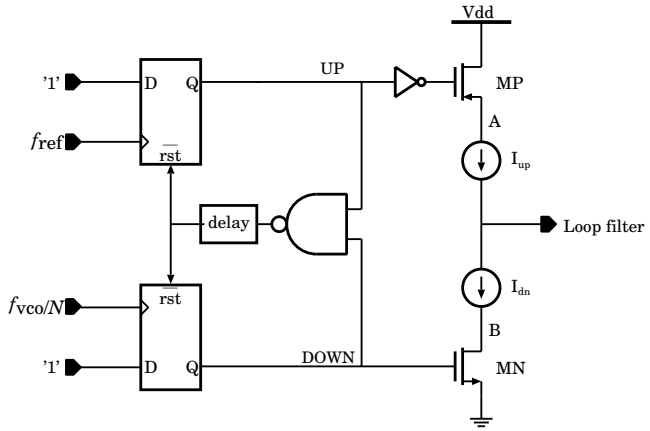

Fig. 2. Phase/Frequency Detector (PFD) and charge pump circuits

The two PFD output signals, labelled as UP and DOWN signal in the diagram, control the charge pump switching. The UP switch is using a PMOS, while the DOWN switch is using an NMOS. An equal amount of delay on both these signals is needed to eliminate *dead zone* problem. So, the PFD delay itself does not contribute to reference spurs. On the other hand, a differential delay between these signals introduce reference spurs, as this will cause either the $I_{\rm up}$ or $I_{\rm dn}$ to be on for a longer period of time. In circuit implementation of the PFD circuit, this differential delay is a result of an inverter required on the UP switch in order to turn it ON. The delay could be minimized by using transmission gate to match the UP and DOWN signals [6] or using complementary differential cascode inverter. However, the delay still cannot be fully eliminated and result in maximum reference spurs at the PLL output.

When UP and DOWN switches in charge pump are OFF, there should be zero net current flow to the filter circuit. However, there is still a very small current due to leakage current in the UP and DOWN transistors of the CP circuit. The amount of this current depends on the used technology. For the selected process (0.18 μm SiGe BiCMOS technology from Jazz semiconductor), the calculated current leakage in these transistors are 25 pA and 29 pA for the PMOS and NMOS transistors, respectively.

Ideally, $I_{\rm up}$ should equal $I_{\rm dn}$ in a charge pump. However, because of the process variation and channel length modulation effect on the current mirror structures, $I_{\rm up}$ and $I_{\rm dn}$ are slightly different. This mismatch can be as large as 10%-20% between these currents, depending on the current source structure, transistor sizes and used fabrication technology.

Other causes of the reference spurs are charge injection and charge sharing in MN and MP. The charge injection is from charges stored in the channels of the switch transistors when they turn OFF and the charge sharing is from node A and B (shown in Figure 2) in the charge pump when both transistor are ON [8].

III. PLL MODEL

Despite the fact that PLL is a non-linear system, a linearized model can be used with assumption the phase error is small and the loop bandwidth much smaller compared to reference frequency [9]. Based on linear model, we propose a behavioural model for testing and estimating the PLL performance while considering parameters obtained from transistor level simulations.

Many PLL models have been published [10]–[12]. However, none allow for accurate reference spur estimation. In this paper, a PLL Simulink behaviour model that model introduces four non-idealities in the PFD and charge pump components is presented. The aim is to investigate how each non-idealities in PFD and charge pump affect the reference spur level in PLL.

The developed PLL Simulink model is shown in Figure 3. PFD model can be seen at the top left of the figure and charge pump model at the top right of the figure, and the complete PLL block is shown underneath. The VCO was modelled using a continuous time VCO block running at 20.9 GHz with a 1 GHz/V gain. The VCO output is divided by 256 using a frequency divider, then feed to the second input of the PFD. A 81.64 MHz signal was used as a reference frequency.

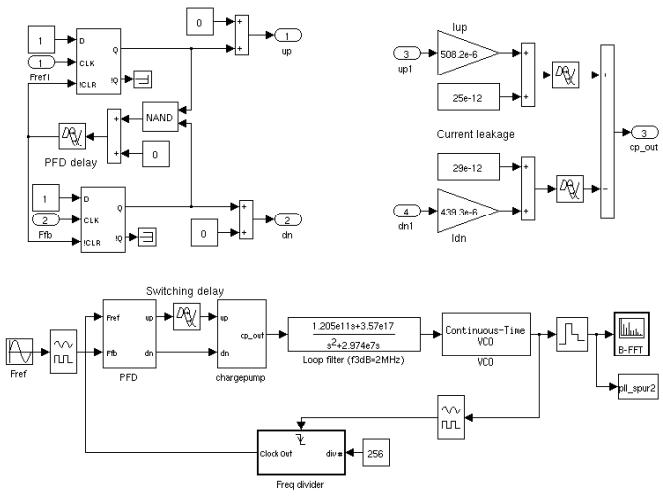

Fig. 3. PLL Simulink model

The PFD is constructed using two D-flipflops and a NAND gate, as shown in Figure 3. The PFD delay is modelled by a

transport delay. For the charge pump, two non-idealities are included, namely current mismatch and current leakage. The amount of charge injection is very difficult to estimate because it is a complex function of various parameters that poorly controlled such as clock transition time [6]. Thus, this factor was not included in the Simulink model. However, based on estimated performance the charge injection has minimal effect on the reference spurs compared to current mismatch and PFD delay. Between the PFD and charge pump, a transport delay was included to model the charge pump switching delay. The charge pump output is then filtered by a low pass filter. A second order low pass filter was used and the filter is modelled by its transfer function. The filter is designed for a 2 MHz loop bandwidth.

All the non-idealities values were retrieved from a transistor level modelling of these components using Cadence Spectre simulation. For the current leakage and current mismatch, a dc analysis was conducted to obtain the current mismatch value at different tuning voltage. Furthermore, a transient analysis was conducted to estimate the PFD delay.

The PLL transistor level schematic was constructed using a 0.18 μm SiGe BiCMOS technology provided by Jazz Semiconductor. As mentioned before, the PLL model presented in this paper is aimed at estimating the reference spurs, which is caused by non-idelaities in PFD and charge pump circuits. Therefore, only PFD, charge pump and loop filter are constructed at the transistor level in Cadence Spectre. The VCO and the frequency divider were constructed using Verilog behaviour modelling language.

IV. MODELLING RESULTS

The reference spurs level was measured from the Simulink model simulation and was compared to reference spurs levels measured from Cadence Spectre simulation, as shown in Figure 4. The maximum error between simulink and Cadence spectre simulation is less than $\pm 3\%$. It is suspected that this difference is due to the dynamic mismatch behaviour of the current mirrors.

Using the proposed Simulink model, the effects of PFD delay and current mismatch on the reference spurs level were estimated. The current leakage effect on reference spur could be reduced with a large charge pump current [13]. In this work, the current leakage (less than 30 pA) is very small compared to charge pump current (500 uA). Therefore, the effect of current leakage could be neglected. While the effect of VCO gain and loop filter bandwidth and order on the reference spur level were considered as discussed below.

A. PFD Delay Effect

In order to investigate the effect of the PFD delay on the reference spurs using the proposed model, the PFD delay was changed from 230 ps to 330 ps in 10 ps steps, as shown in Figure 5. Based on the transistor level simulation, 230 ps is the minimum delay to avoid the *dead zone* problem. It is clear from the figure that the larger PFD delay the further increase in the reference spur level. The left hand side y-axis shows

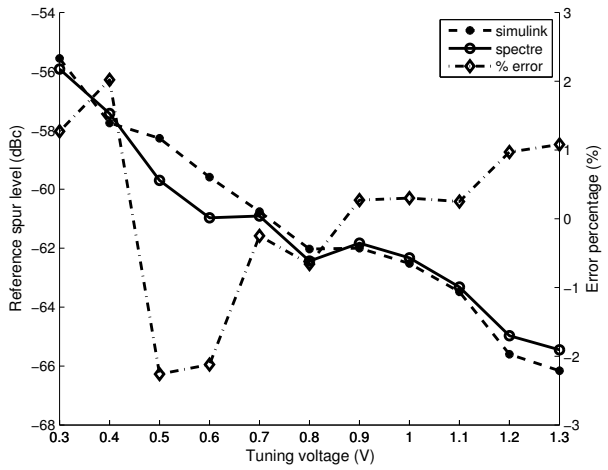

Fig. 4. Reference spur level from Simulink model and Cadence Spectre

the amount of reference spur level in dBc at 78.125 MHz offset from the carrier frequency (20 GHz) for a number of delays of error between Cadence Spectre and Simulink results, where the right hand side y-axis shows the percentage of error between spectre and simulink result.

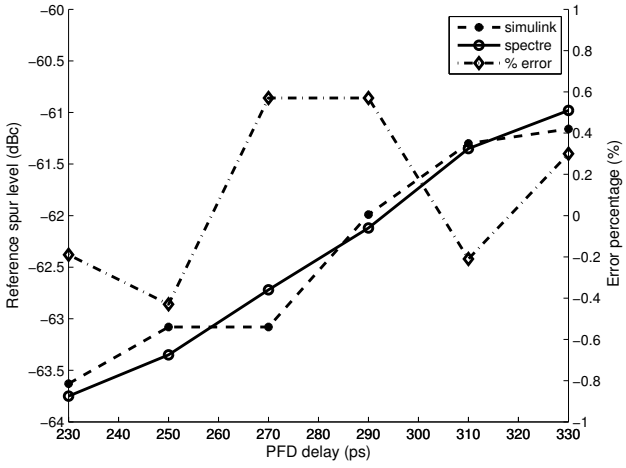

Fig. 5. PFD delay affecting the reference spur level

B. Current Mismatch Effect

Current mismatch in the charge pump is a serious problem in the PLL. Therefore, in the literature a number of approaches are devised to match the $I_{\rm up}$ and $I_{\rm dn}$ [14]–[16]. To investigate the current mismatch effect using the proposed model, two cases are considered. Firstly, when $I_{\rm up}$ larger than $I_{\rm dn}$, while the second is when $I_{\rm dn}$ larger than $I_{\rm up}$.

As shown in the Figure 6, a slightly larger $I_{\rm dn}$ increases the reference spurs performance. In contrast, larger $I_{\rm up}$ decrease the spur performance. This is because the excess $I_{\rm dn}$ com-

pensates for the PFD delay and charge sharing effect on the reference spur level.

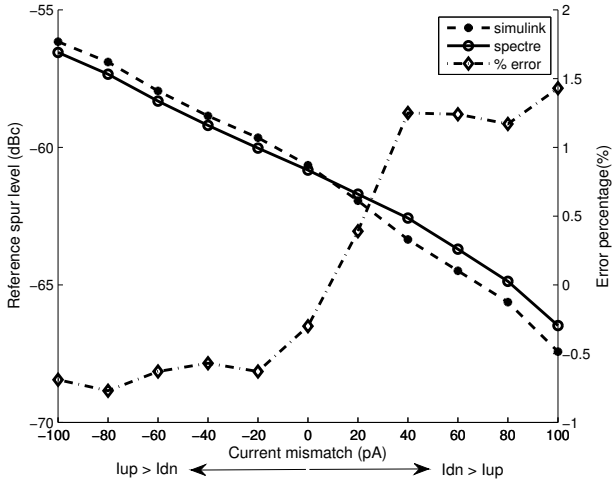

Fig. 6. Current mismatch affecting the reference spur level.

C. VCO gain effect

A PLL should be able to provide a range of output frequencies for channelling purpose. This output range is called PLL tuning range. The VCO gain in a PLL is chosen based on the PLL tuning range requirement. For a large tuning range, the PLL requires a high gain VCO. On the other hand, having a large VCO gain makes the VCO input very sensitive to any noise. In addition to affecting the PLL phase noise performance, this will also increase the reference spur level.

The effect of VCO gain on the reference spur level was examined by sweeping the VCO gain from 1 GHz/V to 2 GHz/V, in steps of 0.1 GHz/V. The reference spur level for each VCO gain is plotted in Figure 7. As shown in the figure, the reference spur level is highly affected by the VCO gain. Therefore, a small VCO gain is good for the reference spurs but not for the tuning range. For this reason, in the literature a number of VCO designs use two varactors, one will allow for course tuning of the VCO gain, while a small varactor is used for fine tuning purposes [17]. Another approach is to use a switched capacitor network in the VCO design, thus a small varactor could be used while maintaining a large tuning range [18].

D. Loop Filter Effect

A passive filter is commonly used in the PLL design. The effect of the filter order on the reference spur level is considered. Also, the reference spur level when using a second order low pass filter is compared to third order low pass filter as function of the loop bandwidth as shown in Figure 8. The loop bandwidth is required to be less than 10% of the reference frequency to maintain the loop stability [19]. This PLL use a 78.125 MHz reference clock. Hence a loop bandwidth of less than 8 MHz is needed. As a large loop bandwidth will result

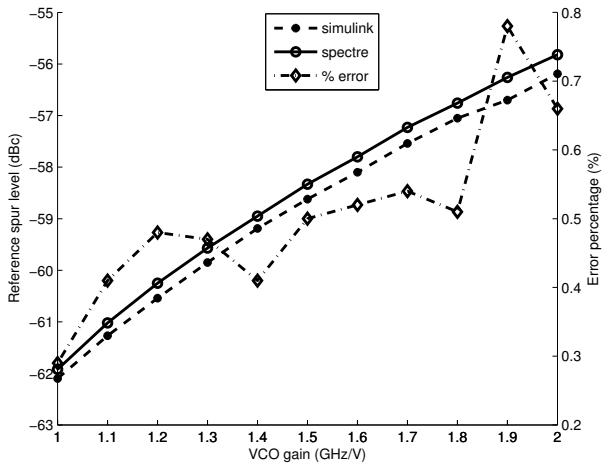

Fig. 7. VCO gain affecting the reference spur level

in a higher contribution of spur noise level, a loop bandwidth ranging from 1 to 4 MHz was used.

The proposed model simulation results is in full agreement with the transistor level simulation to less than $\pm 0.6\%$ error when considering both second and third order loop filters at different values of loop bandwidth. Using a third order filter provides a 5 dB improvement in performance at small bandwidth. The larger increase in the loop bandwidth, will result in a further degradation in the reference spur performance. On the other hand, a small loop bandwidth can cause the PLL to take a very long time to settle. Therefore, a trade-off between loop bandwidth and settling time has to be considered [20].

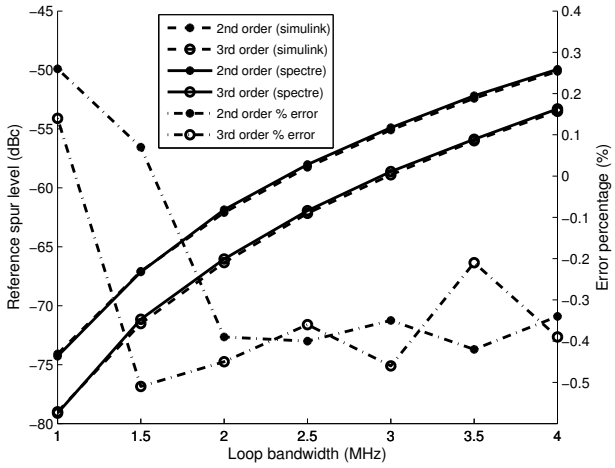

Fig. 8. Loop filter order and loop bandwidth affecting the reference spur level

Due to this reason, many PLL implementations are using third order PLL because of its apparent improvement in the reference spur. Higher order PLL might also help to further reduce the reference spur, but the trade-off is an increase of

the loop filter design complexity and the loop stability.

V. Conclusion

A comprehensive PLL Simulink model has been developed. The model allows the investigation of PFD delay, charge pump current mismatch, VCO gain, and loop filter bandwidth and order effects on the reference spur level. The Simulink model was verified using transistor level simulation based on Cadence Spectre. The difference between estimated performance results by the model and transistor based simulation is less than $\pm 3\%$. Based on this model, a good reference spur performance could be achieved by reducing the PFD delay, charge sharing, charge injection, switching delay, VCO gain, and loop bandwidth, in addition to using higher order loop filter. Also, another interesting observation when I_{dn} was slightly larger than I_{up}, that reference spur level was reduced, an explanation to this effect was also given.

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