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A physics-based approach for power integrity in multi-layered PCBs

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A PHYSICS-BASED APPROACH FOR POWER INTEGRITY IN MULTI-LAYERED PCBs

by

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ABSTRACT

Developing a power distribution network (PDN) for ASICs and ICs to achieve the low-voltage ripple specifications for current digital designs is challenging with the high-speed and low-voltage ICs. Present methods are typically guided by best engineering practices for low impedance looking into the PDN from the IC. A pre-layout design methodology for power integrity in multi-layered PCB PDN geometry is proposed in the thesis. The PCB PDN geometry is segmented into four parts and every part is modelled using different methods based on the geometry details of the part. Physics-based circuit models are built for every part and the four parts are re-assembled into one model. The influence of geometry details is clearly revealed in this methodology. Based on the physics-based circuit mode, the procedures of using the pre-layout design methodology as a guideline during the PDN design is illustrated. Some common used geometries are used to build design space, and the design curves with the geometry details are provided to be a look up library for engineering use.

The pre-layout methodology is based on the resonant cavity model of parallel planes for the cavity structures, and parallel-plane PEEC (PPP) for the irregular shaped plane inductance, and PEEC for the decoupling capacitor connection above the top most or bottom most power-return planes. PCB PDN is analyzed based on the input impedance looking into the PCB from the IC. The pre-layout design methodology can be used to obtain the best possible PCB PDN design. With the switching current profile, the target impedance can be selected to evaluate the PDN performance, and the frequency domain PDN input impedance can be used to obtain the voltage ripple in the time domain to give intuitive insight of the geometry impact on the voltage ripple.

ACKNOWLEDGMENTS

I would like to take this opportunity to express my sincere gratitude to Prof. Drewniak and Prof. Fan for the incredible support and guidance with professional skills development and research work. I would also to thank Prof. Pommerenke for suggestions and inspirations through my master program. I'm also grateful for all the members of the "Electromagnetic Compatibility Laboratory" at Missouri University of Science and Technology for all the support and encouragement through the process.

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1. INTRODUCTION

Printed circuit board (PCB) power distribution network (PDN) design forms a critical part of system design for the high speed digital systems. PDN is used to deliver power to integrated circuits (ICs). A PDN design in a system often consists of multiple power/power-return planes, vias, and decoupling capacitors on printed circuit board (PCB). For high speed digital system, multiple DC supplies are commonly used in the system, resulting in complicated interconnections of DC supplies. Therefore, the PCBs in these systems require many routing and power/ground layers, often exceeding 20-30 layers. And at the same time, the PCBs function at higher frequencies and the components are placed more densely, which increases the interference between the components and makes the system more sensitive to the electromagnetic interference (EMI) problems and signal integrity (SI) problems which occur in these high-speed digital designs. Also, the maximum voltage ripple specifications become lower as the decrease of the power supply. Designing a good PCB PDN geometry is more critical and challenging in high speed digital system design.

EMI and SI problems of a PDN design come from different aspects [1]-[7]. For a system, switching current of ICs from power to power return (often denoted “ground” in designs) gives rise to significant noise in the supply voltage [8]-[9]. The voltage ripple of one DC supply can easily couple to other DC supplies, causing the voltage ripple on the other power nets. Also, the voltage ripple can couple to the nearby signals, which may be amplified later, and cause noise on IOs or disturb the functionalities of the signals. Another problem caused by voltage ripple is radiation. Electromagnetic field lines bend at the edge of the PCB, which causes radiation to space around the edge. Electromagnetic field lines also bend at the discontinuities on the boards, like vias, connectors, and IC packages, leading to reflection and radiation. Voltage ripple can enhance the radiation by coupling to radiating structures like the heat sinks, connector shields, cables, etc. Voltage ripple enhances the radiation to spread energy in the space, which increases the power consumption in a system.

The PDN performance is often analyzed based on the input impedance looking into the PCB from the IC, which is called PDN input impedance. The input impedance is

compared to the target impedance to evaluate the PDN design. Target impedance is selected as the impedance profile which generates the maximum voltage ripple within tolerance [10].

When designing a PCB PDN, engineers would follow some guidelines from experience or 'rules of thumb'. Most of the guidelines come from two-layer or four-layer board analysis, and are not applicable to high-layer PCB PDN structures. While there are commercially available tools [11]-[13] and numerical algorithms [14]-[15] that provide post-layout analysis based on the geometry, like Altium Designer and Cadence Allegro. These tools contain lots of constraints to help designers avoid mistakes and achieve a better PCB layout design. However, most of the layout constraints come from experience based on four-layer or six-layer board analysis. And they can't analyze the performance of the PCB design by running an EM analysis to identify the EMC/EMI or SI problems by itself. More importantly, the results from the post layout simulation tools are not so easily correlate directly with the geometry details in the design. In most design scenarios, the designers have to run multiple simulations or perform large amount of measurements to test the how the performance of the PCB PDN is related to the geometry, and adjust the design incrementally. However, the process is time consuming due to the long simulation time and complexity of the geometries to adjust the geometry details and there is no systematic way of guiding the process.

For higher layer counted PCB PDN, many more decisions has to be made to meet the target impedance specifications, as stack-up, IC pin placement patterns, decap locations, etc. These geometry details have impacts on the equivalent inductance and IC interconnection inductance. For PCB PDN geometry, the impedance profile follows a generic trend as it is dominated by particular geometry details in different frequency range [16]. There are two important features in the PDN impedance profile. The middle frequency range impedance profile is dominated by the current path from the IC to the decaps through the power net area fill and back to the IC, and the higher frequency range impedance profile is dominated by the current path from the IC to the power net are fill and back to the IC [17].

Decoupling capacitors, referred as "decaps" in this paper for convenience, are used to reduce the PDN input impedance by providing sufficient charges to satisfy the current

draw requirements of the IC. The decap placement details leave footprints in the PDN input impedance in the mid-frequency range. Adding decaps can lower the input impedance in this frequency range. The minimum values of the impedance in the frequency range is limited by the IC pin connection inductance. A pre-layout design methodology is developed based on the two current paths. The PCB PDN structures are segmented into four parts and every part is modelled using different methodologies based on the geometric characters of the part. With the switching current profile, the time domain voltage ripple is calculated based on the physics-based circuit model. In the end, all parts in the PCB PDN geometry are combined and a pre-layout methodology is proposed.

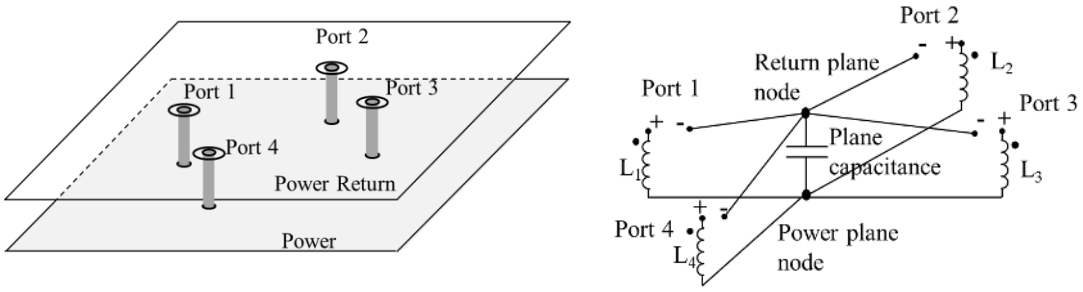
The pre-layout methodology which quantitatively reveals the connection between the PDN performance and geometry details is proposed in this thesis. The methodology enables designers to have a detailed and complete understanding of the influence of the geometries details before the layout, which can be used as guidelines during the design process.

2. PHYSICS BASED METHODOLOGY FOR PCB PDN

The input impedance is modeled based on the physics based equivalent circuits extracted from different methods, due to the geometric details of different structures in the PCB PDN geometry. The basic structure of a PCB PDN geometry is a single cavity formed by two parallel plates. There are two methods used in the thesis based on the shape of the cavity, the cavity model [18] [19] and parallel plate PEEC (PPP) [21]-[24], PPP is able to extract the circuit model for irregular power shape, while the cavity model is applied to rectangular cavity. Apart from the cavities in the PCB PDN geometry, decoupling capacitors are used to lower the PDN input impedance to meet the target impedance. In this thesis, decoupling capacitors are referred as 'decaps' for convenience. However, decaps are not simple capacitances which can be attached to the PCB directly. Pads and traces are used to provide the connection from decaps to the PCB. Also, the decaps have parasitic parameters, but the ESL and ESR values are not sufficient to provide the information to approximate the influence of the decap parasitics on the PDN performance. The model for the connection from the top ground layer to the decaps is referred as L_{above}, which is modelled based on PEEC.

2.1. CIRCUIT EXTRACTION FORM CAVITY MODEL

Two thin metal layers separated by a small distance form a cavity. The distance between the two layers needs to be electric small. The cavity geometry is modeled as planar circuit based on the cavity model [1][18]-[20]. Due to the assumptions on the geometry, electromagnetic principles are used to build a model, which is called the cavity model, to characterize the electric and magnetic fields inside the cavity. Figure 2.1 shows the one cavity with four vias and the equivalent circuit model for this geometry with four vias being set as ports. The circuit model is based on the transfer impedance between the vias of rectangular cavity from the cavity model. The via and the plane around it in the cavity is represented as an inductor. The cavity capacitance is calculated as plane-pair capacitance. For multi-layered PCB PDN geometries, the circuit modelling rule can be extended to include the vias and cavities in the physics-based circuit model.



(a) (b)

Figure 2.1. (a) An open plane-pair cavity with four vias; (b). The equivalent circuit mode based on the cavity model in [17];

The formulation for component values in the equivalent circuit is explained below [17][18]. The impedance looking into a via i in a rectangular cavity when the source is placed at via j can be written as,

$$Z_{ij} = \frac{1}{j\omega C_p} + j\omega L_{ij}(\omega) \tag{1}$$

where, C_p is a parallel plate capacitance for the first cavity mode with (m, n) = (0, 0) given by

$$C_p = \varepsilon \frac{ab}{d} \tag{2}$$

and the inductance is found using,

$$L_{ij} = \frac{\mu d}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{(2-\delta_m)(2-\delta_n)}{k_{mn}^2 - k^2} g_{mni} g_{mnj} \Big|_{(m,n)\neq(0,0)} \tag{3}$$

where,

$$k_{mn}^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2 \quad , \quad k^2 = \omega^2 \mu\varepsilon \quad \text{,and}$$
$$g_{mni} = \cos\left(\frac{m\pi x_i}{a}\right)\cos\left(\frac{m\pi y_i}{b}\right)\text{sinc}\left(\frac{m\pi W_{xi}}{2a}\right)\text{sinc}\left(\frac{m\pi W_{yi}}{2b}\right). \tag{4}$$

Here, a, b, and d: Dimensions of cavity along the x, y, and z directions, respectively,

(x_i,y_i) : Location of the i^{th} port,

W_{xi}, and $W_{yi,}$: i^{th} Port dimensions along the x and y directions, respectively,

m, and n : Cavity mode indices in the x and y directions, respectively,

μ : permeability of the dielectric layer, and

ε : permittivity of the dielectric layer.

δ_m and δ_n : the Keronechker delta function.

The extracted inductance used in the model should be frequency dependence. But, it is found that the inductance value is relatively constant till 60% of the first cavity resonance frequency [18]. For low frequency approximation, it is acceptable to use a single inductance value at DC to find its contribution of the cavity impedance. The infinite summation can be truncated in practice as soon as target convergence is achieved. For the test structure used herein, the mode number m=n=800 is necessary to reach the target convergence within 5% [19].

For multi-layer PCB PDN geometry, the circuit can be built the same way as the single cavity for every cavity. And the equivalent circuit models for all cavities can be assembled together to form the equivalent circuit model for the entire geometry. An example of multilayer planes with the connection of multiple power/ground vias between IC and decoupling capacitors is illustrated in Figure 2.2 (a). Its's one-to-one corresponding circuit model is shown in Figure 2.2 (b), where the capacitance and inductances for a plane pair calculated from (2) are connected in series with those for other plane pairs at the location of vias

2.2. . PARALLEL-PLATE PEEC

The partial element equivalent circuit (PEEC) methodology was proposed in [21]-[24], and has been developed into a mature modelling strategy. The key idea behind this

approach is to divide the geometry into electrically small cells, which can be modelled with lumped circuits due to very small functional variation of field quantities along the cells. For different field components, there may be different types of cells as long as the nodes from different types of cells coincide to allow forcing voltage and current continuity at these nodes. An application of this methodology to the parallel plane structure in PCB stack-up, called plane-pair PEEC (PPP), where the planes were assumed to be thin metal sheets with equal and opposite currents on the top and bottom conductors. Orthogonal mesh cells are applied to both planes to form cell pairs which take advantage of the fast decay in the inductive coupling between the different elements [24]. Figure 2.3 shows the mesh for vias in a single cavity geometry by using the PPP approach.

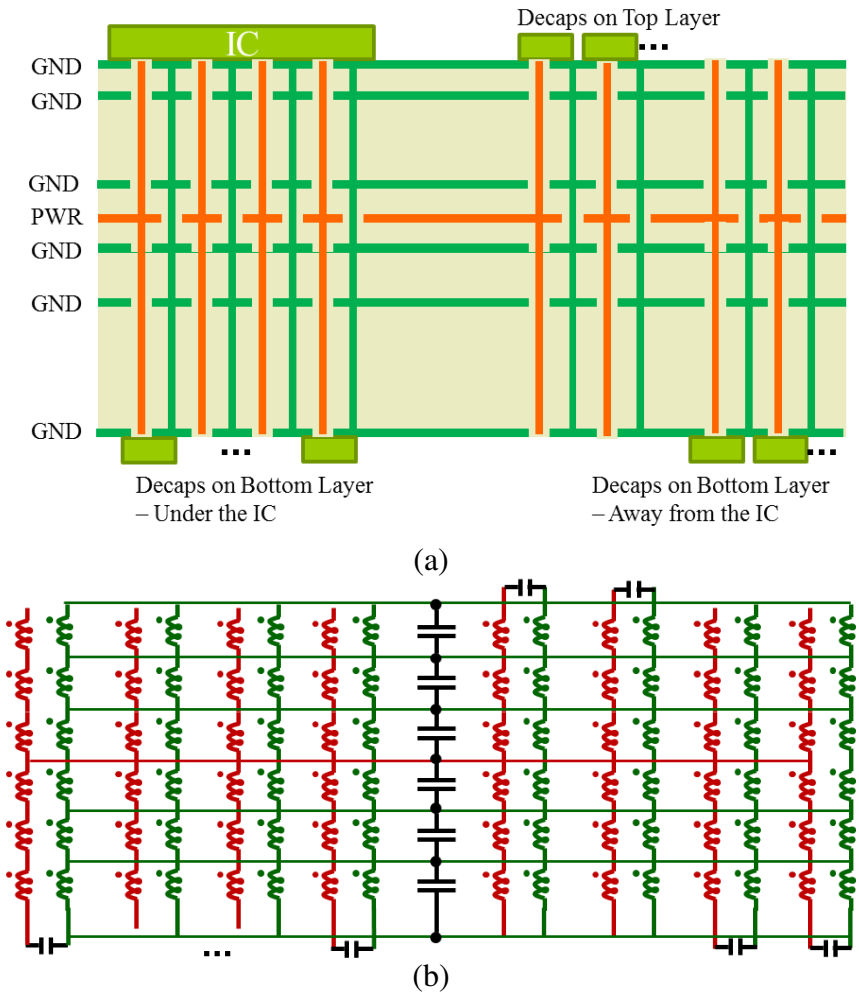


Figure 2.2. (a) A multilayer power/ground structure with multiple via connections, and, (b) its corresponding circuit model from the cavity model.

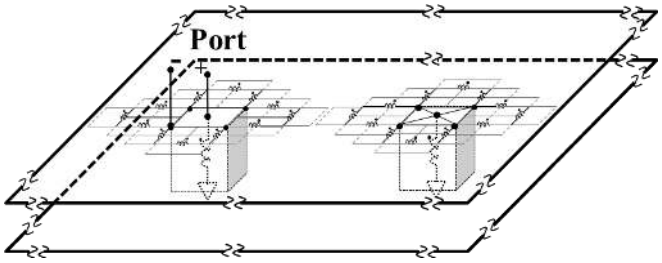


Figure 2.3. The mesh used around the vias in one cavity for the inductance calculation based on PPP.

The geometry of two vias in one cavity is modelled using parallel-plate PEEC method, and the mesh used for the inductance calculation is shown around the vias in Figure 2.3. This method can be used to develop an equivalent circuit of the entire plane, and the voltage and current can be solved using the modified nodal analysis (MNA). The inductance sub-circuit is solved separately to find the equivalent inductance for a set of power vias and a set of shorting or return vias. The basic idea of partial element equivalent circuit (PEEC) methodology proposed in [21] is to divide the geometry into numerous electrically small cells, along which the field variation is very small. In these cells, the geometry can be modelled with lumped circuits. The circuit elements in the cells need to maintain the voltage and current continuity at the nodes.

The PPP approach converts electromagnetic problems into circuit problems, which can be solved in an efficient way, while maintain the accuracy. The speed and accuracy of PPP approach were discussed in [21] and [24]. The inductance term of every cell can be represented with partial self-inductance and partial mutual inductance. The plane capacitance model in (5) is applied to calculate the capacitance of the cells.

$$C_p = \frac{\varepsilon A}{d}, \tag{5}$$

Where A is the cell area at each node, and d is the separation of the planes. The resistance of the plane is written as (6).

$$R_c = 2\frac{\Delta x}{\sigma \Delta y \delta}, \tag{6}$$

Here σ is the conductivity of the planes, Δx and Δy are the dimensions for the cell in the perpendicular direction which is parallel to the current directions. It assumes that skin-depth $\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$ is smaller than conductor thickness.

An equivalent circuit of the entire plane can be developed using the modified nodal analysis (MNA) method. By applying Kirchhoff's voltage (KVL) and current laws (KCL), the circuit equation can be written as (7).

$$\begin{pmatrix} \overline{\overline{C}} & \overline{\overline{A}} \\ \overline{\overline{A^T}} & \overline{\overline{L+R}} \end{pmatrix} \begin{pmatrix} \overline{\overline{V}} \\ \overline{I} \end{pmatrix} = \begin{pmatrix} \overline{\overline{I_s}} \\ \overline{0} \end{pmatrix}, \tag{7}$$

Where, $\overline{\overline{A}}$ is the incident matrix which stores all the connection information, $\overline{\overline{I_s}}$ is the external current source, $\overline{\overline{L}}$ is partial inductance matrix, $\overline{\overline{R}}$ is resistance matrix, and $\overline{\overline{C}}$ is capacitance matrix. The current $\overline{I}$ and voltage $\overline{\overline{V}}$ at the notes can be calculated by solving the circuit equations. Then the current density of the planes is written as (8).

$$\overline{\overline{J}} = \frac{\overline{\overline{I}}}{w}, \tag{8}$$

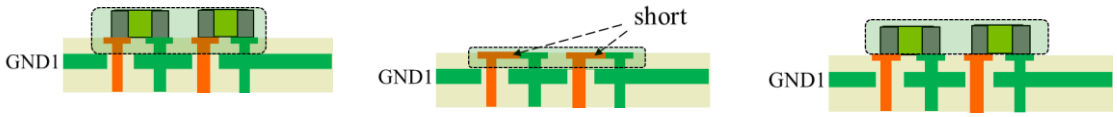
Here w is the mesh cell dimension.

2.3. PMSR FOR DECAP CONNECTION MODELING

The Physics-based Model Size Reduction (PMSR) method is used to model the decap connection from the decap to the PCB using traces, pads, and vias above the top most or bottom most power-return planes [25]-[26]. A relatively simple circuit which correlates with the geometry is reduced from the conventional PEEC model based on PMSR. Nodes are selected from the complex PEEC model to be the final nodes after the reduction according to the geometry details. The original circuit model from the PEEC between the nodes is used to extract lumped RLGC elements for PMSR. Then all reduced circuit models are assembled again based on the node connectivity matrix from the

geometry. KCL and KVL principles are applied to the reduced equivalent circuit models. Due to the efficiency and accuracy of the PEEC till relatively high frequency, the PMSR method maintains the accuracy and efficiency, while implementing the geometry influence in the calculation.

The connection from the decap to the PCB is separated into two parts. One part is the inductance from the decap pads to the ground layer of the PCB when the decaps are shorted, as shown in Figure 2.4 (b). The other one is the decap itself, as shown in Figure 2.4 (c). The inductance from the decap pad to the PCB is denoted asd L_{above}, and PMSR is applied to obtain the physics-based circuit model. For the decap itself, usually the ESL and ESR values provided by the vendors are not adequate for accurate modeling. The decap model itself can be modeled based on PEEC, as in [25].The physics based circuit model extraction process of L_{above} for the geometry with two decaps placed in pairs in can be extracted as Figure 2.5.



(a) (b) (c)

Figure 2.4. Decap connection above the PCB separation, (a) Decap connection definition, (b) Labove when the decaps are shorted, (c) Decap part in the decap conection.

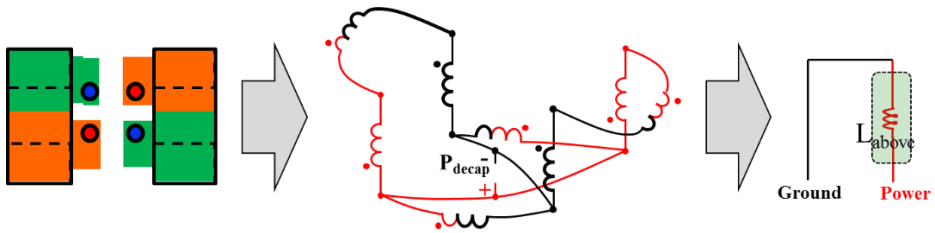


Figure 2.5. The physics-based circuit model extraction based on the PMSR.

3. PCB PDN DESIGN CRITERIA

3.1. GENERIC PCB PDN INPUT IMPEDANCE

The PDN input impedance looking from the IC has a generic trend with frequency, as different geometry structures dominate in different frequency ranges. At relatively low frequency, the PDN input impedance is dominated by the decap capacitance, and the input impedance reduces with the frequency increasing. In this frequency range, the current comes from the IC port, goes to the power net area fill, passes the power net area fill and reaches the decaps. After passing the decaps, the current goes back to the power net area fill and then to the IC power-return. The equivalent inductance of the current path is defined as L_{PCB_EQ} in the thesis. As the frequency increases, the capacitance between the power net area fill with its neighboring power-return net starts to dominate the PDN input impedance. The plane capacitance calculated from (2) for rectangular power/power-return cavity, enables the current to come directly back to the IC power-return after reaching the power net area fill. The equivalent inductance of the current path from the IC to the power net are fill and back to the IC directly without reaching the decaps is defined as IC interconnection inductance L_{PCB_IC}. At high frequencies, the L_{PCB_IC} dominates the PDN input impedance. As frequency grows even higher, the cavity resonances start, and the cavity can't model PDN performance after cavity resonance.

The equivalent inductance L_{PCB_EQ} can be segmented into different parts, the decap interconnection inductance L_{PCB_Decap} of the current path from the power net area fill to the decap and back to the power net area fill, the IC interconnection inductance L_{PCB_IC}, the power net area fill inductance L_{PCB_Plane} of the current path from IC region in the power net area fill to the decap region and back to the IC region, and the decap connection inductance L_{above} from the decap to the PCB. The segmentation is explained in details in 3.4.

3.2. TARGET INPUT IMPEDANCE DEFINITION

PCB PDN design is mostly evaluated based on the input impedance looking into the PCB from the IC. The PDN input impedance is compared with the target impedance, which is selected as the impedance profile that generates the maximum voltage ripple within tolerance [10].

The definition of target impedance is based on the switching current profile. Intuitively, the target impedance can be defined as

$$Z_{\text{target}} = \frac{V_{\text{supply}} \times Percentage_{Specified}}{I_{switching}} \tag{9}$$

In this definition, the voltage ripple and switching current both change with time. But the target impedance is frequency domain concept. To resolve the problem, the maximum values of voltage and current are used in this definition. Then the target impedance is a constant through the entire frequency range, which is resistance. However, the PDN input impedance is frequency dependent, as shown in Figure 3.1. The requirement of lowering the PDN input impedance to a constant value through the entire the frequency range can lead to over-design in practice [10].

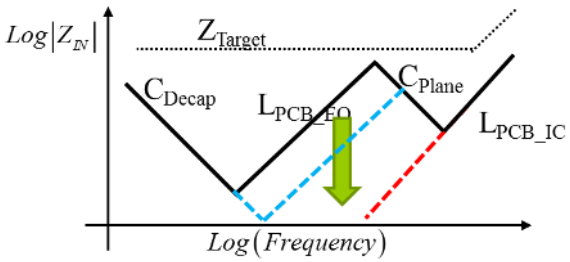


Figure 3.1. The generic PCB PDN input impedance. By adding decoupling capacitors, the mid frequency range inductance reduces.

The target impedance should be defined in a way which is related to the switching current profile in frequency domain. Usually IC has two modes, working and resting. In a PDN design, the number of ICs which switch varies with time. The switching current profile can be complex. For a simple approximation, the switching current can be modeled as the summation of triangle waves of different frequencies. The magnitudes of the frequency harmonics of the triangle waves decrease with the increase of the frequency. Then, the target impedance definition increases at higher frequencies. The target

impedance can be defined as (10), [10]. The PDN input impedance and the target impedance is shown in Figure 3.1.

$$Z(f)_{\text{target}} = R + j\omega L \tag{10}$$

3.3. SURFACE CURRENT ANALYSIS

Surface current distribution for PCB PDN is closely related to the geometry. However, the discontinuity caused by vias changes the current distribution. Surface current distribution reveals the current path and the strength of the coupling between geometry structures. The current density distribution can be calculated based on the cavity model [19] and plane-pair PEEC [24].

In the cavity, the surface current distribution on the planes can be analyzed from the field distribution. The thickness of the cavity is electric small, the electric field inside the cavity only has $\hat{z}$ component, which is listed below.

$$E_z(x,y)\Big|_{J=J_j} = j\omega\mu(\hat{J}_j \cdot \hat{z})\frac{1}{ab}\sum_m\sum_n \frac{(2-\delta_m)(2-\delta_n)}{(k_x)(k_y)} \frac{\left[\begin{array}{l}\cos(k_x x)\cos(k_y y)\cos(k_x x_j)\cdot \\ \cos(k_y y_j)\sin(\frac{k_x W_{xj}}{2})\sin(\frac{k_y W_{yj}}{2})\end{array}\right]}{k^2-[(k_x)^2+(k_y)^2]} \tag{11}$$

Magnetic field can be calculated based on the electric field using Maxwell's equation as (12), [27].

$$\begin{aligned}\vec{H} &= \frac{j}{\omega\mu}\nabla\times\vec{E} = \frac{j}{\omega\mu}\left[\left(-\frac{\partial E_z}{\partial x}\right)\hat{y}+\frac{\partial E_z}{\partial y}\hat{x}\right] \\ &= \frac{(\hat{J}_j\cdot\hat{z})}{ab}\left[\begin{array}{l} k_y\cos(k_x x)\sin(k_y y)\cos(k_x x_j)\cdot \\ \sum_m\sum_n \frac{(2-\delta_m)(2-\delta_n)}{(k_x)(k_y)}\frac{\cos(k_y y_j)\sin(\frac{k_x W_{xj}}{2})\sin(\frac{k_y W_{yj}}{2})}{k^2-[(k_x)^2+(k_y)^2]}\hat{x} - \\ k_x\sin(k_x x)\cos(k_y y)\cos(k_x x_j)\cdot \\ \sum_m\sum_n \frac{4\sigma_m^2\sigma_n^2}{(k_x)(k_y)}\frac{\cos(k_y y_j)\sin(\frac{k_x W_{xj}}{2})\sin(\frac{k_y W_{yj}}{2})}{k^2-[(k_x)^2+(k_y)^2]}\hat{y}\end{array}\right]\end{aligned} \tag{12}$$

Then, surface current density can be represented as (13), [27].

$$\vec{J}(x_i, y_i)\Big|_{J=J_j} = \frac{\hat{J}_j}{ab}\begin{bmatrix} \sum_m \sum_n \frac{(2-\delta_m)(2-\delta_n)}{(k_x)(k_y)} \frac{k_y f_1(x_i, y_i, x_j, y_j)}{k^2 - k_{mn}^2}\hat{y} + \\ \sum_m \sum_n \frac{(2-\delta_m)(2-\delta_n)}{(k_x)(k_y)} \frac{k_x f_2(x_i, y_i, x_j, y_j)}{k^2 - k_{mn}^2}\hat{x} \end{bmatrix} \tag{13}$$

Here,

$$k_x = \frac{m\pi}{a},\quad k_y = \frac{n\pi}{b},\quad k_{mn}^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2,\quad k^2 = \omega^2\mu\varepsilon \quad \text{,and}$$

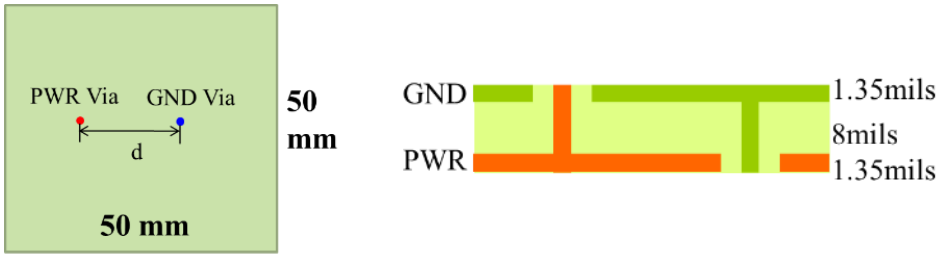
$$f_1(x_i, y_i, x_j, y_j) = \cos(k_x x)\sin(k_y y)\cos(k_x x_j) \times \cos(k_y y_j)\sin(\frac{k_x W_{xj}}{2})\sin(\frac{k_y W_{yj}}{2}), \tag{14}$$

$$f_2(x_i, y_i, x_j, y_j) = \sin(k_x x)\cos(k_y y)\cos(k_x x_j) \times \cos(k_y y_j)\sin(\frac{k_x W_{xj}}{2})\sin(\frac{k_y W_{yj}}{2}).$$

3.3.1. Test Geometry for Current Density Distribution. The physics behind the segmentation of the geometry is based on the current paths in the PCB PDN. The current distribution along the planes of the geometry gives more intuitive understanding of how the geometry influences the mutual inductance between the vias in the cavity. A single rectangular cavity formed by a power layer and a power-return layer with a power via and a shorting power-return via is used as the test geometry to illustrate the coupling mechanism in different situations [27], as shown in Figure 3.2. One of the via is defined as a port and the other via is shorted to both plates of the cavity. The comparison is designed to show how the distance of the vias influence the coupling between them. The two vias are placed close (5mm) in one case, and are placed far away (25mm) in another case. The circuit model for the geometry is shown in Figure 3.3, with the values of self and mutual inductance for the different cases. The surface current density for the cases in Figure 3.3 is shown in Figure 3.4.

To calculate the surface current density J_{ij}, the plane is meshed into many sample points. The simplest mesh is uniform mesh, but it will take large number of mesh cells to

get relative accurate results. To reduce the number of samples while maintain the accuracy, sub-mesh is used at the discontinuities where the surface current changes a lot to capture the variations. In this case, denser mesh is applied around the via regions.



(a) (b)

Figure 3.2. A plane-pair cavity with a power via and a shorting ground via placed with distance d, (a) top view of the test case, (b) stack-up of the test case. [27]

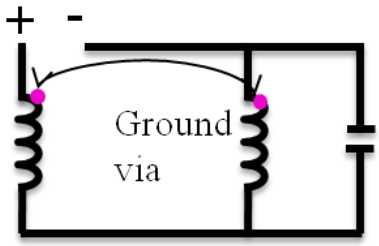
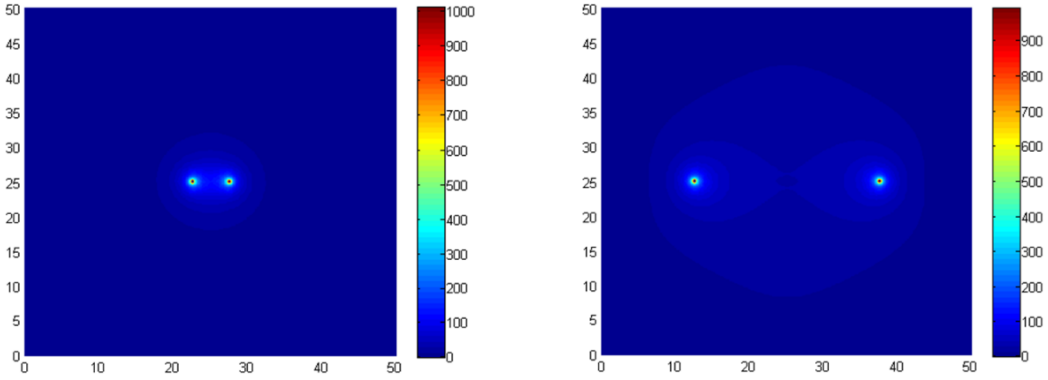


Figure 3.3. Circuit model for geometries shown in Figure 3.2.



(a) (b)

Figure 3.4. Current density plot based on the cavity model for the geometry shown in Figure 3.2 with different d values, (a) d=5mm, (b) d=25mm. [27]

The current density distributions based on the cavity model for the two cases are shown in Figure 3.4.When the two vias placed closely, the current concentrates around the vias as shown in Figure 3.4 (a). When the two vias are placed far away, the current spreads to much larger area as shown in Figure 3.4 (b).

3.3.2. Current Distribution Comparison between the Cavity Model and Plane-Pair PEEC. The surface density distribution for the case with d=25mm based on the plane-pair PEEC is calculated and compared with the result based on the cavity model as shown in Figure 3.5. The results obtained from the two methods are identical, but the magnitude contour from the plane-pair PEEC provides more details than the one from the cavity model in the outside region. For the area near the vias, the contour shapes are different for the two methods, while the magnitudes are similar.

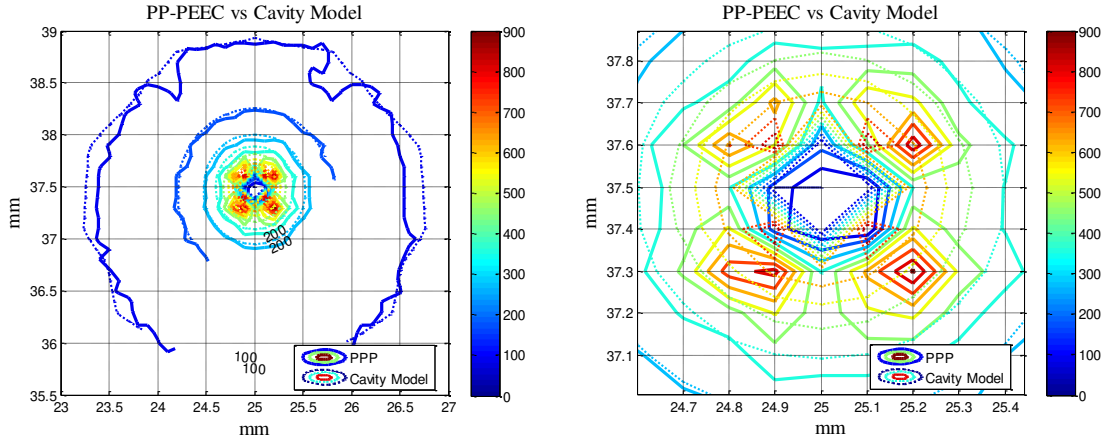


Figure 3.5. Current density comparison around the vias between cavity model and PP-PEEC for the geometry shown in Figure 3.2 for d=25mm, (a). the via region, (b).zoom-in region for the via center shown in (a). [27]

3.3.3 Current Distributions in the PCB PDN Structures. These two cases of current distribution describes the current distribution in the IC/decap interconnection region and the power net area fill part respectively. As shown in Figure 3.4, when the two vias are placed closely, the shorting via provides the return path nearby. The surface current distribution is independent from the plane shape. In the IC or decap interconnection part, the power-return vias are close to the power vias, and the current concentrates around the

area, as the return path is nearby. Also, decaps are usually places at the leftover regions after the routing during the layout process, the distance from the decap to the IC ports are relatively larger than the distance from the power vias to the power-return vias in the decaps. The mutual inductances between the power vias and power-return vias of the IC and decap regions are negligible. The assumption that there is little or no mutual coupling between LPCB_IC and LPCB_Decap holds in most cases. When the two vias are placed far away, the surface current spreads along the planes and the inductance calculation is shape dependent when the vias are placed close to the edge. In the power net area fill, the current has to cross the planes from the corresponding IC region to the corresponding decap region in the part. The current path in Figure 3.4 (b) illustrates the current distribution in the power net area fill. The current distribution is strongly dependent on the power net area fill shape. Unfortunately, in the complex PCB PDN design, the power net area fill are usually cut into pieces with many voids embedded inside. The irregular shapes and the voids in the power net area fill can increase the LPCB_Plane dramatically.

Thus in the PDN designs with power and power-return vias placed at large distance, which is comparable to the distance from the edge, the power plane shape matters [28]. If there are enough return vias placed nearby the power vias, the current path is much less dependent on the plane shape. In most PCB PDN geometry, the power area fills can be irregular shaped. If the power shape doesn't influence the current path, the calculation of the cavity model can still be applied to calculate the equivalent inductance of the current path passing the power shapes. For the cases where the power shapes influence the current path, the PPP can be applied to calculate the inductance.

When the return vias are placed closely, the current concentrates in the nearby area. The mutual inductance terms are influenced by the distance. This fact can be used to measure when to ignore or include the mutual terms between IC and decap vias. And due to the fact of the concentration of the current distribution when the vias are place closely, the decap connection inductance and the IC connection inductance path can be segmented separately, without considering the mutual inductance between them.

3.4. GEOMETRY SEGMENTATION

The two features, L_{PCB_EQ} and L_{PCB_IC} in the PCB PDN input impedance are critical to the PCB PDN design. Decaps are used in the PCB PDN design to provide enough charges and lower the PDN input impedance. It is observed that L_{PCB_IC} can be reduced by adding more decaps. For the current path of L_{PCB_EQ}, there are four inductance contribution portions which can be segmented, which are the IC interconnection inductance L_{PCB_IC}, decap interconnection inductance L_{PCB_Decap}, the inductance of the current crossing the power net area fill L_{PCB_Plane}, and the decap connection inductance from decap to the PCB L_{above}. The segmentation is based on the assumption that there is no or little coupling between each block. Under this assumption, every block can be modeled individually. The the L_{PCB_EQ} can be expressed as the summation of the four parts, as in (15). A general PDN stack-up with many decaps placed on the top layer, the bottom layer away from the IC and the bottom layer under the IC is shown in Figure 3.6. The segmentation of every part is defined in the figure.

$$L_{PCB\_EQ} = L_{PCB\_Decap} + L_{PCB\_IC} + L_{PCB\_Plane} + L_{above} \tag{15}$$

In the IC and decap regions, the power vias and ground vias are placed closely. The current concentrates and doesn't cross the power net area fill. In these regions, the mutual inductance between IC and decap regions can be ignored when the distance from the decaps to the IC is large enough.

L_{PCB_Decap} depends on the decaps to power net area fill distance, the number of decaps , the decap package pattern and placement pattern. The convergence rate of L_{PCB_Decap} is influenced by the via placement patterns, pitch distance, package size, etc.

L_{PCB_IC} depends on the IC to the power net area fill distance, the pin placement pattern, the number of the IC pins, and the pitch size of the pins. The convergence rate of L_{PCB_IC} is influenced by the via placement patterns and the pitch size.

The L_{PCB_Plane} contains decap part and IC part. Then it depends on all factors related to L_{PCB_Decap} and L_{PCB_IC}, including the number of IC pins, IC pin placement patterns, IC pitch, the number of decaps, decap placement patterns and decap pitch. It also depends on the stack-up of the power net area fill, and the distance between the IC and decaps,

Compared to L_{PCB_IC} and L_{PCB_Decap}, L_{PCB_Plane} is more complicated, since the current path in the power net area fill is complex, which will be explained later.

The relation between L_{PCB_IC} and L_{PCB_EQ} is based on current path. From experiment results, L_{PCB_EQ} will convergent to L_{PCB_IC} by adding decaps.

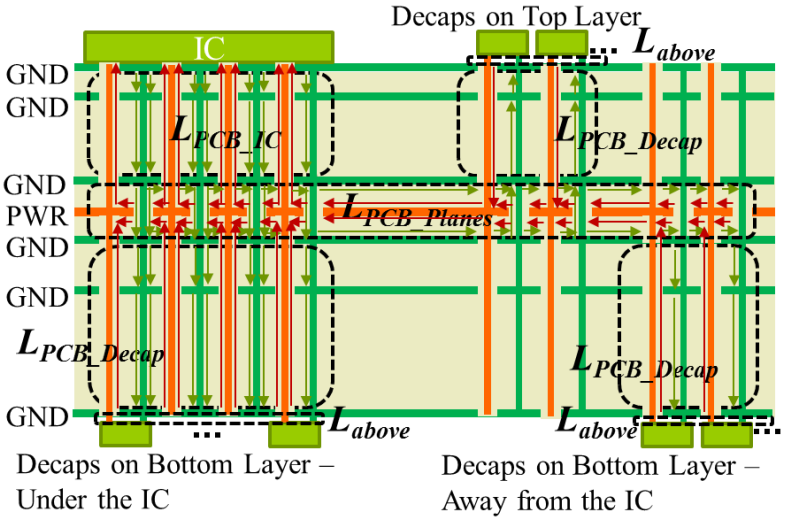


Figure 3.6. A stack-up of a high-layer count PCB PDN geometry with a power net fill and the definitions of the parts segmented from the PCB PDN geometry. [17]

3.5. EQUIVALENT INDUCTANCE AS CRITERIA

In PDN input impedance, two inductances, the equivalent inductance L_{PCB_EQ}, and the IC connection inductance L_{PCB_IC}, stand out because of different current paths [17]. Adding decaps can reduce the mid-frequency range equivalent inductance L_{PCB_EQ} to the L_{PCB_IC}. The convergence criteria of the L_{PCB_EQ} is defined as the ratio of the difference between L_{PCB_EQ} and L_{PCB_IC} to L_{PCB_IC}. From (15) L_{PCB_EQ} is the summation of L_{PCB_Decap}, L_{PCB_Plane} ,L_{PCB_IC} and L_{above}. Then the convergence criteria can be expressed as ratio of the summation of L_{PCB_Decap}, L_{PCB_Plane} and L_{above} to the L_{PCB_IC}. From the cavity model formulation in (3), the inductance contribution is proportional to the cavity thickness. An approximation of the thickness ration of the decap interconnection region, power net area fill and IC interconnection region can be used when the inductance contribution is largely influenced by the thinness. In general PCB PDN stack-up, either the distance from the decap to the power/power-return cavity h_1 or the power/power-return cavity thickness h_2 is

much larger than the other, leading to either L_{PCB_Decap} or L_{PCB_Plane} being the dominant term in L_{PCB_EQ}. In this case, the criteria can be evaluated approximatively based on the ratio of the thicknesses with acceptable precision.

4. L_{PCB_IC} CONVERGENCE

4.1. L_{PCB_IC} SEGMENTATION IN THE STACK-UP

L_{PCB_IC} is defined as the IC interconnection inductance in the PCB. The current path in the block is from the IC port to the power net area fill and back to the IC port. The principle used to extract the L_{PCB_IC} from the total equivalent inductance L_{PCB_EQ} is to maintain the current path to be the same. By applying the principle, the modeling setup to extract L_{PCB_IC} is to put the port at the IC port, and put shorts at the locations of IC vias on the nearest power-return plane in the power/power-return cavity, as shown in Figure 4.1. In this way, the current path is forced to be the same as that in the definition.

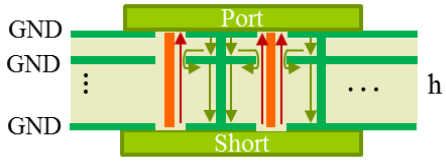


Figure 4.1. IC interconnection inductance extraction in the PCB.

4.2. IC PIN PLACEMENT PATTERNS

The ICs have lots of power and power-return pins placed with a specific pitch size in a relatively small area. The number of IC power pins and power-return pins is designed by the package or IC designers. There are several common IC pin placement patterns, and three of them, defined as row, regular, and hexagonal, as shown in Figure 4.2, are analyzed in the thesis. The hexagonal placement patterns have different configurations with the different relative locations of the power and power-return vias. The placement patterns of row, regular, and hexagonal has the ratio of power to power-return vias to be 1. The power and power-return vias are placed in alternating way to take advantage of the mutual inductance since the current directions on the power vias and power-return vias are opposite. The power vias in the rectangular placement pattern are surrounded by the power-return vias, which maximize the mutual inductance influence on the IC interconnection inductance. This pattern is seen as another reference in the comparison of L_{PCB_IC} for different placement patterns. The pitch size for the IC vias is 1mm. In the

comparison, the 1/n curve, which is the inductance by simply adding the power pins in the layout, is added to show the mutual inductance influence on the L_{PCB_IC}.

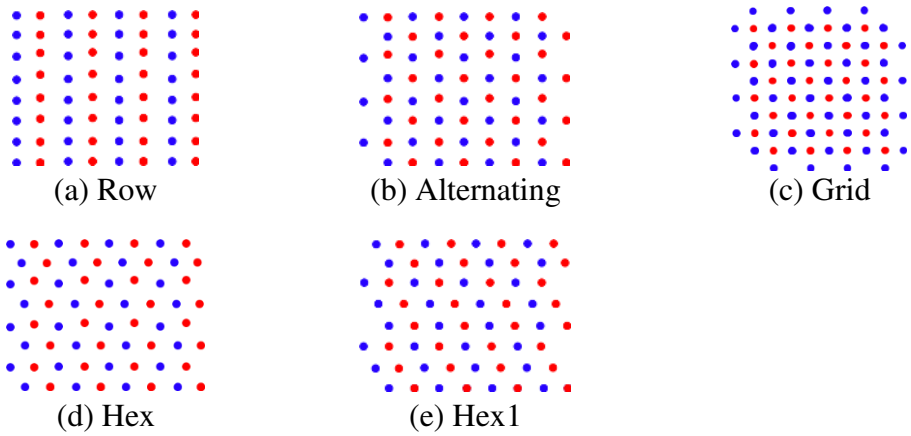


Figure 4.2. Five IC pin placement patterns with different power and power-return relative locations, (a). Row placement pattern with power and power-return vias placed in a row, (b). Regular placement pattern with power and power-return vias placed alternating, (c). Grid placement pattern with the unit cell of one power via surrounded by four power-return vias, (f). Hex placement pattern with power and power-return vias placed alternating in hexagonal pattern, (e) Hex1 placement pattern with another configuration of power and power-return vias as in (d).

4.2.1. Circuit Reduction and Rigorous L_{PCB_IC} Formulation. From the cavity model, the IC connection part can be modeled as shown in Figure 4.3. In the L_{PCB_IC} calculation, the circuit model can be simplified by combining all power vias into one power via and combining all ground vias into one ground via.

L_{PCB_IC} is simulated based on the circuit model from the cavity model for one cavity. From (3) , the inductance is proportional to the cavity thickness. Thus, L_{PCB_IC} can be scaled to different cavity thickness easily. The cavity thickness used in the model is 30 mils for the results shown in this session.

Figure 4.3 shows the methodology to find L_{PCB_IC} based on the circuit extracted from the cavity model. The power and ground vias are divided into two groups based on the assumption that the current direction is the same for all the vias in each group. Then, all power vias can be merged into one power via, and all groud vias can be merged into one ground via. The reduction is based on the voltage and current relation, as shown in (16) to (18).

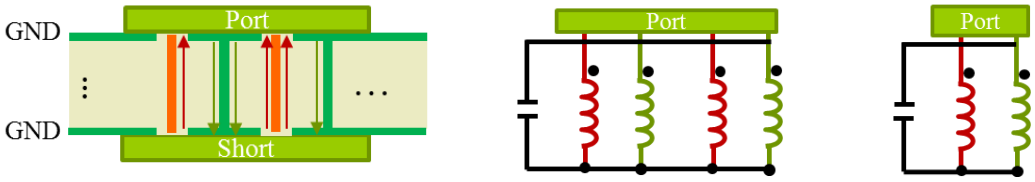


Figure 4.3. The physics-based circuit model reduction for L_{PCB_IC}.

The KVL for each group is expressed as,

$$j\omega \mathbf{L}_{Group}\mathbf{I} = \mathbf{V} \tag{16}$$

where,

$$\begin{aligned} \mathbf{I} &= \begin{bmatrix} I_1 & I_2 & \cdots & I_n \end{bmatrix}, \\ \mathbf{V} &= \begin{bmatrix} V_1 & V_2 & \cdots & V_n \end{bmatrix} \end{aligned} \tag{17}$$

$$\mathbf{L}_{Group} = \begin{bmatrix} L_{11} & L_{12} & \cdots & L_{1n} \\ L_{21} & L_{22} & \cdots & L_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ L_{n1} & L_{n2} & \cdots & L_{nn} \end{bmatrix} \tag{18}$$

I_k is the current through the k[th] IC power/power-return via in the group, and,

V_k is the voltage across the via looking from the port.

Assuming voltages across the parallel inductors are the same, then by inversing the L matrix, (16) is changed to

$$j\omega \mathbf{I} = \mathbf{L}_{Group}^{-1}\mathbf{V} \tag{19}$$

Since $V_1 = V_2 = \cdots = V_n \triangleq V_{Group}$, by adding I_i, (19) can be written as

$$j\omega L_{Group} I_{Total} = V_{Decap} \tag{20}$$

where,

$$I_{Total} = I_1 + I_2 + \cdots + I_n \tag{21}$$

Then, a relationship can be defined between effective inductance L_{Group} and the inductance matrix, as,

$$L_{Group} = \left(\sum_{columns} \sum_{rows} \left[\mathbf{L}_{Group} \right]^{-1} \right)^{-1} \tag{22}$$

Through the procedures, the power via inductors and ground via inductors are merged into one power via inductor and one ground via inductor in series. The L_{ij} matrix can be written as

$$\mathbf{L}_{PCB\_IC} = \begin{bmatrix} L_{PWR} & L_{PWR\_GND} \\ L_{PWR\_GND} & L_{PWR} \end{bmatrix} \tag{23}$$

Here L_{PWR} is the self-inductance of the one power via grouped from all power vias,
L_{GND} is the self-inductance of the one ground via grouped from all ground vias,
And L_{PWR_GND} is the mutual-inductance between the groud via and the power via.
Then L_{PCB_IC} can be calculated as

$$L_{PCB\_IC} = L_{PWR} + L_{GND} - 2L_{PWR\_GND} \tag{24}$$

4.2.2. L_{PCB_IC} Simulation Results Comparison. A single cavity with the thickness of 40 mils is used to simulate the L_{PCB_IC} for the placement patterns shown in Figure 4.2. The L_{PCB_IC} modelling results comparison is shown in linear and loglog scales in Figure 4.4. 1/n curve is calculated as the first IC pin divided by the number of IC pins, which is the trend if adding the IC pins in parallel without considering the mutual inductances between the vias. Figure 4.4 (a) shows the convergence trend of L_{PCB_IC} by adding the number of IC pins, and Figure 4.4 (b) shows the convergence rate of L_{PCB_IC}. From both

comparisons, the L_{PCB_IC} of the placement patterns shown in Figure 4.4 is very close to 1/n curve with the cavity thickness is 40mils. Since L_{PCB_IC} is proportional to the cavity thickness, resulting in the difference of L_{PCB_IC} between different placement patterns increases with the cavity thickness. But 1/n curve is a good approximation for L_{PCB_IC} with the cavity thickness in the range of 30mils.

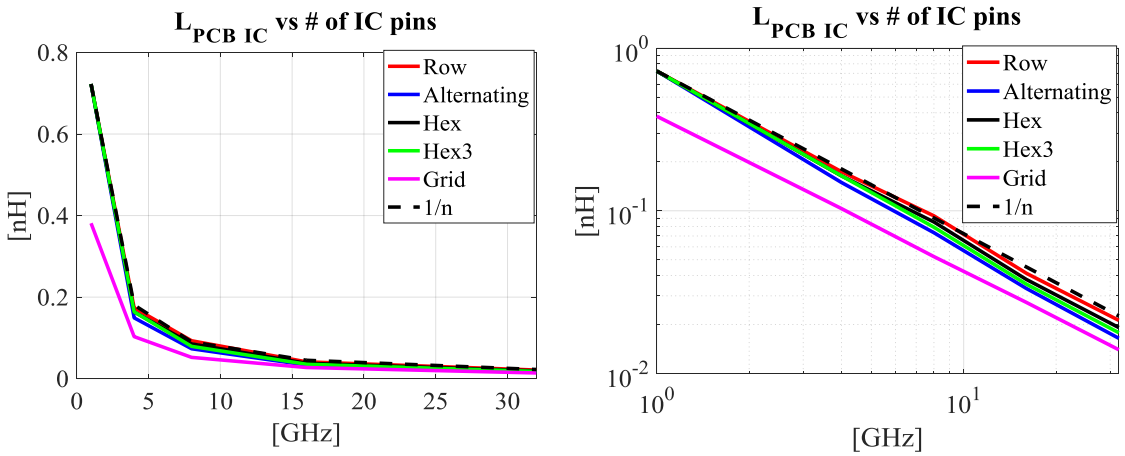


Figure 4.4. L_{PCB_IC} comparison for the IC pin placement patterns shown in Figure 4.2 .

4.3. UNIT CELL APPROACH FOR L_{PCB_IC} APPROXIMATION

Unit cell approach can be used to calculate LPCB_IC for the pattern of one power via surrounded by four power-return vias. The unit cell for the IC placement pattern shown in Figure 4.2 (c) is one power via surrounded by four ground vias. The return current for the power via mostly concentrates on the nearby power-return vias. Thus, the way to construct the L_{PCB_IC} formula of the pattern is based on adding the unit cell in parallel and using curve fitting to quantize the mutual inductance influence, as shown in(25).

$$L_{PCB\_IC\_grid} = h_1\left(\frac{L_{self\_PUL,1unitcell}}{n_{ICpin}} + L_{Mutual,unitcell\_PUL}\right) \tag{25}$$

Here, the first term of (25) can be seen as the self-inductance of the cells, and the second term is the mutual inductance between the cells.

To calculate the first pair connection inductance, KCL and KVL are applied to the unit cell of four vias. In the formulation, the voltages and currents for the four power return vias are assumed to be the same. Figure 4.5 shows the name and location of the vias in the unit cell.

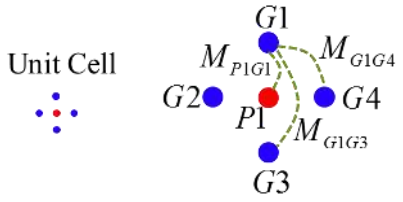


Figure 4.5. Unit cell definition in the IC pin placement pattern and the mutual inductance definitions

$$\begin{bmatrix} L_{P1} & M_{P1G1} & M_{P1G2} & M_{P1G3} & M_{P1G4} \\ M_{P1G1} & L_{G1} & M_{G1G2} & M_{G1G3} & M_{G1G4} \\ M_{P1G2} & M_{G1G2} & L_{G2} & M_{G2G3} & M_{G2G4} \\ M_{P1G3} & M_{G1G3} & M_{G2G3} & L_{G3} & M_{G3G4} \\ M_{P1G4} & M_{G1G4} & M_{G2G4} & M_{G3G4} & L_{G4} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix} \quad (26)$$

Where,

Assume $I_2 = I_3 = I_4 = -I_1 / 4, V_{IC} = V_1 - V_2,$

L_{Pi} is the self-inductance of the ith power via, i=1,

L_{Gi} is the self-inductance of the ith power-return via, i=1,2,3,4,

M_{PiGj} is the mutual-inductance of the ith power via and jth power-return via,

M_{GiGj} is the mutual-inductance of the ith power-return via and jth power-return via,

V_i and I_i are the voltage and current for the ith via,

V_{IC} is the voltage across the unit cell.

By solving the matrix, the unit cell L_{PCB_IC} is calculated as

$$L_{self\_PUL,\text{unitcell}} = L_{self,PWR} + \frac{L_{self,GND}}{4} - 2M_{PG} + \frac{M_{GG1}}{2} + \frac{M_{GG2}}{4} \tag{27}$$

Here $M_{GG1} \triangleq M_{G1G4} = M_{G1G2} = M_{G2G3} = M_{G3G4}$, and $M_{GG2} \triangleq M_{G1G3} = M_{G2G4}$.

Figure 4.6 shows the formulation of L_{PCB_IC} based on (25). The error introduced by the unit cell approach is not significant. The upper bound of L_{PCB_IC} is in the row IC pin pattern and the lower bound is in the grid IC pin pattern. During the design of IC interconnection inductance, these two cases can be used to calculate the range of L_{PCB_IC}. Since for the other cases, the 1/n curve is close to the L_{PCB_IC} calculated rigorously from the cavity model, L_{PCB_IC} can be calculated approximately using 1/n curve to calculate the number of IC pins during the design.

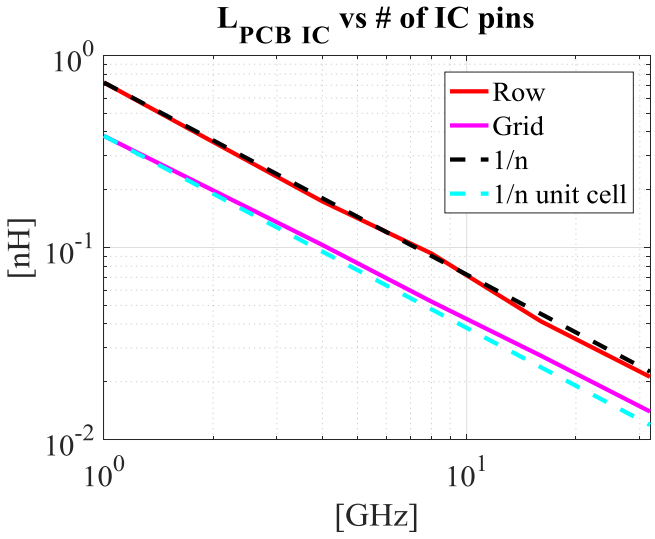


Figure 4.6. L_{PCB_IC} formulation validation shown in (25).

4.4. SELF AND MUTUAL INDUCTANCE EXTRACTION IN L_{PCB_IC}

From Figure 4.4 (b), the convergence rates of L_{PCB_IC} for different placement patterns are different, due to different mutual inductance influence. The mutual inductance influence is clearly seen in the formula(25), and (27).The inductance $L_{self,PWR} + L_{self,GND}\,/\,4$ is the self-inductance of the unit cell, and the term $-2M_{PG} + M_{GG1}\,/\,2 + M_{GG2}\,/\,4$ describes

the mutual term in each cell. The per unit height mutual inductance between each cell for L_{PCB_IC} is in the range of pH, which is very small compared with the self-inductance of all the cells.

4.5. MEASUREMENT FOR L_{PCB_IC} CONVERGENCE

CST models can be used to validate the L_{PCB_IC} calculation from the cavity model. Two ports measurement can be used to eliminate the series inductance from the port. Two fixtures are designed in Figure 4.7 to account for the same voltage assumptions on the IC pins with the principle of maintaining the same current path. The comparison of L_{PCB_IC} from the cavity model, the formulas, and full-wave simulation CST is shown in Figure 4.8. The comparison shows good agreement with each other.

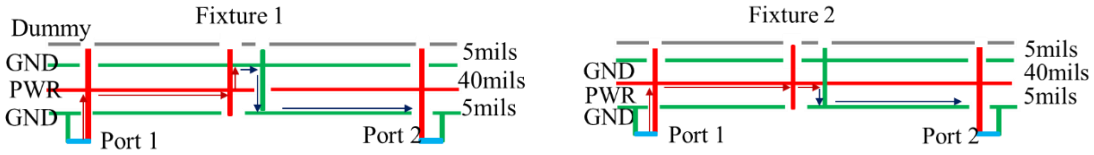


Figure 4.7. Stack up details of the test cases with IC pins added incrementally in the center.

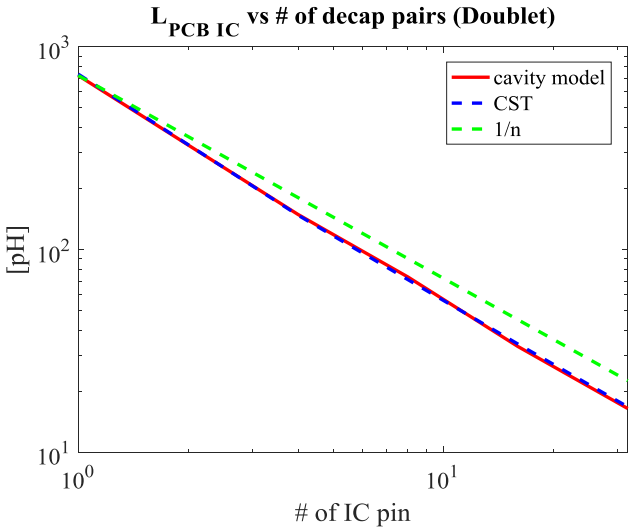


Figure 4.8. L_{PCB_IC} results comparison from the cavity model, the formulas, and CST for alternating placement pattern.

5. L_{PCB_Decap} CONVERGENCE

5.1. L_{PCB_Decap} DEFINITION

A generate multi-layered PCB PDN stack-up with many decaps placed on the top layer, the bottom layer away from the IC and the bottom layer under the IC by sharing IC power and return vias is shown in Figure 3.6. Decaps are connected to the power net area fill through vias, pads and planes. The equivalent inductance along the current path from the power net area fill to the decaps and back to the power net area fill is defined as decap connection inductance L_{PCB_Decap}. In the frequency where the series decap interconnection inductance dominates, adding decaps can reduce L_{PCB_Decap} and converge to a certain value.

The decap connection inductance L_{PCB_Decap} is found by setting the ports at the corresponding locations of the decaps in the power net area fill and the shorts at the decap locations. In this way, the current goes from the power net area fill, passes the decaps and comes back to the power net area fill. The power vias of the decap carry the current in one direction and the return vias carry the current in the opposite direction, with the total forward and return current being the same. By assuming the same potential difference across the vias with current in the same direction, the decap connection inductance L_{PCB_Decap} can be extracted from the circuit model. This approach has been validated in [8],[9] and [5].

L_{PCB_Decap} depends on the decap to power net area fill distance, the decap placement patterns, the number of decaps, and the decap package patterns. The convergence rate of L_{PCB_Decap} is influenced by the via locations in the decap package patterns, pitch distance, package size, etc. Every parameter leaves its own footprint in the L_{PCB_Decap} calculation.

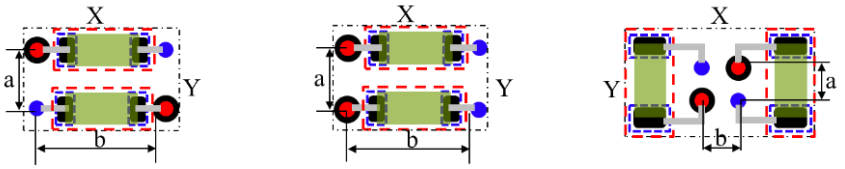
5.2. DECAP CONNECTION INDUCTANCE CONVERGENCE CRITERIA

The decap connection inductance L_{PCB_Decap} convergence rate is influenced by the mutual inductance between the vias and it depends on how the mutual inductance contributes the calculation. To quantify the mutual inductance of the vias, a reference case is used by simply adding decaps in parallel without considering the mutual inductance, referred as 1/n in the thesis. The decap connection inductance of the reference case is calculated as the decap connection inductance of one decap divided by the number of

decaps. The L_{PCB_Decap} convergence rate is defined by comparing to the reference convergence rate.

5.3. DECOUPLING CAPACITOR PLACEMENT PATTERNS

To analysis the convergence of L_{PCB_Decap}, several decap package placement patterns, as shown in Figure 5.1 are introduced to observe the trends in L_{PCB_Decap}.



(a) (b) (c)

Figure 5.1. Three decoupling capacitor placement patterns used in the thesis, (a) Alternating placement patterns with the neighbour vias of the decap placed in different directions; (b) Aligned placement patterns with the neighbour vias of the decap placed in different directions; (c)Doublet placement patterns with vias placed as close as possible in alternating directions.

In Figure 5.1, three decap placement patterns, denoted as alternating, aligned and doublet, are used in the thesis. The difference of these patterns are the relative positions of the power vias and ground vias. Alternating placement pattern has the power and ground vias placed in an alternating pattern for the neighbor decaps. Aligned placement pattern has the power and ground vias placed in the same direction for the neighbor decaps. The doublet layout has two decaps placed in the pair with the power and ground vias placed in the alternating directions at the minimum distance. The doublet is similar to the alternating layout, but the vias are placed as close as possible.

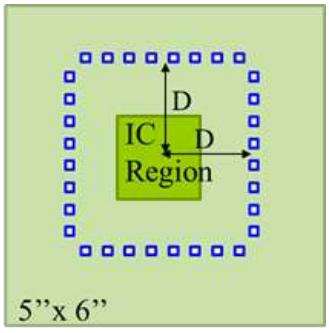
To check the convergence rate of the three patterns, decaps are placed in pairs in a line with the distance D around the IC region, as shown Figure 5.2. In layout design process, it is difficult to use the space close to the IC edge for decaps as it would limit the signal routing region around the IC, which forces the designer to place the decaps away from the IC. The relative via locations change with the decap package patterns and decap sizes. Table 5.1 shows the details of the relative via locations and package sizes of one

decap pair for different decap package layouts and sizes based on the manufacture limitations.

Table 5.1. Relative via locations and package size ([mils]) of the three decoupling capacitor placement patterns

Placement pattern	Size	a	b	X	Y
Alternating/Aligned	0201	45	120	159	85
	0402	53	136	175	101
	0603	88	207	246	171
	0805	108	223	262	211
Doublet	0201	32	32	149	71
	0402			165	87
	0603			235	158
	0805			275	174

For doublet layout, the relative positions of vias in the package are the same, since the vias are placed as close as possible, and the relative via locations are decided by the pad-stack and manufactory limitation. From the table, the doublet layout does not have to increase the decap package sizes, but two decaps always have be placed together, which limits the flexibility of layout. Doublet layout has a block of keep-out region of the four vias placed together in the center of the decap package, under the assumption that the only block area in the layout of the PCB is caused by the vias.



represents one decap pair placed in the patterns shown in (a) and (b)

Figure 5.2. The decap pair locations with decaps placed in a line with the distance D to the IC region used in the alternating, aligned and doublet placement patterns.

5.4. L_{PCB_Decap} FORMULATION

The decap connection inductance is extracted from the physics-based circuit model based on the cavity model. The cavity thickness used in the model is 40 mils for the results shown in this session, but the results are scalable to cavity thickness as the cavity model formulation shows that the inductance values are proportional to the height of the cavity.

The current distributions for the three decap package patterns are different between the neighbor vias, which results in the different convergence rate with the number of decaps. Based on the voltage and current relationship between the decap connection vias, a simplification methodology is applied to find the L_{PCB_Decap} for each pattern. The power and ground vias are divided into groups by assuming the current direction to be the same for each group. Thus, all the power vias of the decap are in one group, and all the ground vias are in the other group.

Figure 5.3 shows the stack up and port settings used to segment L_{PCB_Decap} from multi-layer stack up, based on the principle of maintaining the current path to be the same as the whole PCB PDN stack-up. In the stack-up shown in Figure 5.3, two decaps are placed on the top layer. For the decaps placed on the bottom layer, the similar stack-up can also be used to segment decap connection inductance by switching the decap and port locations shown in Figure 5.3. Figure 5.4 (b) shows the one-to-one corresponding circuit model based on the cavity model.

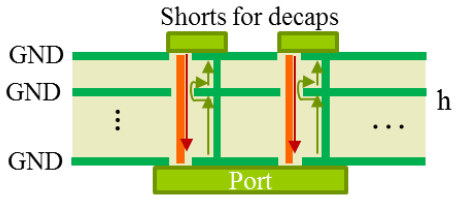


Figure 5.3. The stack-up settings to extract decap interconnection inductance L_{PCB_Decap}.

Multiple steps of circuit reduction are applied to the circuit model shown in Figure 5.4 (b). The stack-up with many power-return layers is simplified into three layers with two cavities. It can be shown that the number of power-return layers in the decap connection block doesn't influence the LP_{CB_Decap} calculation. L_{PCB_Decap} is related to the dielectric thickness from the topmost power-return layer to the nearest power-return layer

in the power net area fill. The first step is to combine the inductors of the top cavity and bottom cavity. From the cavity formulation (3), the inductance is proportional to the height of the cavity. The inductors for the top cavity and bottom cavity are independent due to the boundary conditions. To combine the inductors for the top cavity and bottom cavity for the same via, the inductance can be easily scale to the summation of the two cavity heights, which is the summation of the inductances of the top and bottom cavities in the case. This procedure is denoted as series reduction. After the series reduction, the circuit shown in Figure 5.4 (b) is changed to the circuit model shown in Figure 5.4 (d) and the geometry shown in Figure 5.4 (a) is changed to Figure 5.4 (c), which indicates that the decap connection inductance is related to the total distance from the decap to the power cavity ground layer, regardless of the number of ground layers in between. The next step is to combine the parallel inductors together. The current path in the power and power-return vias are opposite, and they can be grouped separately.

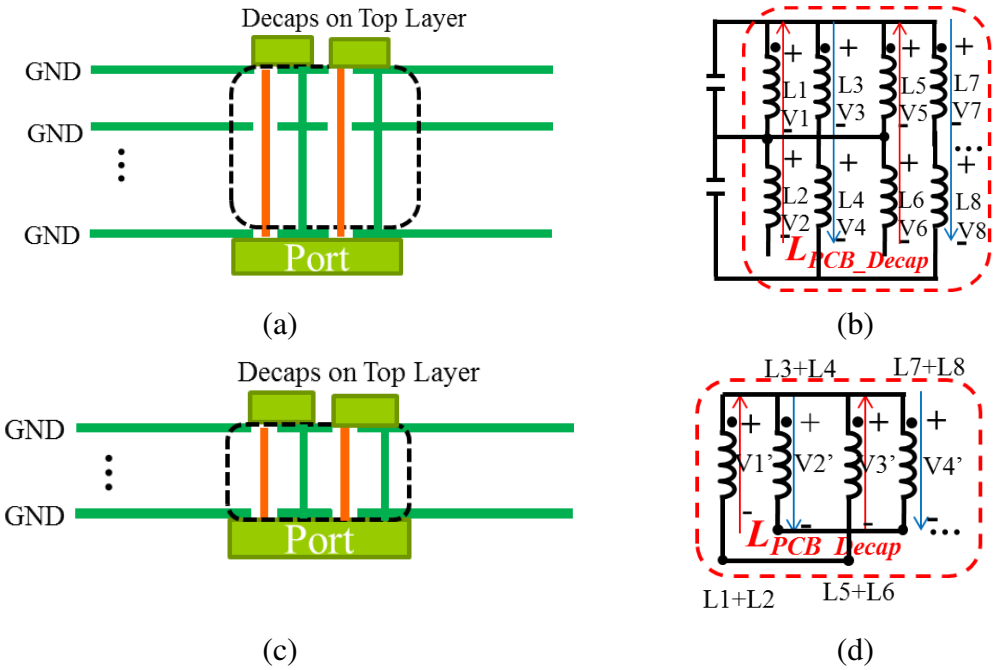


Figure 5.4. Physics-based circuit model reduction for the L_{PCB_Decap} calculation based on the cavity model, (a) L_{PCB_Decap} stack-up extracted from the high layered stack-up shown in Fig, (b) one-to-one corresponding circuit model for (a), (c) the stack-up after the series reduction applied to the geometry in (a), (d) one-to-one corresponding circuit model for the geometry in (c).

From the L_{PCB_IC} convergence session, the inductance of the one inductor after grouping can be written as

$$L_{Group} = \left(\sum_{columns} \sum_{rows} \left[\mathbf{L}_{Group} \right]^{-1} \right)^{-1} \tag{28}$$

Then the power via inductors and ground via inductors are merged into one power via inductor and one ground via inductor in series. The L_{ij} matrix can be written as

$$\mathbf{L}_{PCB\_Decap} = \begin{bmatrix} L_{PWR} & L_{PWR\_GND} \\ L_{PWR\_GND} & L_{PWR} \end{bmatrix} \tag{29}$$

Here L_{PWR} is the self-inductance of the one power via grouped from all power vias,
L_{GND} is the self-inductance of the one ground via grouped from all ground vias,
And L_{PWR_GND} is the mutual-inductance between the grouped power via and the power-return via.
Then L_{PCB_Decap} can be calculated as

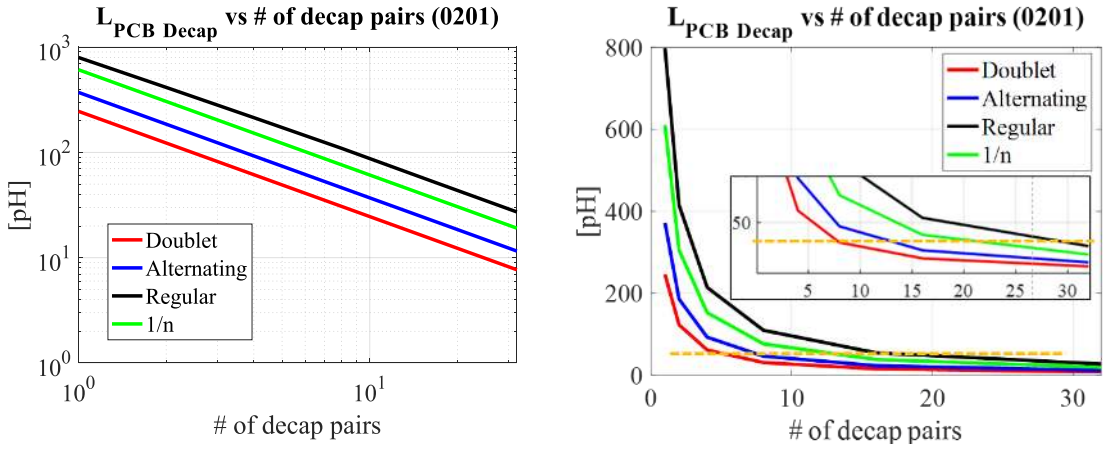
$$L_{PCB\_Decap} = L_{PWR} + L_{GND} - 2L_{PWR\_GND} \tag{30}$$

5.5. L_{PCB_Decap} MODELING RESULTS COMPARISON FOR DIFFERENT DECAP LAYOUTS

A single cavity with the thickness of 40 mils is used to calculate the L_{PCB_Decap} for the three decap package patterns shown in Figure 5.1.The comparison between the three decap package patterns of the L_{PCB_Decap} convergence with the number of decaps (twice of the number of decap pairs) is shown in Figure 5.5. Both linear and loglog plots are shown, as linear plot shows clearly the convergence of L_{PCB_Decap} as the number of decap increases, and the loglog scale reveals the convergence rate for each decap placement pattern of the decap size 0201.

In Figure 5.5, 1/n curve is the L_{PCB_Decap} calculated based on simply adding decaps in parallel without considering their mutual inductances between them. From the L_{PCB_Decap}

trend with the number of decaps is a straight line in loglog plot for all placement patterns, and doublet layout shows the fastest L_{PCB_Decap} convergence rate compared with other layouts. Another thing to notice in Figure 5.5 is to reach the same L_{PCB_Decap} value marked as dash line, regular layout requires over 50 decaps while doublet layout only needs 16 decaps. Doublet layout the can reduce the number of decaps needed dramatically to reach the same convergence requirement of the decap connection inductance.



(a) (b)

Figure 5.5. L_{PCB_Decap} change vs the number of decaps. By adding more decaps, the L_{PCB_Decap} reduces and converges to one number, (a) The convergence rate of L_{PCB_Decap} is a straight line in loglog scale plot, (b) The convergence of L_{PCB_Decap} is clearly shown in linear scale plot.

5.6. L_{PCB_Decap} FORMULATION FOR THE THREE PLACEMENT PATTERNS

Decaps are placed in pairs for the three placement patterns used in the paper, and doublet layout is the placement pattern with the power and power-return vias of the two decaps placed as close as possible in alternating directions. From the cavity model formulation, the mutual inductance between two vias is related to the distance between them. The mutual inductance decreases as the distance increases. For doublet layout, the distance between two packages is much larger than the four power and ground vias inside the package. In this case, the mutual inductance between the four alternating placed vias dominants the L_{PCB_Decap} calculation, and the mutual inductances between the packages are negligible. Thus, adding the doublet layout package can be treated simply adding the packages in parallel without the need to consider the mutual inductances between different

pairs. Then the L_{PCB_Decap} can be simply calculated as the decap connection inductance of the first pair of doublet layout divided by the number of pairs as (31).

$$L_{PCB\_Decap} = \frac{L_{PCB\_Decap\_PUL}\big|_{npair=1}}{n_{(decap\ pair)}} \times h \tag{31}$$

Here, the distance from the decap to the power cavity h_1 is used to scale the L_{PCB_Decap}, and the unit inductance of the first decap pair is provided in the paper for different decap sizes so that application of the formula is more convenient for more general use.

To calculate the first pair decap connection inductance, KCL and KVL are applied to the unit cell of four vias, as shown in Figure 5.6. In the formula, the voltages and currents for the two power /power return vias are assumed to the same respectively.

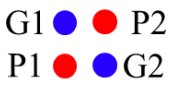


Figure 5.6. The definition of the vias in one pair decoupling capacitors placement patterns.

Figure 5.6 shows the definition of the via names in the decap pair. Based on the via names, the voltage and current relationship can be expressed in (32).

$$\begin{bmatrix} L_{P1} & M_{P1G1} & M_{P1P2} & M_{P1G2} \\ M_{P1G1} & L_{G1} & M_{P2G1} & M_{G1G2} \\ M_{P1P2} & M_{P2G1} & L_{P2} & M_{P2G2} \\ M_{P1G2} & M_{G1G2} & M_{P2G2} & L_{G2} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_1 \\ V_2 \end{bmatrix} \tag{32}$$

Where,

$I_2 = -I_1$, I_1 and I_2 are the currents of the one power via and one power-return via, respectively.

$V_{Decap} = V_1 - V_2$, V_1 and V_2 are the voltages of power and power-return vias, respectively.

V_{Decap} V_{Decap} is the voltage across the unit cell, between the power and power-return vias.

L_{Pi} is the self-inductance of the i[th] power via, i=1,2,

L_{Gi} is the self-inductance of the i[th] power-return via,

M_{PiPj} is the mutual-inductance of the i[th] power via and j[th] power via,

M_{PiGj} is the mutual-inductance of the i[th] power via and j[th] power-return via,

Then L_{PCB_Decap} can be calculated as $L_{PCB\_Decap} = \frac{V_{Decap}}{2I_1}$.

By solving the matrix, L_{PCB_Decap} for one decap pair is calculated as

$$L_{PCB\_Decap\_PUL}\big|_{n_{(decap\ pair)}=1} = \frac{1}{2}(L_P + L_G - 2M_{PG} + M_{P1P2} + M_{G1G2} - M_{P1G2} - M_{P2G1}) \quad (33)$$

Every inductance term shown in the formula is calculated based on the summation of different modes in cavity model as shown in (3). Here the self-inductance of each via, the mutual inductance between the power via and power-return via in the same pair, are assumed to be the same.

The formulation for doublet layout is based on the assumption that the distance between the vias in the different decap packages is larger than the distance between the vias in the same pair, so that the mutual inductances between the vias in different packages can be ignored. The formulation can be applied to any case with decaps placed in pairs with the distance between each pair is large enough so the assumption is valid. For the cases used in the paper, the decap pairs are placed randomly and the nearest neighbor pair is far away enough, thus, the formulation for the doublet layout can be applied to the other two placement patterns. The validation of the formula (31) is shown in Figure 5.7. The dashed lines are the L_{PCB_Decap} calculated with the L_{PCB_Decap} of the one pair divided by the number of pairs with the assumption that the mutual inductances between the packages are negligible, and the solid lines are the L_{PCB_Decap} calculated rigorously based on the cavity model. The agreement of the two sets of L_{PCB_Decap} shows that the mutual inductances

between the packages can be neglected. The first decap inductance of the three layouts used in this paper for decap size 0805 with h_1=10mils is listed in Table 5.2.

Table 5.2. The L_{PCB_Decap} of one decap pair for the three 0201 decap packages

Decap 0201	Aligned	Alternating	Doublet
$L_{PCB\_Decap}\|_{nDecapPair=1}$	798pH	372pH	246pH

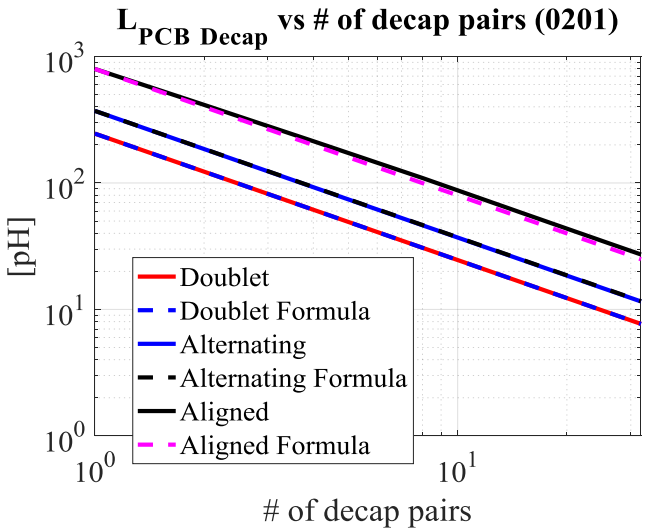


Figure 5.7. Formulation validation for three decap placement patterns shown in Figure 5.1.

5.7. MUTUAL INDUCTANCE INFLUENCE IN L_{PCB_Decap}

From (33), the convergence rates of L_{PCB_Decap} for different placement patterns are different, due to different mutual inductance influence. The mutual inductance influence is clearly seen in the formula (33). The inductance $L_P + L_G - 2M_{PG}$ is the inductance of one power via with the power-return via in the same decap, which is the same for every decap in the same layout. The term $M_{P1P2} + M_{G1G2} - M_{P1G2} - M_{P2G1}$ describes how the mutual inductance between the vias of the two decaps in one pair contributes to the L_{PCB_Decap} calculation. Here, the mutual inductances with the same current flow are added to the total inductance, while the mutual inductances with the opposite current directions are subtracted from the total inductance. Considering the mutual inductance decreases with the increase of the distance between two vias, for the alternating and doublet placement

patterns, the distance between the power via P1(G1) and the power-return via G2(P2) is closer than the distance of power vias P1 and P2, or G1 and G2, leading to the mutual inductances M_{P1G2} and M_{P2G1} larger than M_{P1P2} and M_{G1G2}. The mutual term between the two decap vias $M_{P1P2} + M_{G1G2} - M_{P1G2} - M_{P2G1}$ in (33) is negative. Similarly, for the regular placement pattern, the mutual inductance term in (33) is positive, leading to larger inductance. Since the distance between the power and power-return vias in the doublet layout is the smallest, the M_{PG} is the largest and it helps to lower L_{PCB_Decap}. The inductance terms for the placement patterns shown in Figure 5.1 are listed in Table 5.3.

Table 5.3. The self and mutual inductances in the one decap pair for the three decap packages in size 0201

	Aligned	Alternating	Doublet
$L_P + L_G$	2435	2413	2428
M_{P1P2} / M_{G1G2}	821	619	831
M_{P1G2} / M_{P2G1}	619	821	898
M_{PG}	633	633	901
$M_{P1P2} + M_{G1G2} - M_{P1G2} - M_{P2G1}$	404	-404	-135

5.8. L_{PCB_Decap} DESIGN CURVES AND DESIGN PROCEDURES

5.8.1. L_{PCB_Decap} Design Library. For the decap package patterns mentioned in the paper, the L_{PCB_Decap} convergence with the number of decaps can be analytically calculated. Table 5.4 lists the L_{PCB_Decap} per of one decap pair, so that during the design procedure, the designers can just look up the table, calculate the L_{PCB_Decap} convergence with the number of decaps and get a relatively good approximation about the decap layout in PCB PDN design.

Table 5.4. The L_{PCB_Decap} [pH] per mil of one decap pair for the three decap packages of different sizes

$L_{PCB\_Decap\_PUL}\|_{n(Decap)=1}$	Aligned	Alternating	Doublet
0201	20	9.3	6.1
0402	20.4	10.1	6.1
0603	22.2	12.6	6.1
0805	22	13.5	6.1

5.8.2. Procedures to Design the L_{PCB_Decap} Convergence. In PCB PDN geometry, decaps can be placed on the top layer, on the bottom layer away from the IC, and on the bottom layer under the IC sharing the IC vias. From the formulation, L_{PCB_Decap} is proportional to the distance from the decap to the power cavity. Placing the decaps close to the nearest power net area file can reduce L_{PCB_Decap} proportionally.

A recommended procedure to use this approach is to firstly decide the stack-up of the PCB PDN geometry either based on the other requirements of the design or the decap locations. Then, the decaps can be put on the nearest possible layer. Then, the possible decap package pattern with the fastest convergence rate can be chosen and the number of decaps can be calculated or estimated based on the design curves and formulas. For other decap placement patterns, the L_{PCB_Decap} can be simulated rigorously using (28) to (30), and the convergence rate can be obtained to guide the design.

5.9. VALIDATION OF L_{PCB_Decap} CONVERGENCE

A test case set is designed to validate the L_{PCB_Decap} convergence design methodology. As many decaps are scattered, it is impossible to assign the same port on all decap locations. A measurement set is designed to measure the L_{PCB_Ddecap} with the decaps increasing in pairs incrementally. The design is based on maintaining the same current path. In the measurement set, there are two fixtures, as shown in Figure 5.8. In fixture 1, the power vias are shorted to the topmost ground layer. While in fixture 2, the power vias are open. The current path difference between is from the power layer to the topmost ground layer, passing the short locations and back to the power layer, which is the same as the current path in the decap connection block.

To get the L_{PCB_Decap} part from the measurement, two ports measurement is used. From the definition of Z_{21}, the measurement contains the L_{PCB_Decap} information regardless of the equivalent inductance from the port to the power layer and back to the port. The physics based circuit model is shown in Figure 5.9 for both cases. The plane partial inductance and via partial inductance are segmented in the physics-based circuit model. Based on the Z_{21} measurement, the inductance of L3, L4 and L5 are measured in fixture 1. And the inductance L5 is measured in fixture 2. The inductance calculated from fixture 1

minus the inductance calculated from fixture 2 is equivalent inductance of the same current path as in the decap connection block.

Three design sets are built for the three decap placement patterns discussed in the paper. Decaps are placed in a line around the IC region with 1'' distance on the board. For each test board, it has 32 unit cells of vias for 32 pairs of decaps. Since only the decap connection inductance is considered in the paper, decaps are represented as short during measurement. The corresponding vias are shorted gradually based on the number of decaps added on the board. The results are shown in Figure 5.10.

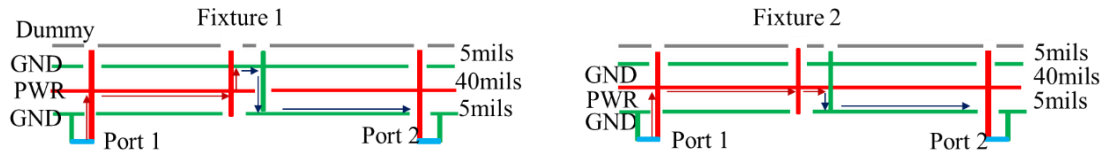
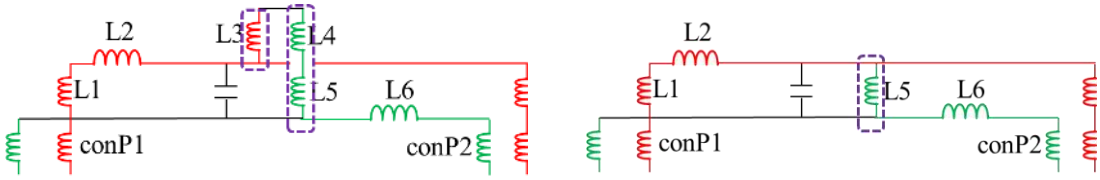


Figure 5.8. Stack up details of the test cases with decoupling capacitors added in pairs incrementally.



(a) (b)

Figure 5.9. Physics-based circuit model for the fixture 1 (a) and fixture 2 (b) of the measurement test cases.

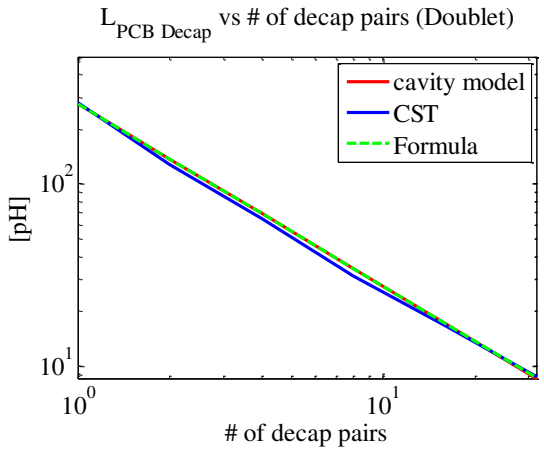


Figure 5.10. The comparison of L_{PCB_Decap} from cavity model, formulas, CST and measurement for doublet layout of size 0402.

CST models are built based on the Z21 measurement to extract L_{PCB_Decap}. Doublet layout is used to validate the calculation of L_{PCB_Decap} from the cavity model with the full-wave simulation results from CST. The comparison of CST with the extraction from the cavity model and the formula is shown in Figure 5.10.

6. L_{PCB_Plane} CONVERGENCE

6.1. L_{PCB_plane} EXTRACTION BASED ON THE CAVITY MODEL

L_{PCB_Plane} is the equivalent inductance of the current path in the power net area fill from the IC part to the decap part and back to the IC part. From [28], the current distribution of the power net area fill is high dependent on the area fill, as the distance from the IC to the decap is large due to the practice that decaps are usually placed at the leftover region after routing. For complex designs, the power net area fill are usually irregular with many voids inside. These structures have a dramatic influence increase on the current path, resulting in large increase in the L_{PCB_Plane}. The L_{PCB_Plane} can be modelled based on two methods, the cavity model, when the power net area fill shape is rectangular or the power net are fill shape has little influence on the current path from the IC part to the decap part, and PPP, when the power net area fill is irregular shaped with voids inside. The physics based circuit model can be extracted based on the two methods separately. But the analysis of the pre-layout methodology of this part shares the same approach. The design approach is illustrated based on the cavity model in this session, and a brief description about how to apply PPP to complete the methodology is explained in the end.

To extract the L_{PCB_Plane} from the multi-layer PCB PDN geometry, the port is set to be the corresponding IC locations in the power net area fill, the and corresponding decap location in the power net area fill is set to be short. Depending the locations of the decaps, the short locations have three cases, as shown in Figure 6.1. The current paths for the three cases are different. For the decaps placed on the top layer, after the current reached the corresponding decap locations in the power net area fill, the current goes up to reach the decaps and comes back. The dominant current path for this case is in the top cavity. As for the decaps placed on the bottom layer away from the IC, the situation is similar as when the decaps are placed on the top layer, with the dominant cavity to be the bottom cavity. For the decap placed on the bottom layer under the IC, the current does not have to cross the power net area fill to reach the decaps. The current comes from the IC to the decaps through the vias and goes back to the IC. The current path for this case is the same as the that in the L_{PCB_IC} and L_{PCB_Decap} parts, and can be analyzed similarly.

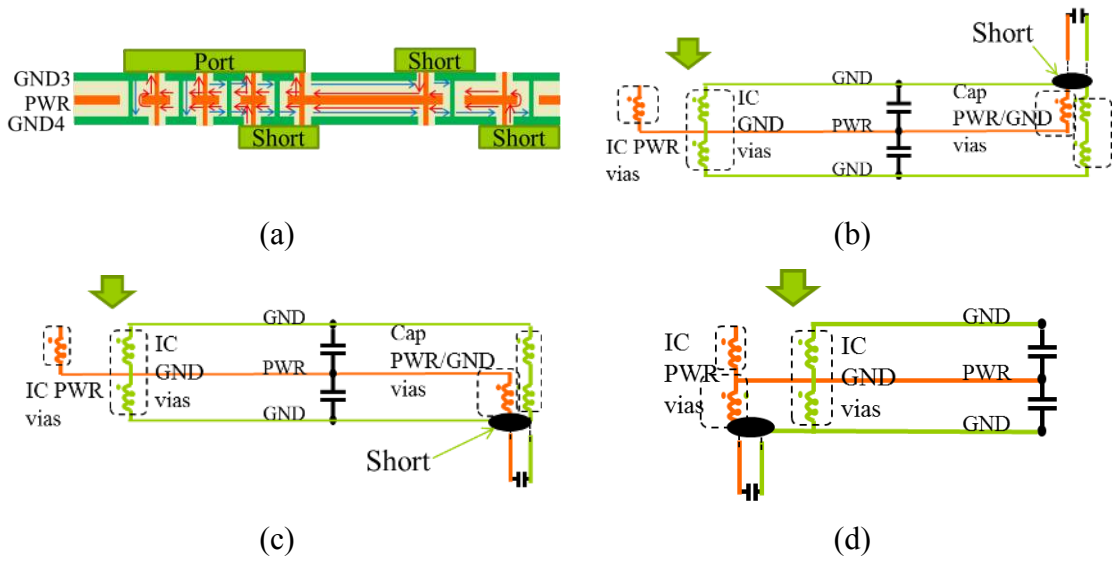
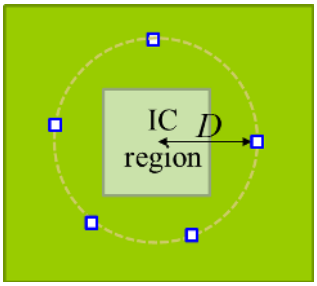


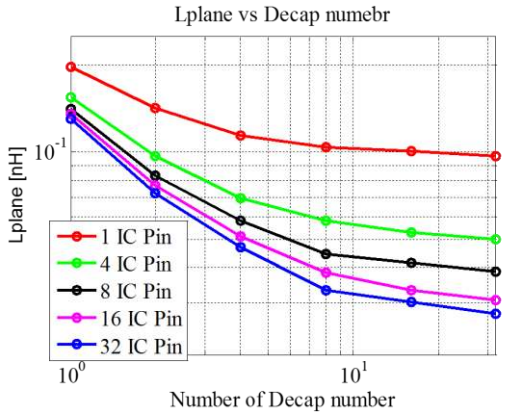
Figure 6.1. L_{PCB_Plane} (a) stack-up extraction, current path, and equivalent circuit model from the cavity model for decap placed (b) on the top layer, (c) on the bottom layer away from the IC, (d) on the bottom layer under the IC.

L_{PCB_Plane} depends on the IC and decap details, decap locations, decap to the IC distance, the stack-up, power net area shape, and voids. Decaps are placed as a circle at distance D around the IC region for more clear D definition, as shown in Figure 6.2. The L_{PCB_Plane} results from the cavity model are shown in Figure 6.3. From Figure 6.3 (a), L_{PCB_Plane} decreases with the number of decaps and the number of IC pins. From Figure 6.3 (b), L_{PCB_Plane} depends on the decap locations, due to different current paths in the power net area fill for different decap locations. In Figure 6.3 (b), since the thicknesses for the top and bottom cavities are the same, the L_{PCB_Plane} results when the decaps are placed on the top and on the bottom away from the IC are the same. For the case when decaps are placed on the bottom layer under the IC, the L_{PCB_Plane} can be analyzed the same as L_{PCB_IC}, and it depends on the distance from the IC port to the decap locations directly. When this distance is large, even though the current does not have to cross the power net area fill, the L_{PCB_Plane} can be larger than the other two cases. Figure 6.3 (c) shows the L_{PCB_Plane} increases with the distance from the IC to the decaps, as the current path is longer when the decap to IC distance is larger, for the cases when decaps placed on the top layer and on the bottom layer away from the IC.

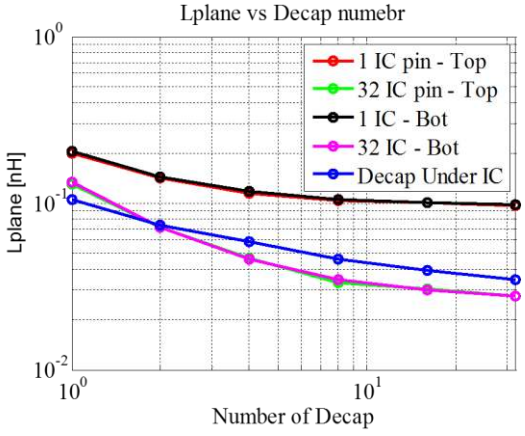


represents one decap pair placed in the patterns shown in Figure 5.1

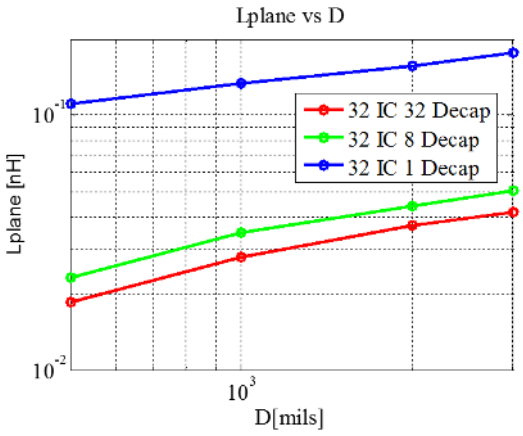
Figure 6.2. The top view of the decap and IC locations for the L_{PCB_Plane} analysis, (a) decap pairs are placed in a circle with the distance D to the IC region, (b) decap pairs are placed in a line with the distance D to the IC region.



(a)



(b)



(c)

Figure 6.3. The L_{PCB_Plane} change with (a) the number of decaps and different numbers of IC pins, (b) decap locations, (c) decap to IC distance.

6.2. L_{PCB_Plane} MODELING BASED ON PPP

The physics-based circuit model for L_{PCB_Plane} from the cavity model doesn't separate the inductance contributions from the vias and the power net area fill, and the circuit model can only be used when the current path is not influenced by the edge effect [28] of the discontinuity in the power net area fill. However, in the real design, the power net area fill does not meet the requirement to use the cavity model. For these cases, PPP can be applied to calculate the L_{PCB_Plane}.

In PPP, the plane inductance and via inductance can be extracted separated, as shown in Figure 6.1. In the physics-based circuit model for the L_{PCB_Plane} from PPP shown in Figure 6.4, the inductors in horizontal represent the plane inductance, and the inductors in vertical represent the via inductance. The result of PPP application is shown in Figure 6.5 and Figure 6.6.

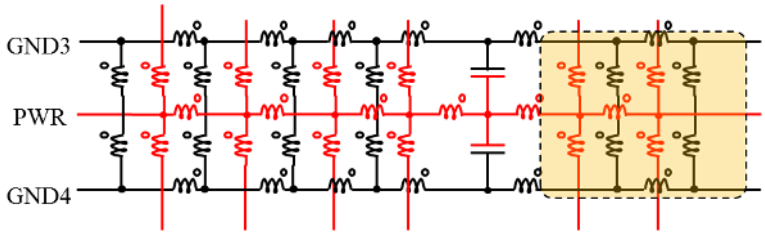
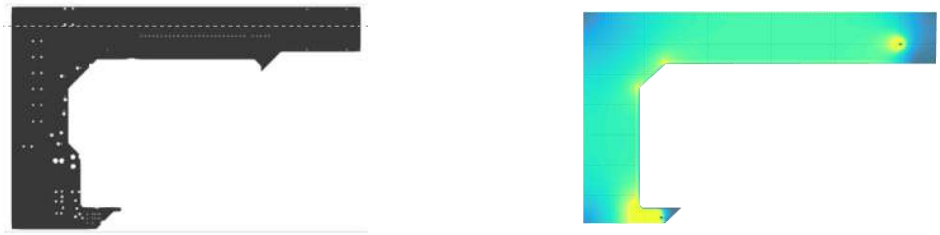


Figure 6.4. The physics-based circuit model of L_{PCB_Plane} for the stack-up shown in Figure 6.1 (a) from PPP.



(a) (b)

Figure 6.5. (a). An irregular power net area fill shape from a real design, (b) the current distribution calculation based on PPP for the power net area fill shown in (a), (c) the physics-based circuit model for L_{PCB_Plane} from PPP. [29]

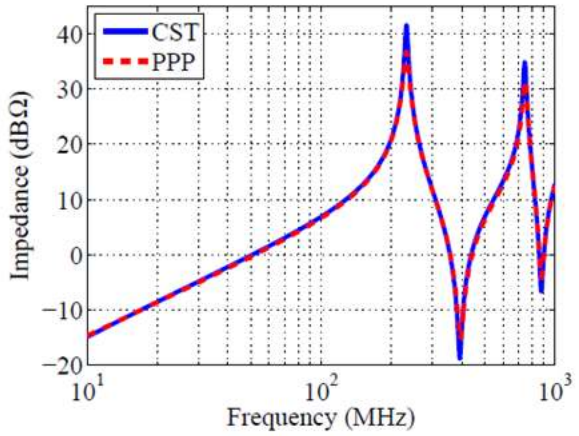


Figure 6.6. PDN input impedance for the L_{PCB_Plane} results comparison from PPP and CST [29].

An example of the irregular power net area fill in real design is shown in Figure 6.5 (a), [29]. The current distribution for this power net area fill is shown in Figure 6.5 (b). The current path is strongly influenced by the power net area fill shape. Figure 6.6 shows the comparison of the results from CST and PPP with a good agreement.

PPP can be used for the cases with irregular power area fill with voids, and holes, where the cavity model is not applicable. Even though the modeling methodologies for the L_{PCB_Plane} based on the cavity model and PPP are different, the pre-layout design methodology based on L_{PCB_Plane} is not influenced by how the physics-based circuit model is extracted, as the impact of the geometry details on the response remains the same.

* Note: The work of applying PPP to calculate L_{PCB_Plane} is contributed by Siqi Bai.

7. L_{above} DESIGN

7.1. L_{above} MODELS AND RESULTS

The connection from the decap to the PCB can be modeled using PEEC. L_{above} is the equivalent inductance from the decap to the PCB above the top GND plane when the decaps are shorted, including the trace inductance, and pad and via inductances.

A simplified 3 layer 0402 capacitor model for decap placement pattern with two decaps placed in pairs is used in this session to illustrate how to build L_{above} macromodel. The capacitor model details are shown in Figure 7.1. Labove is influenced by the distance to the ground plane. The impact of the ground plane under the capacitor macromodel is calculated using the full-wave PEEC tool and the values of the total inductance with different distance to the ground plane are listed in the Table 7.1 [25].

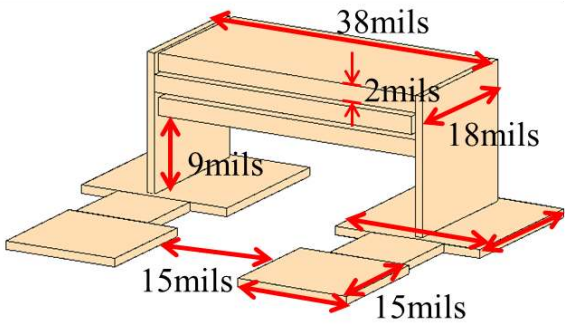


Figure 7.1. The simplified 3 layer 0402 capacitor model with traces and pads. [25]

Table 7.1. Comparison of macromodel inductances of 0402 capacitor model [25]

Model Details	Spacing to ground	Total Inductance
PEEC model with ground plane	5 mils	340 pH
PEEC model with ground plane	30 mils	390 pH
PEEC model without ground under capacitor	∞	570 pH

The process to extract the physics-based equivalent circuit model for L_{above} is explained for the decap placement pattern with decaps placed in pairs with power/power-return vias placed in alternating directions. The distance between the vias is set to be 40mils. The top and side views for doublet layout are shown in Figure 7.2 and Figure 7.3

respectively. PMSR is used to simplify the PEEC model of the L_{above}. The simplified physics-based circuit model is shown in Figure 7.4 (a). and Figure 7.4 (b). The equivalent model is intuitively related to the geometry of the structure, as shown in Figure 7.5. The self and mutual open loop inductances from PMSR are listed in Table 7.2.

$$L_{ol,PG1} \approx L_{ol11,via} + L_{ol22,via} + 2L_{ol12,via} + L_{ol11,trace} \tag{34}$$

$$L_{ol,PG2} \approx L_{ol33,via} + L_{ol44,via} + 2L_{ol34,via} + L_{ol22,trace} \tag{35}$$

$$L_{above} \approx \frac{L_{ol,PG1}L_{ol,PG2} - L_{ol12,trace}^2}{L_{ol,PG1} + L_{ol,PG2} - 2L_{ol12,trace}} \tag{36}$$

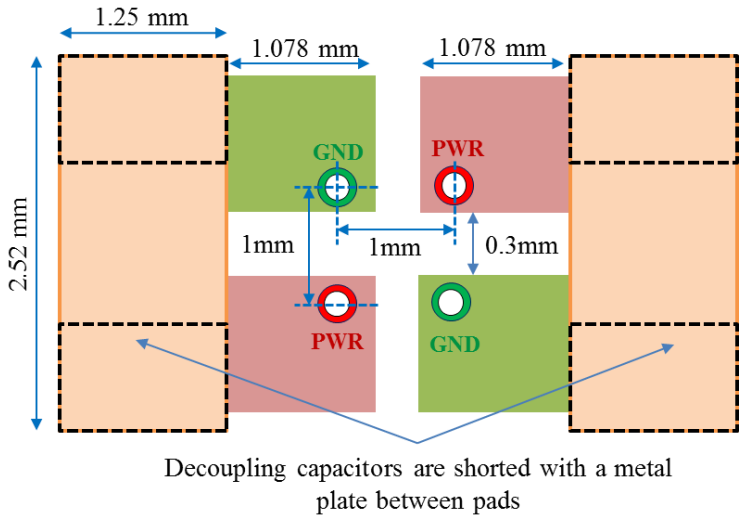


Figure 7.2. Top view of the doublet decoupling capacitors connection method. The capacitor was modeled as a metal plate [25].

The comparison between PPEC, EMC Studio and PMSR for L_{above} is shown in Table 7.3. The difference between EMC Studio and PEEC is 12%, due to the via model assumption. Additional inductance in the EMC Studio model results from lumped port, which is defined on a 1 mm long wire segment in order to excite both power vias at the same time. Analytical solution for the reduced circuit using (34), (35) and (36) is 7% lower than the PMSR solution because plane inductances are neglected.

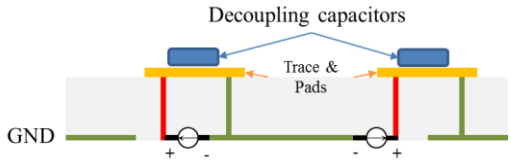
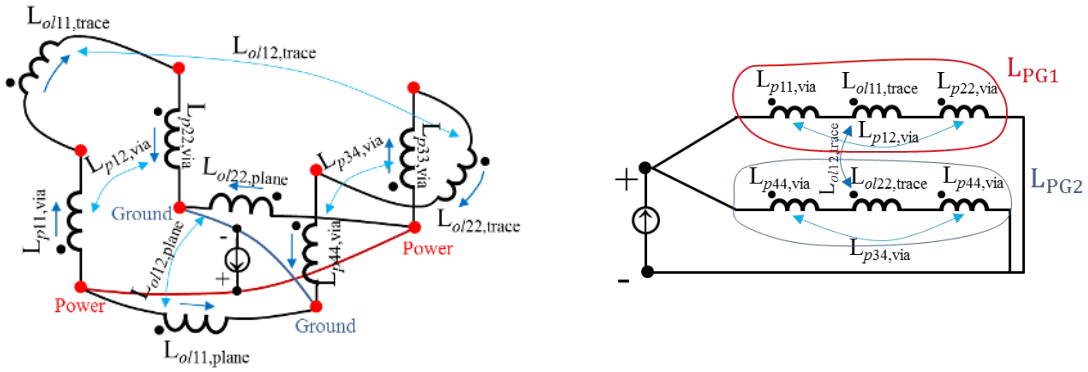


Figure 7.3. Side view of doublet decoupling capacitors connection method [25].



(a) (b)

Figure 7.4. (a) Reduced equivalent circuit for the doublet design, (b) Circuit diagram for the doublet design [25].

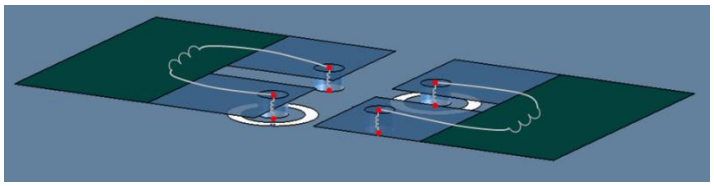


Figure 7.5. Equivalent model imposed on the doublet geometry [25].

Table 7.2. Self and mutual open loop inductances of the simplified circuit obtained using PMSR method for the doublet design [25].

$L_{p11,via}$	$L_{p22,via}$	$L_{p33,via}$	$L_{p44,via}$
20 pH	20 pH	20 pH	20 pH

$L_{p12,via}$	$L_{p13,via}$	$L_{p14,via}$	$L_{p23,via}$	$L_{p24,via}$	$L_{p34,via}$
2.9 pH	2.0 pH	2.9 pH	2.9 pH	2.0 pH	2.9 pH

$L_{ol11,trace}$	$L_{ol22,trace}$	$L_{ol12,trace}$
335pH	335 pH	28 pH

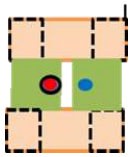
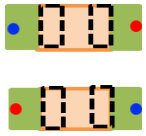
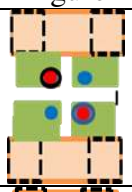
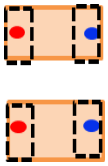
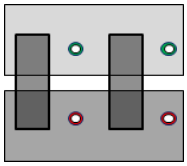
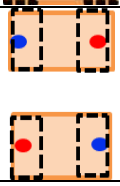
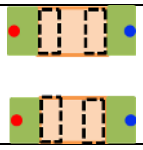
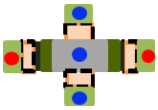
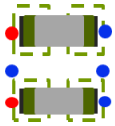
Table 7.3. L_{above} equivalent inductance for the doublet design [25].

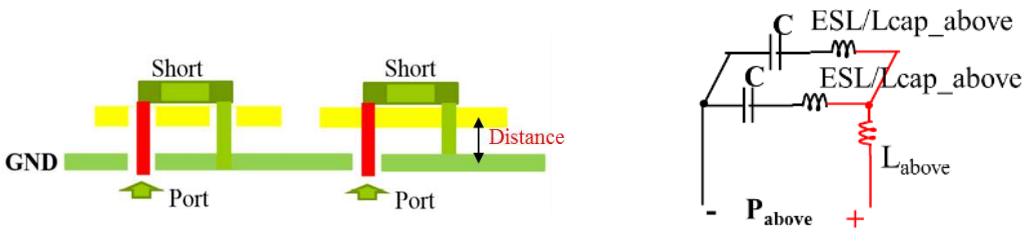
PEEC Model	PMSR Circuit	Analytical Solution from Reduced Model	EMC Studio
218 pH	218 pH	205 pH	244 pH

7.2. NINE CAPACITOR PLACEMENT PATTERNS AND DESIGN SPACE

Nine decap placement patterns are studied in the thesis for commonly used dimensions, as shown in Table 7.4. For every decap placement pattern, three different sizes 0805/0603/0402 of the decap are used to build the design library for L_{above} with different distance from the decap to the first ground plane. The L_{above} library for doublet layout with different decap distance to the ground plane is shown in Table 7.5. The circuit model is shown in Figure 7.6. The L_{above} can be used as a single inductor in series with the decoupling capacitance and decap parasitic inductance in the pre-layout methodology. The decap model for the capacitance and parasitic inductance can be referred in [30].

Table 7.4. Decoupling capacitor of sizes 0805/0603/0402 for L_{above} design space

#	Name	Figure	#	Name	Figure	#	Name	Figure
1	Shared via		2	Alternating		3	Doublet	
4	Via in pad aligned		5	Shared pad		6	Via in pad alternaing	
7	Aligned		8	3-terminal decap		9	Multi-via	



(a) (b)

Figure 7.6. (a) Side view from the decap to PCB, (b) L_{above} model used in the pre-layout methodology.

Table 7.5. L_{above} [pH] for doublet layout with 0805/0603/0402 sizes

Distance (mil)	0805	0603	0402
3.5	118	130	155
5	151	163	190
10	235	249	272
15	308	313	334

* Note: The work of L_{above} is contributed by Tamar Makharashvili, Xiang Fang, and Ying Cao.

8. PHYSICS-BASED CIRCUIT MODEL FOR PCB PDN

In this session, the physics-based circuit models for the four parts are re-assembled to form a circuit model for PCB PDN geometry, as shown in Figure 8.1. The re-assembling follows the circuit rules and the continuity of voltage and current need to be ensured in the process. In the segmentation and re-assembling process, the voltage at the ports of every part is assumed to be the same. Under this assumption, the physics-circuit model can be assembled directly at the ports.

The physics-based circuit model can be used for post PDN analysis to get the input impedance [31]. And with switching current profile, the circuit model can be used directly in circuit simulator to get the voltage ripple of the PCB PDN.

The physics-based circuit model bridges the geometry with the response, which enables designers to explore the influence of the geometry on the PDN performance.

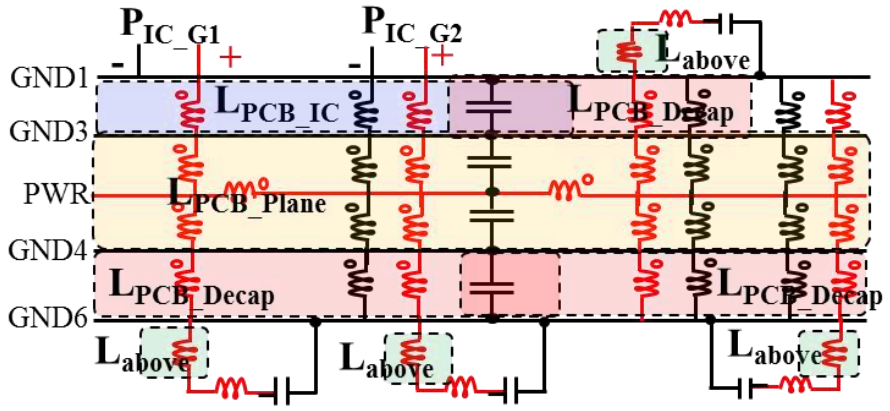


Figure 8.1. The physics-based circuit model with four parts assembled together for the geometry shown in Figure 3.6.

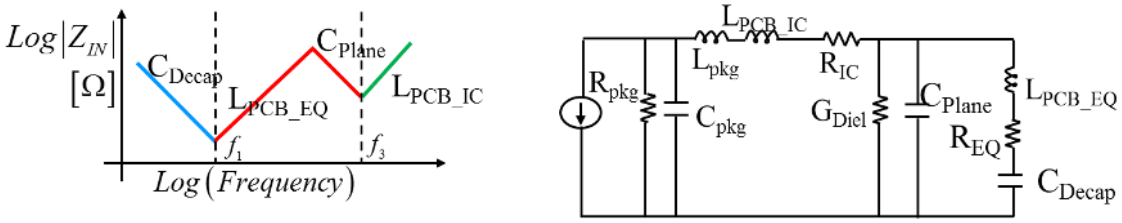
9. VOLTAGE RIPPLE CALCULATION

9.1. BEHAVIOR CIRCUIT MODEL FOR VOLTAGE RIPPLE CALCULATION

The pre-layout design methodology for PCB PDN geometry is used to achieve low voltage ripple of the PDN in the system. With the switching current profile, the voltage ripple can be calculated based on the PDN input impedance.

There are two ways of calculating the voltage ripple. From the physics-based circuit model, a transient simulation can be performed to simulate the voltage ripple directly. While, for a practical PCB PDN case, the power net area fill may be buried deep in the stack up with several power-return layers, with the decoupling capacitors placed on the top layer, on the bottom layer away from the IC part and on the bottom layer under the IC, connected to the power and ground layer using through-hole vias. The physics-based lumped circuit is very complex for such a case with hundreds of vias and decoupling capacitors. Another way of calculating voltage ripple is to use a behavior circuit model extracted from the physics-based circuit model to fit the generic PDN input impedance [16].

In the behavior circuit model, decoupling capacitor branches are combined together by using the total capacitance, C_{Decap} in one branch. And the plane capacitance is represented as C_{Plane} in the behavior circuit model, with the capacitance from two power cavities combined into C_{Plane}. L_{PCB_EQ} and L_{PCB_IC} are represented as one inductor respectively. The behavior circuit model is shown in Figure 9.1 (b) based on the generic PDN input impedance shown in Figure 9.1 (a).



(a) (b)

Figure 9.1. (a) A generic response for a PCB-PDN, (b) behavior model based on the physics-based circuit model from Figure 8.1. [16]

The Z-parameter of the PDN input impedance has poles and zeros. The peak frequencies and valley frequencies are named f_1, f_2, and f_3, in ascending order of frequency. The elements in the equivalent circuit have different behaviors at different frequency ranges. From 0 to f_1, C_{Decap} dominates the performance of the circuit. As the frequency increases, the input impedance caused by C_{Decap} decreases. While, at the same time, the impedance caused by L_{PCB_EQ} starts increasing. L_{PCB_EQ} and C_{Decap} reach series resonance at frequency f_1. After f_1, C_{Decap} gets shorted, i.e., offers low impedance. L_{PCB_EQ} dominates the performance of the circuit. The input impedance increases as the frequency increase until C_{Plane} becomes non-negligible. L_{PCB_EQ} and C_{Plane} reach parallel resonance at frequency f_2, resulting in the pole at f_2. After f_2, C_{Plane} dominates the performance of the equivalent circuit. As frequency continues increasing, impedance caused by C_{Plane} decreases while the impedance caused by L_{PCB_IC} increases. L_{PCB_IC} and C_{Plane} reach series resonance at frequency f_3. After f_3, L_{PCB_IC} determines the performance of the equivalent circuit.

In practice, the geometry always has some loss. In PDN geometry, loss contribution from three regions is considered, the decap connection region, R_{EQ}, the IC connection region, R_{IC}, and the dielectric loss in the power cavity region, G_{Diel}. R_{EQ} and R_{IC} are in series with their associated inductance and capacitance. While G_{Diel} is in parallel with C_{Plane}.

9.2. FREQUENCY SEGMENTATION

In this section, the input impedance Z-parameter is divided into three non-overlapping frequency ranges. The frequency segmentation is done such that the fitting can capture the peaks (frequency and magnitude) accurately while ignoring the zeros in the Z-parameters. The input impedance magnitude is comparatively low at the valleys, causing very little impact on the voltage ripple calculation if not captured accurately. Then the frequency is divided into three ranges: 0~f_1, f_1~f_3 and f_3~first cavity resonance frequency, after which the simplified equivalent circuit from the cavity model is not able to capture the distributed behavior of the planes [6]. In the frequency range f_1~f_3, the parallel resonance impedance can be captured. Figure 9.2 illustrates frequency segmentation.

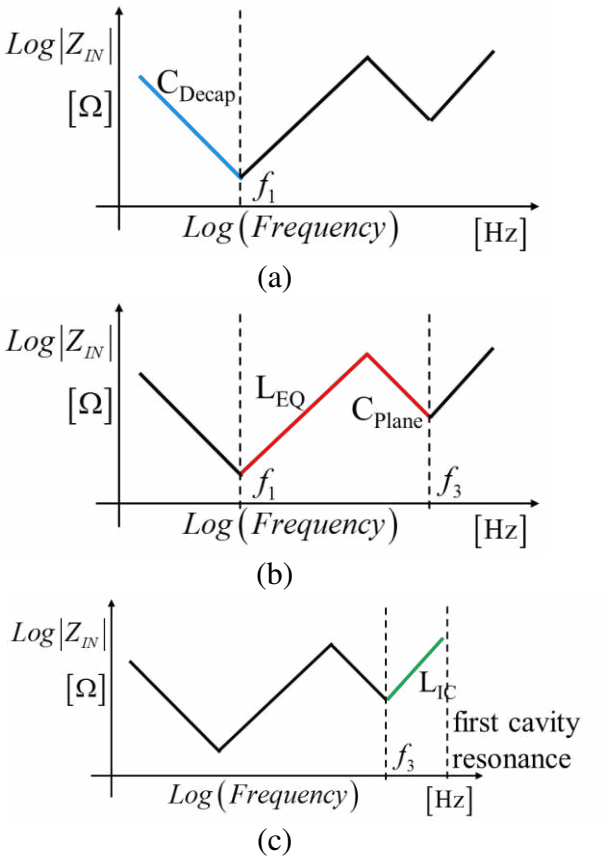


Figure 9.2. Frequency segmentation of Z-parameter (a).Z1(0~f1), (b). Z2(f1~f3), (c). Z3(f3~first cavity resonance). [16]

9.3. PARAMETERS FITTING

To find the simplified circuit model for the input impedance, the values for L_{EQ}, L_{IC}, C_{Plane} and C_{Decap} are needed. These parameters can be approximated by assuming that, only one element dominates the input impedance for a particular frequency range. The assumption holds for the frequency ranges from 0~f_1 and f_3~first cavity resonance of the power cavity. In these two frequency ranges, the impedance is linear on a log-log scale as they are dominated by C_{Decap} and L_{IC}. Using the slope of these two linear regions, C_{Decap} and L_{IC} values can be determined. The resonance frequencies, f_1 and f_3, can be picked out easily from the Z-parameter curve. From the series resonance formula for lumped circuit in (37), with corresponding L or C, the other C or L can be derived.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{37}$$

The frequency f_1 is caused by L_{PCB_EQ} and C_{Decap}. From formula, L_{PCB_EQ} can be determined. The resonance f_3 is caused by L_{IC} and C_{Plane}. From C_{Plane}, L_{PCB_IC} can also be derived. In input impedance profile, the peak and valley impedances only have the real part, which are determined by series resistance or parallel conductance. The impedances at resonance frequencies f_1, f_2, and f_3, are the resistance values R_{EQ}, R_{Diel}, R_{IC}, respectively.

9.4. EQUIVALENT CIRCUIT FOR EVERY FREQUENCY RANGE

For the first frequency range 0~f_1, C_{Plane} can be viewed as open, L_{PCB_IC} and R_{IC} is too small to be considered. And G_{Diel} is very large. It won't have large effect on the impedance value. The equivalent circuit can be simplified to the circuit shown in Figure 9.3, and only C_{Decap} dominates the circuit performance.

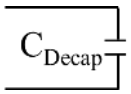


Figure 9.3. Equivalent circuit for frequency range 0~f1[16].

The input impedance is expressed as

$$Z_{in}(\omega) = \frac{1}{j\omega C_{Decap}} \tag{38}$$

For the second frequency range f_1~f_3, L_{PCB_EQ} and C_{Plane} dominate. G_{Diel} determines the input impedance peak value at resonance f_2. L_{IC} and R_{IC} can be ignored. The equivalent circuit for this frequency range is illustrated in Figure 9.4. The input impedance in this range is

$$Z_{in}(\omega) = (j\omega L_{PCB\_EQ} + R_{EQ}) \,//\, \frac{1}{j\omega C_{Plane}} \,//\, \frac{1}{G_{Diel}} \tag{39}$$

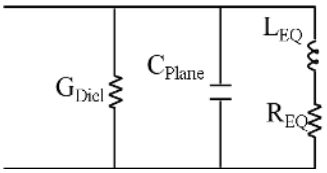


Figure 9.4. Equivalent circuit for frequency range f1~f3 [16].

For the third frequency range, only L_{PCB_IC} dominates the input impedance performance, while G_{Diel} still influences. L_{IC}, R_{IC} and G_{Diel} are in series. The equivalent circuit for this range is shown in Figure 9.5. The input impedance in this range is

$$Z_{in}(\omega) = j\omega L_{PCB\_IC} + R_{IC} + \frac{1}{G_{Diel}} \tag{40}$$

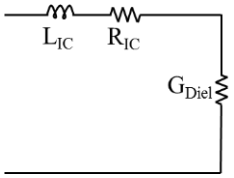


Figure 9.5. Equivalent circuit for frequency range f_3~first cavity resonance frequency [16].

9.5. VOLTAGE RIPPLE CALCULATION

In this section, the switch current is required to get the frequency domain voltage noise. Periodic triangle pulse is often used to model the switching current. In practice, when different number of transistors switch at the same time, the amplitude of the switching current may change. Considering the change of amplitude, the switching current, used in this paper, is made up two of periodic triangular pulses with different amplitudes, as shown in Figure 9.6 (a) [16]. Together with the input impedances for the three frequency ranges, three frequency domain voltage noises are generated. Inverse Fourier Transform can be applied to transform the voltage noise to time domain voltage ripple analytically, as(41).

$$\begin{aligned} &v_1(t) = F^{-1}\{I(f)Z_1(f)\}, v_2(t) = F^{-1}\{I(f)Z_2(f)\}, v_3(t) = F^{-1}\{I(f)Z_3(f)\} \\ &v_{ripple}(t) = v_1(t) + v_2(t) + v_3(t) \end{aligned} \tag{41}$$

This provides the basic methodology to transform the noise voltage from the frequency domain to time domain. However, in practice, the inverse Fourier Transform is difficult to implement for an arbitrary waveform. Instead, as the switching current can be represented with period triangular pulses, Fourier series can be applied to transform the signal between the frequency domain and time domain. From Fourier series, the switching current can be expressed as a sum of the complex exponential functions as,

$$I(t) = \sum_{k=0}^{\infty} X_k^I e^{j2\pi k f_0 t} \tag{42}$$

The coefficient can be expressed as,

$$X_k^I = \frac{1}{T_0}\int_0^{T_0} X(t) e^{-j2\pi k f_0 t} dt \tag{43}$$

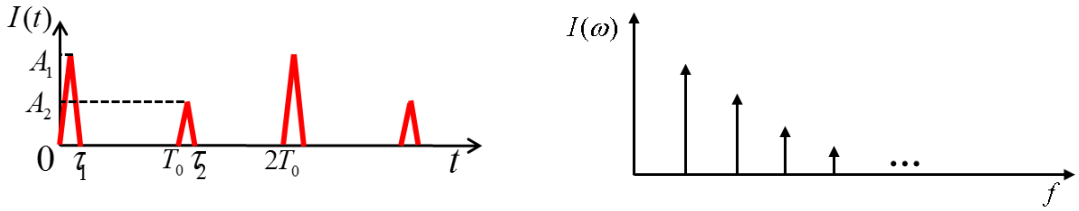
The coefficients for switching current are,

$$\begin{aligned} X_k &= \frac{2A_1}{(-\mathrm{j}2\pi\,\mathrm{f_0 k})^2 \tau_1 T_0}(\mathrm{e}^{-\mathrm{j}2\pi\,\mathrm{f_0 k}\,\tau_1} - 2\,\mathrm{e}^{-\frac{\mathrm{j}2\pi\,\mathrm{f_0 k}\,\tau_1}{2}} + 1) \\ &+ \frac{2A_2}{(-\mathrm{j}2\pi\,\mathrm{f_0 k})^2 (\tau_2 - \mathrm{T_0}/2) T_0}(\mathrm{e}^{-\mathrm{j}2\pi\,\mathrm{f_0 k}\,\tau_2} - 2\,\mathrm{e}^{-\mathrm{j}\pi\,\mathrm{f_0 k}(\frac{\mathrm{T_0}}{2}+\tau_2)} + \mathrm{e}^{-\mathrm{j}\pi\,\mathrm{f_0 k T_0}}) \\ f_0 &= \frac{1}{T_0} \end{aligned} \tag{44}$$

When k=1,

$$X_1^I = \frac{A_1\tau_1}{2T_0} + \frac{A_2(\tau_2 - \mathrm{T_0}/2)}{2T_0} \tag{45}$$

In frequency domain, the switching current has Dirac functions with the amplitude of the coefficients at corresponding frequencies, as shown in Figure 9.6 (b).



(a) (b)

Figure 9.6. Switching Current Profile in (a) Time domain, (b) Frequency domain. [16]

In the frequency domain,

$$V(f) = I(f) \times Z(f) \tag{46}$$

Frequency domain voltage noise components can be found by multiplying the current and the input impedance in the frequency domain. As the current has frequency components at the fundamental frequency and its harmonics, the voltage noise has the same frequency components. The amplitudes at these frequencies are the product of current component amplitudes and Z-parameter amplitudes at the same frequencies. From Fourier series definition, the voltage noise components contain the information of Fourier series coefficients and corresponding frequency components as,

$$X_k^V = X_k^I \times Z(kf_0) \tag{47}$$

$$V(t) = \sum_{k=0}^{\infty} X_k^V e^{j2\pi kf_0 t} \tag{48}$$

Here, f_0 is the fundamental frequency.

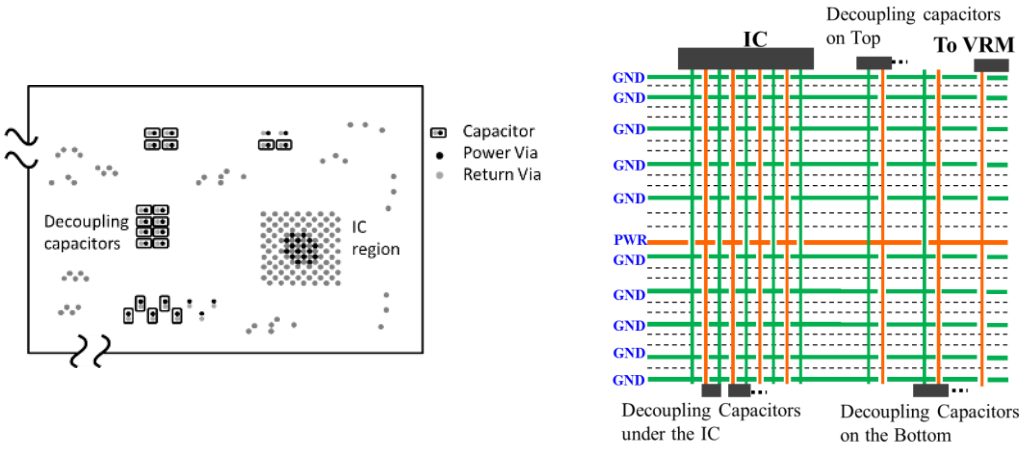
Using the steps described above, the contribution of every frequency range to the total voltage ripple is quantified. By adding the voltage ripples caused by different ranges of input impedance, the total voltage ripple behavior is well defined. Because of the adding procedure, the divided frequency ranges cannot be overlapped, or it may lead to some frequency components counted twice.

9.6. APPLICATION TO REAL-WORLD PCB

A real high layer-count PCB PDN geometry is used to generate the response, as shown in Figure 9.7. The board has 28 layers, with the power net area fill at layer 16. This particular case has decoupling capacitors placed on the top of the PCB. The representative top view of this geometry is shown in Figure 9.7 (a). The stack up of the board is shown in Figure 9.7 (b). The detailed layout and capacitor locations cannot be shared due to confidentiality restrictions.

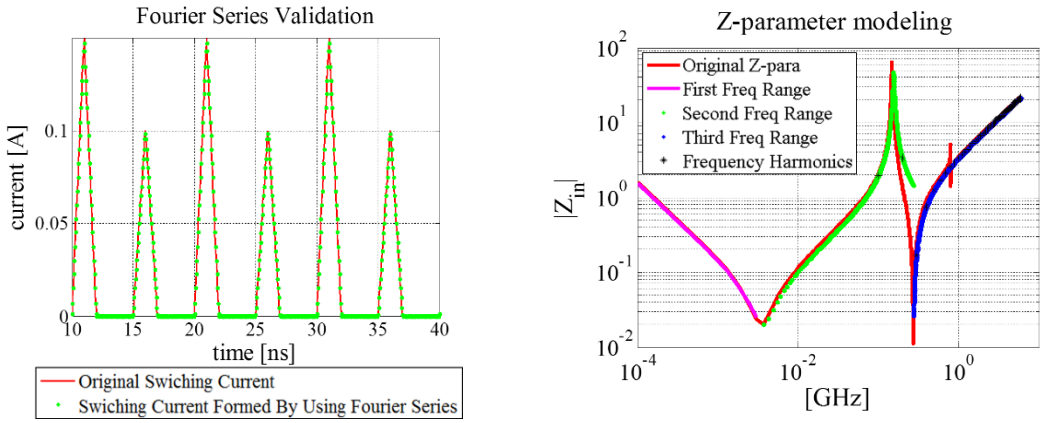
The switching current frequency is decided based on IC switching frequency. For a data rate of 200 Mbps, the bit width is 5ns. For the switching current, $T_0 = 5ns$. The rise time of the signal is 1 ns. The base of the triangular pulse is 2 ns wide. The amplitudes A_1 is 1.5 A, A_2 is 1 A. The Fourier series coefficients are calculated for the current waveform, and used to calculate back the original waveform to validate the calculations. Figure 9.8 (a) compares the signal calculated by Fourier series with the original signal.

The input impedance for the geometry mentioned above is used to fit the simplified circuit model. Figure 9.8 (b) compares the input impedance calculated by applying simplified equivalent circuit at different frequency ranges with the original measurement. This validates the simplified circuit model response in the frequency domain. The voltage ripples for different frequency ranges are shown in Figure 9.9 (a), (b) and (c). The voltage ripple for the first frequency range is zero, because there is no harmonic in this frequency range. It can be observed that the voltage ripples have different frequency contents. By adding them together, the total voltage ripple is shown Figure 9.9 (d).



(a) (b)

Figure 9.7. Real high layer PCB board geometry (a). Top view of the board, (b). The stack up of the board with many decoupling capacitors placed on the top layer around the IC, bottom of the IC and on the bottom layer but away from the IC. [20]



(a) (b)

Figure 9.8. (a) Compare signal formed by Fourier series with the original signal [10], (b) Equivalent circuit validation for every frequency range. [16]

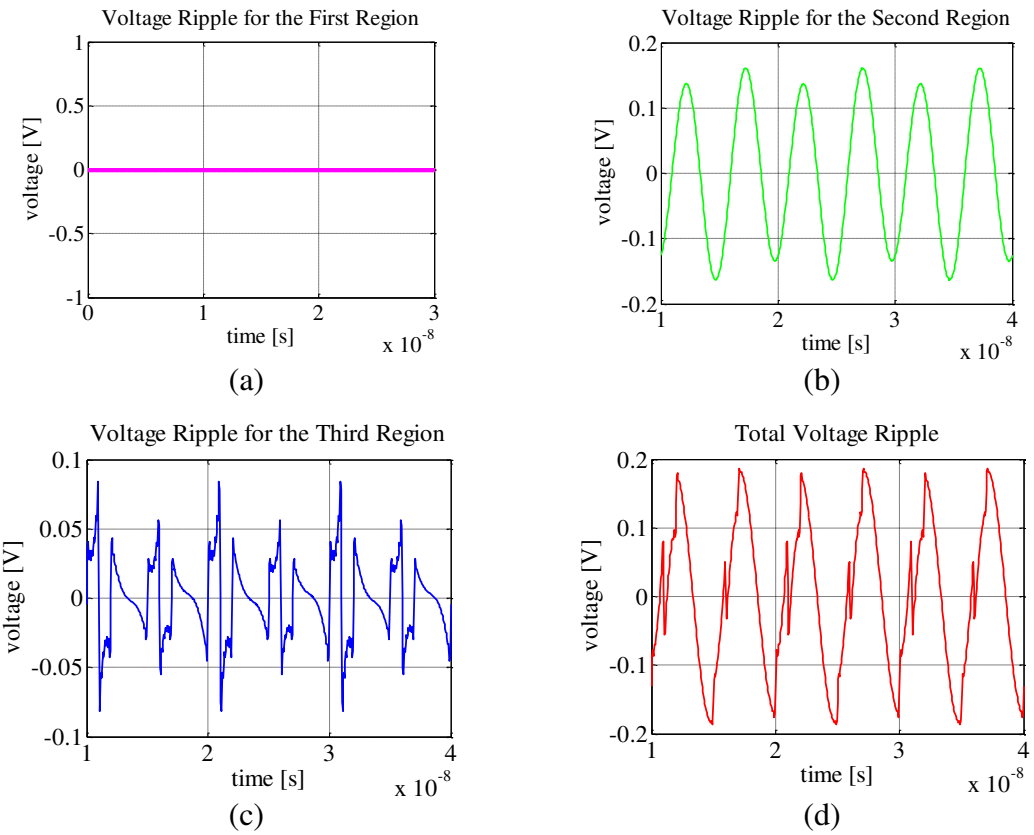


Figure 9.9. Voltage ripple in time domain for (a) frequency 0~f1; (b) f1~f3; (3) f3~first cavity resonance; (4) total voltage ripple. [16]

10. PRE-LAYOUT DESIGN METHODOLOGY PROCEDURE

10.1. PRE-LAYOUT DESIGN CRITERIA

The pre-layout design methodology is based on the L_{PCB_EQ} and L_{PCB_IC}. In the methodology, the ratio of the different between L_{PCB_EQ} and L_{PCB_IC} to L_{PCB_IC} can be used a design criteria.

$$\frac{L_{PCB\_EQ} - L_{PCB\_IC}}{L_{PCB\_IC}} \leq x \tag{49}$$

Substituting(15), the criteria can be represented as,

$$\frac{L_{PCB\_Plane} + L_{PCB\_Decap} + L_{above}}{L_{PCB\_IC}} \leq x \tag{50}$$

Based on the stack-up and geometries, two generic cases can be identified regarding to the decap design and power net area design. When the inductance contribution from the power net area fill is much larger than the decap contribution, the design criteria can be change to (51).

$$\begin{aligned} &L_{PCB\_Plane} \gg (L_{PCB\_Decaps} + L_{above}), \\ &\frac{L_{PCB\_Plane}}{L_{PCB\_IC}} \leq x \end{aligned} \tag{51}$$

And if the decap connection inductance is much larger than the power net area fill inductance, the the design criteria can be change to (52).

$$\begin{aligned} &L_{PCB\_Plane} \ll L_{PCB\_Decap} + L_{above}, \\ &\frac{L_{PCB\_Decap}}{L_{PCB\_IC}} \leq x \end{aligned} \tag{52}$$

In the decap connection inductance, the inductance contribution of L_{PCB_Decap} and L_{above} can also be analyzed separately based on the dominate component.

Thus, L_{PCB_IC} has to be designed first based on the pre-layout methodology. And then, the domination part of the components in L_{PCB_Plane}, L_{PCB_Decap} and L_{above} can be designed separately.

10.2. L_{PCB_IC} DESIGN

The IC interconnection inductance L_{PCB_IC} is the smallest value of the L_{PCB_EQ}. To lower the PDN impedance, the first step is to lower L_{PCB_IC}. L_{PCB_IC} depends on the distance from IC to power net area fill, IC pin placement patterns, IC pin numbers, pad-stack and pitch size. Usually, IC pin placement is controlled by the chip or package designers. Thus, the best practice to lower L_{PCB_IC} is to put the power net area fill as close to the IC as possible with the consideration of other requirements and limitation of the design, since L_{PCB_IC} is proportional to the distance from the IC to the power net area fill.

After L_{PCB_IC} design, the dominant component of L_{PCB_EQ} can be used for further PDN layout design.

10.3. PRE-LAYOUT DESIGN APPROACH BASED ON L_{PCB_Decap}

When L_{PCB_Decap} is the dominant component in the L_{PCB_EQ}, a recommended procedure is to put the decaps can be put on the nearest possible layer to the power net area fill first. Then, the possible decap package pattern with the fastest convergence rate can be chosen and the number of decaps can be calculated or estimated based on the design curves and formulas. For other decap placement patterns, the L_{PCB_Decap} can be simulated rigorously using (28) to (30) and the convergence rate can be obtained to guide the design.

10.4. DESIGN APPROACH BASED L_{above}

When L_{above} is the dominant component in the L_{PCB_EQ}, the placement pattern of decap with the smallest L_{above} should be chosen to lower L_{PCB_EQ}. In this case, the decap locations on the PCB is irrelevant in the design process.

10.5. DESIGN APPROACH BASED ON L_{PCB_Plane} DOMINANT

When L_{PCB_Plane} is the dominant component in the L_{PCB_EQ}, the current path in the power net area fill needs to be changed to minimize the L_{PCB_Plane}. There are several options. The decaps can be placed as close as possible to the IC region to reduce the current path from the IC to the decap. Adding decaps and IC pins can reduce the L_{PCB_Plane}. The decap placement pattern with the fastest convergence rate can be used to lower L_{PCB_Plane}. The mutual inductance between the power net area fill with the power-return area fill can be used to lower L_{PCB_Plane}. The power-return area fill in the stack-up can be placed closer to the power net area fill to maximize the mutual inductance between them. If the power net area fill is irregular, or with many voids, the shape can be redesigned to reduce the dependence of the current path on the shape. For the case with the thickness of the total PCB is small, the decaps can be placed directly under the IC pin vias on the bottom layer. In this case, the current does not have to cross the power net area fill, and LPCB_EQ can be calculated directly using the same topology as the L_{PCB_Decap} or L_{PCB_IC}. The ratio of the L_{PCB_EQ} to L_{PCB_IC} is the same as the thickness of the PCB to the distance from the IC to the power net area fill. For thin PCB PDN geometries, the approach of placing the decaps under the IC on the bottom layer can achieve low L_{PCB_EQ}. But since the placement pattern for the decaps is limited by the IC via placement pattern, this method is not flexible.

11. DISCUSSIONS AND CONCLUSION

A physics-based pre-layout design methodology is proposed in the thesis for PCB PDN geometry. The methodology provides a systematic approach to guide the PCB PDN design, with the physics-based circuit model to bridge the PDN response with the geometry details. The methodology can be used be used with high layer count structures and low layer count structures, in the same manner, as generic response of the PCB-PDN remains the same.

In the pre-layout design methodology, four parts are segmented and modeled separately first, and the physics-based circuit models for the four parts are re-assembled to form one model for the PDN geometry. The methodology is based on the assumption that the four parts have little or no coupling between each other. As long as the assumption is applicable to the design, the pre-layout methodology design methodology can be used.

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