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***Abstract*— This paper presents a direct digital converter for Wheatstone bridge sensors which is realized with commercial off-the-shelf (COTS) components. The power efficiency of the readout is enhanced by embedding the bridge sensor in a second-order Continuous-Time Sigma-Delta Modulator (CTΔΣM). By directly digitizing the output signal of a Wheatstone bridge in the current mode, the noise performance is dominated by the operational amplifier (Opamp) in the first integrator and the bridge sensor. To demonstrate the performance of the proposed circuit, a MEMS Piezoresistive Differential Pressure (MPDP) sensor is used. Measurement results show a resolution of 12.7 mPa$_{rms}$ (0.41 mΩ$_{rms}$), with a 0.5 ms conversion time, can be achieved. Powered by 5 V, the circuit and the bridge sensor draws 9.55 mW and 7.58 mW, respectively.**

***Index Terms*—Direct digital converter, bridge sensor readout, Continuous-Time Sigma-Delta Modulator, mPa-level differential pressure sensing.**

I. Introduction

RECENTLY, digital converters that can directly convert physical values of sensors into digital values have become increasingly more attractive for many low-power and energy-constrained applications. Some examples are: capacitance-to-digital converters (CDCs), inductance-to-digital converters (IDCs), and resistance-to-digital converters (RDCs) [1-3]. Most of the reported solutions are based on application-specific integrated circuits (ASICs) as they offer energy efficiency and small footprints. However, in many industrial applications, such as precision mechatronic systems used in manufacturing [4], only a limited number of high performance sensors are needed. The use of ASICs increases cost, while available off-the-shelf circuits cannot always provide the required performance. Therefore, the alternative is to design a readout circuit using commercial off-the-shelf (COTS) components.

This paper presents a power-efficient COTS-based direct digital converter for precision mechatronic systems which detects differential pressure with 15 mPa$_{rms}$ resolution [4]. To facilitate use in the feedback of a fast servo loop for pressure control, the direct digital converter requires a 0.5 ms conversion time [4]. Furthermore, the power consumption of the direct digital converter should be less than 20 mW to minimize the self-heating of the electronics.

Owing to their high sensitivity, piezoresistive differential pressure sensors are commonly embedded in Wheatstone bridges to measure ultra-low differential pressure. An example of such a sensor is the AC4010 from Acuity Inc. (Fig. 1a), which senses differential pressure $p_1 - p_2$ by measuring the deflection of a silicon membrane with high piezoresistivity (Fig. 1b) [5]. With four piezoresistors connected in a full Wheatstone bridge, the sensitivity is quadrupled.

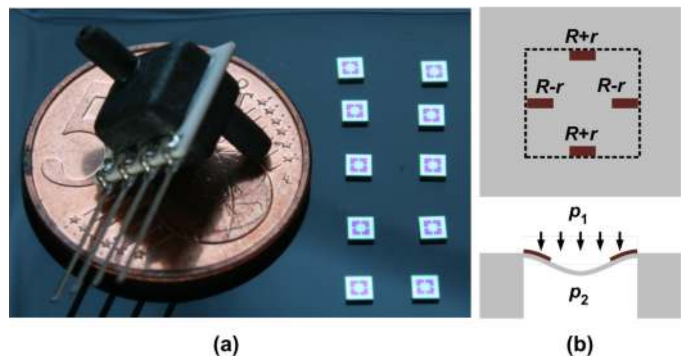


Fig. 1. (a) MEMS piezoresistive differential pressure sensor; (b) Piezoresistors that can be used in a full Wheatstone bridge configuration.

Conventionally, the bridge sensor is operated in voltage mode with an Instrumentation Amplifier (IA) that amplifies the output voltage of the bridge [6]. These readout methods consist of two main parts: an IA and an Analog-to-Digital Converter (ADC), as shown in Fig. 2a. An IA is typically designed with a high input impedance and a large accurate gain to boost the signal amplitude of the sensor outputs and to drive the succeeding ADC stage, which converts the results into digital code. This results in readout involving two local feedback loops to guarantee precision (IA and ADC) (Fig. 2a), with an overall open loop gain that far exceeds the necessary closed loop gain. However, this readout has lower energy efficiency, since an IA consists of at least two operational amplifiers (Opamps), in case high resolution has to be achieved, which dominates the power dissipation readout [7 - 9].

To address these issues, an alternative readout topology has been proposed in the literature (Fig. 2b) [10, 11]. It embeds the IA and the ADC in one closed loop to improve energy efficiency and reduce complexity. In this architecture, one feedback loop is implemented using an indirect current feedback network. The high input impedance of the readout ICs is realized using Gm-C integrators. However, additional design effort is needed to accommodate the poor linearity of the Gm-C integrators, resulting in a large area [11]. Furthermore, applying this architecture with COTS components is difficult as a very good match is required between the G1 and G2 stages to avoid thermal drift. Lastly, the energy efficiency of the readout is still limited by these two Gm stages.

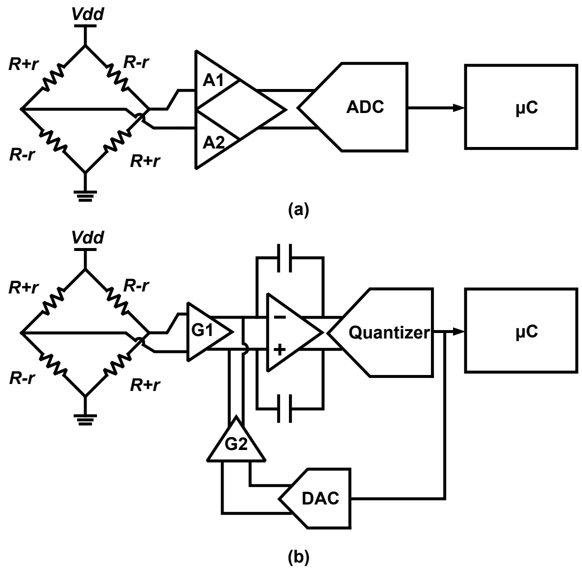


Fig. 2. Typical readout solution for the bridge sensor: (a) Two-loop topology; (b) Single-loop topology.

In comparison, capacitively coupled IAs (CCIAs) provide even better energy efficiency because they only have a single main Opamp which dominates the noise and power dissipation of the readout circuit of the bridge sensors [12]. However, an energy-efficient CCIA is also difficult to realize using COTS components on a PCB board, since the noise performance will be degraded by the PCB board parasitic [13].

Reading the Wheatstone bridge in the current mode is a promising approach to avoid the shortcomings of the voltage mode readout approach and thus improve the energy efficiency of the sensing system. Several studies on the current mode readout using transimpedence amplifiers and current conveyors have been reported [14, 15]. However, to obtain a digital output from such an amplified signal, a Discrete-Time (DT) ADC with an anti-aliasing filter or a high oversampling ratio is needed.

An optimized COTS-based current mode readout solution that embeds the MPDP sensor into a second-order Continuous-Time Sigma-Delta Modulator (CTΔΣM) which does not require a high-order anti-aliasing filter, is proposed in this paper. This solution simplifies the design of the readout without compromising performance. The paper is organized as follows. Section II discusses the operating principle of the readout circuit. Section III provides details of the readout architecture. The circuit implementation and COTS components selection is discussed in Section IV. Section V presents experimental results obtained using a prototype readout with the MPDP sensor. Finally, Section VI presents conclusions.

II. Current Mode Operation Principle

Bridge sensors are usually read out in voltage mode, which can, ideally, provide the best linearity performance. The output V_{out} of the Wheatstone bridge can be defined as:

$$V_{\text{out,bridge}} = \frac{Vdd \times r}{R}, \quad (1)$$

where R is the bridge resistance and r is varying resistance. However, as shown in Fig. 2a, two of the Opamps A1 and A2 in a three-Opamp IA are typically located close to the bridge sensors in the signal chain to provide high input impedance [4]. These two Opamps usually dominate the noise contribution of the readout. To obtain better noise performance, more power needs to be consumed by these two main amplifiers, which consequently increases the power consumption of the readout. The same statement is valid for indirect current-feedback IAs (CFIAs), since the input and the feedback Gm stages are the main noise sources of the readout [9].

Instead of reading the Wheatstone bridge in the voltage mode, an alternative interfacing strategy with better energy efficiency is to read out the output current of the Wheatstone bridge with a Transimpedance Amplifier (TIA) [14], as shown in Fig. 3a. The main noise contribution of this circuit comes from a single main Opamp, because R_f is significantly larger than R. The output signal of the TIA can be defined as:

$$V_{\text{out,TIA}} = \frac{2 \times Vdd \times r}{R^2 - r^2} R_f . \quad (2)$$

This shows that the output is a nonlinear function of r. However, the additional nonlinearity due to the variation of r is relatively small compared to the intrinsic nonlinearity of MPDP sensors, since the ratio of r/R is smaller than 1%.

An additional benefit of MPDP sensors is that sensitivity can be easily adjusted by tuning the feedback resistor R_f, which will accommodate the large spread in MPDP sensitivity.

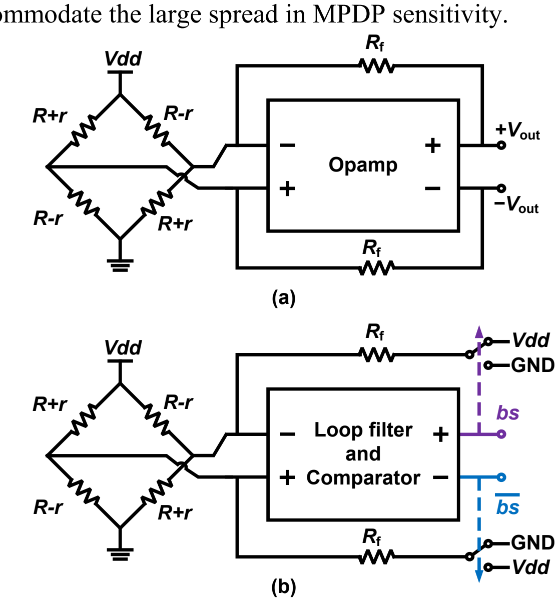


Fig. 3. (a) Wheatstone bridge interface with analog feedback (TIA); (b) Wheatstone bridge interface with digital feedback.

However, in practice, the frequency components in the TIA outputs that are greater than half the sampling rate will alias into the frequency band of interest during the analog-to-digital conversion (ADC) when sampling type (discrete time – DT) ADCs are used [16]. One possible solution is to use an anti-aliasing filter before this ADC, e.g. a SAR ADC, to avoid the impact of high-frequency noise and interference. Especially, for Nyquist rate ADCs, a high-order anti-aliasing filter is preferred for maintaining the gain accuracy around the corner frequency of the filter. Another solution to avoid aliasing is to use an oversampling ADC to relax the requirement for the anti-aliasing filter. However, this oversampling usually results in more power dissipation.

Alternatively, the analog resistive feedback network of the TIA can be realized digitally by using the charge balancing technique in a CT ΣΔ Modulator loop, as shown in Fig. 3b. Fig. 4 shows the readout approach, which is realized by embedding the Wheatstone bridge into a first-order CT ΣΔ ADC. The DC output current of the bridge sensor that is caused by differential pressure will be injected into the virtual ground of the integrator. In every clock cycle, the compensation current, controlled by *bs*, attempts to balance the current from the bridge. Therefore, in a long stream of zeros and ones, the negative feedback loop will make sure the averaged output voltage of the integrator is zero. By extracting the ratio of the number of ones and the total number of clock cycles, the output current of the Wheatstone bridge can be accurately obtained [17].

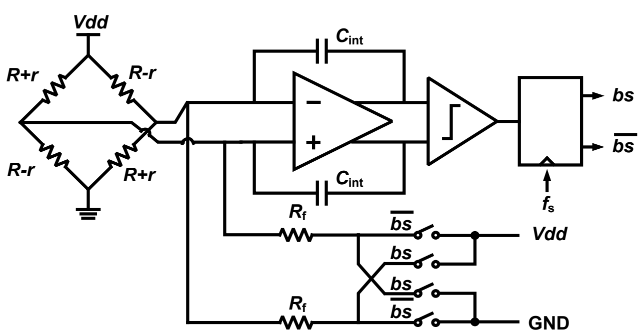


Fig. 4. Wheatstone bridge interface with a first-order CT ΣΔ ADC.

Compared to bridge readout based on DT ΣΔ Modulators, readout based on CT ΣΔ Modulators has several advantages. First, a CT ΣΔ Modulator is inherently anti-aliasing. Compared to DT ΣΔ Modulators, CT ΣΔ Modulators postpone the sampling process until the output of the loop filters. Consequently, the noise folding occurs at the less sensitive point of the loop. The absence of an anti-aliasing filter makes CT ΣΔ Modulators more energy-efficient compared to their DT counterparts [18]. Second, unlike a DT ΣΔ Modulator, which requires a certain unity gain frequency of the Opamp in the loop for a given clock frequency, the clock frequency of a CT ΣΔ Modulator is limited by the regeneration time of the quantizer and the update time of the feedback DAC. Thus, a CT ΣΔ Modulator with a slower Opamp can achieve the same accuracy as a DT ΣΔ Modulator, which has to employ relatively faster Opamps in the loop; hence less power is required in a CT ΣΔ Modulator given the trade-off between power and speed. Last but not least, the switches in the CT ΣΔ Modulator are at low impedance nodes, which simplifies the COTS-based design, as COTS switches usually have a larger charge injection error.

III. Readout Architecture

A. Topology

To guarantee the accuracy of the ΣΔ Modulator, a single-bit DAC, which is inherently linear, has been chosen. Thus, the quantizer can be realized using a comparator. In order to meet the resolution specification of the bridge sensors with fewer clock cycles, a higher-order ΣΔ modulator is preferable. Here, the second-order topology is adopted for energy efficiency. The oversampling ratio is set at 500 so that it can provide enough quantization noise suppression for the target resolution.

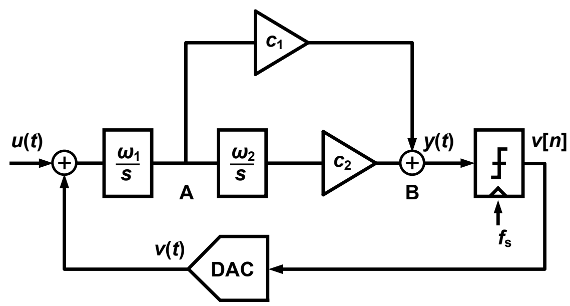


Fig. 5. Feedforward second-order ΣΔ Modulator.

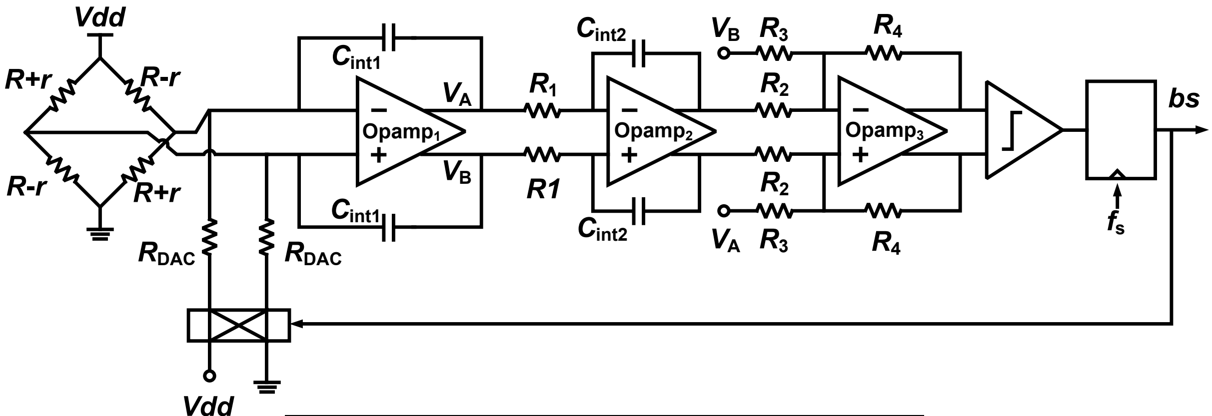
A second-order ΣΔ Modulator requires a certain type of compensation provided by either a feedback structure or feedforward structure to maintain its stability. A feedforward structure is designed (Fig. 5) to simplify the feedback DAC, since the feedback structure requires two feedback DACs. The transfer function from A to B (Fig. 5) is given by:

$$H(s)_{A\to B} = \frac{V_B}{V_A} = c_1 + c_2 \cdot \frac{\omega_2}{s}. \qquad (3)$$

To optimize the Noise Transfer Function (NTF) of the ΣΔ Modulator, we have chosen $c_1 = 4$ and $c_2 = 1$. The first integrator is realized by a current integrator with capacitive feedback. The second integrator is an RC type in which the adder at node B is realized by a differential amplifier with resistive feedback (Fig. 6).

B. Noise Analysis

Because the out-of-band noise of ΣΔ Modulators is eliminated by the digital decimation filter, only in-band noise needs to be considered. Moreover, due to the inherent anti-aliasing property of CT ΣΔ Modulators, sampling does not increase the in-band noise [18]. The in-band noise of the remaining loop filter is suppressed by the gain of the first integrator when referred to the input. This allows the noise contributed by the second integrator, adder, and comparator to be negligible because of the high low-frequency gain of the Opamp in the first integrator. Thus, the main noise contributors are the bridge sensor, the Opamp in the first integrator, and the DAC.



R	3.3 kΩ	R_3	50 kΩ
r	33 Ω	R_4	200 kΩ
R_{DAC}	200 kΩ	C_{int1}	33 pF
R_1	100 kΩ	C_{int2}	4 pF
R_2	200 kΩ	f_s	2 MHz

Fig. 6. Schematic of the feedforward second-order ΣΔ Modulator.

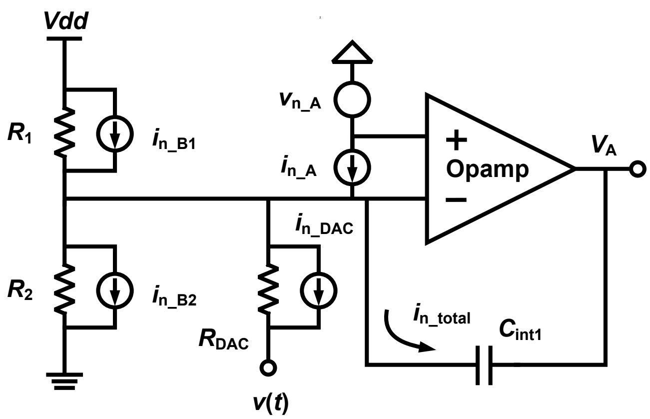


Fig. 7. Noise analysis of the first integrator.

To simplify the analysis, a single-ended version of the loop filter, as shown in Fig. 7, is used to derive the input-referred noise of the CT ΣΔ Modulator. The input-referred noise power at the virtual ground of the first integrator, which includes the noise of the Wheatstone bridge, is given by:

$$
\begin{gathered}
i_{n\_total}^2 = i_{n\_B1}^2 + i_{n\_B2}^2 + i_{n\_DAC}^2 + i_{n\_A}^2 + \left(\frac{v_{n\_A}}{R \| R \| R_{DAC}} \right)^2 , \\
i_{n\_total}^2 \approx 2 \cdot i_{n\_B}^2 + i_{n\_A}^2 + \left(\frac{2 \cdot v_{n\_A}}{R} \right)^2 ,
\end{gathered}
\tag{4}
$$

where v_{n_A} is the input-referred voltage noise, i_{n_A} is the input current noise of the amplifier in the first integrator, and $R=R_1=R_2$. As shown in Eq. 4, the major noise source of this readout circuit is the Opamp and the bridge sensor, since R_{DAC} >> R. This suggests that the proposed architecture can be more power-efficient compared to traditional voltage-mode readouts. Moreover, the performance of the Opamp in the first integrator is the key to the readout performance.

IV. Implementation Details

A PCB-level prototype that uses COTS components has been implemented. In this design, the reference voltage of the readout DAC is the same as the bridge biasing voltage. Therefore, the effect of variation in the biasing voltage is suppressed by the ratio-metric conversion. The noise, offset, and non-linearity of the remaining CT ΣΔ Modulator are suppressed by the gain of the first integrator. Hence, the Opamp of the first integrator and the DAC are the most critical blocks in this design.

A. Opamp of the First Integrator

The MPDP sensor has two main noise sources: thermal noise and $1/f$ noise. The measured output current noise of the sensor (AC4010, Acuity Incorporated) over 2 kHz of bandwidth is 325 pA when the biasing voltage of the sensor is 5 V. First, to ensure that the resolution is defined by the current noise of the sensor, the noise contribution of the readout should be lower of the noise of the MPDP sensor. Second, an energy-efficient fully differential Opamp is needed to minimize the self-heating effect of the first integrator. Lastly, the input offset current drift of the Opamp should be small.

The input offset current drift can be defined as:

$$I_{OS\_drift} = \sqrt{I_{OS\_drift}{}^{2} + \left(\frac{V_{OS\_drift}}{2 \cdot R}\right)^{2}}\ . \tag{5}$$

In Table I four state-of-the-art fully differential amplifiers are presented with their power dissipation, offset, and noise performance. For comparison purposes, LTC6363 [19] and THS4551 [20] are selected as the Opamp of the first integrator, since they have low noise and low offset drift.

TABLE I

STATE-OF-THE-ART DIFFERENTIAL OPAMPS

	THS4521	LTC6363	ADA4940	THS4551
Noise Bandwidth (kHz)	2	2	2	2
Input Current Noise (pA)	357	300	--[1]	245
Input Offset Drift (pA/K)	706	166	--[1]	156
Voltage Supply (V)	5	5	5	5
Power Consumption (mW)	5.7	9.5	6.25	6.85

1. No data exists on the input current noise corner and input offset current drift in the datasheet [21].

B. Digital-to-Analog Converter

A ΣΔ Modulator can only be as good as its DAC. Thus, a single-bit DAC, as shown in Fig. 8, is used here due to its inherent linearity [18]. However, the component mismatch and parasitics in the DAC usually result in offset, drift, and degradation of the readout's common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) [19]. Consequently, the resistors and switches of the DAC need to be carefully selected for good matching and stability; the layout of the DAC needs to be carefully designed to minimize the mismatch introduced by parasitics.

In this design the DAC is realized with LT5400-2: a quad matched resitor network of 100 kΩ resistors with 0.01% resistance matching and 0.2 ppm/°C matching temperature drift [22]. This excellent matching not only guarantees better performance than independently matched resistors, but also simplifies the layout of the DAC.

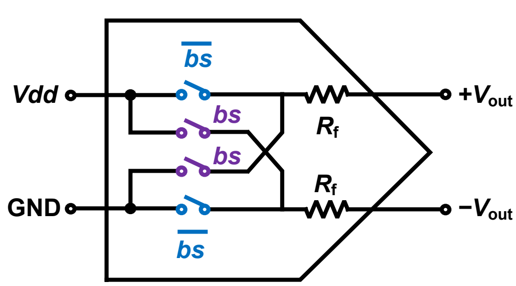


Fig. 8. Simplified schematic of the DAC.

The on-resistance of the switches in the DAC should be much smaller than R_{DAC} to minimize the drift caused by the on-resistance drift. ADG787 [23], which yields low on-resistance and low leakage currents, has therefore been selected for the switches. Owing to the differential architecture and high resistance value of the R_{DAC}, the charge error due to the charge injection is suppressed.

C. Opamps of the Second Integrator and Adder

The noise of the second integrator is suppressed by the gain of the first integrator in the loop. Hence, the noise requirement of the Opamp in the second integrator is relaxed. The same statement is also valid for the Opamp in the adder. To maintain the low power dissipation of the readout, two THS4531s [24], where the single channel draws only 1.25 mW, have been selected as the Opamps of the second integrator and adder.

D. Comparator and Flip-Flop

The delay of the comparator introduces additional loop delay to the ΣΔ Modulator [14]. The Signal-to-Quantization Noise Ratio (SQNR) of the readout is degraded by the delay of the comparator as shown in Fig. 9. The low-power comparator, TLV3202-Q1 [25], has been selected for its low delay (40 ns). To latch the output of the comparator, a single positive-edge-triggered D-type flip-flop is used. The typical delay of the flip-flop is about 6 ns.

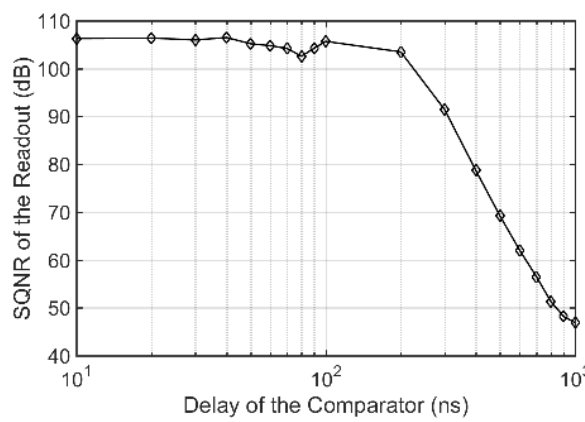


Fig. 9. Simulated SQNR of the readout vs. the delay of the comparator.

E. Other Passive Components

The second-order ΣΔ Modulator is conditionally stable. It is therefore important to keep any variations in the passive components within a range that maintains the stability of the modulator. This is easily achievable for PCB board design by selecting the right types of resistors and capacitors. Moreover, the effect of shift in the Noise Transfer Function (NTF) due to the variations in the passive components is negligible because of the high oversampling ratio.

V. EXPERIMENTAL RESULTS

A PCB-level prototype that uses COTS chips has been implemented (Fig. 10). The first integrator consists of two different Opamps (LTC6363 and THS4551) which consume 9.5 mW and 6.85 mW, respectively. The readout has been tested using an MPDP sensor with a 3.3 kΩ bridge resistance and a 400 Hz $1/f$ corner frequency. The results reported here were obtained with a supply voltage of 5 V, at which the current consumed is 2.44 mA and 1.91 mA, respectively, including the current consumed by all the active blocks in the CT ΣΔ Modulator.

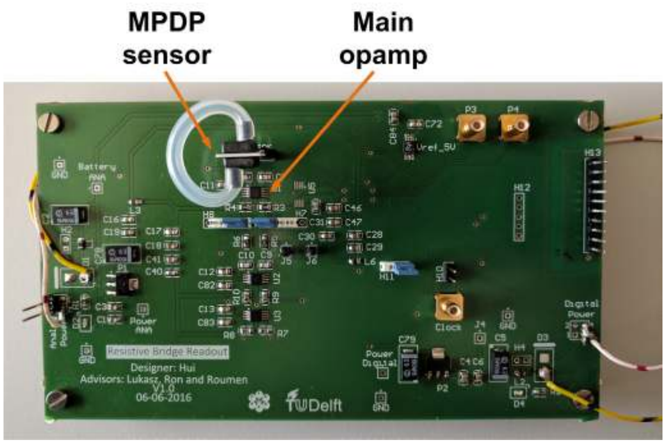


Fig. 10. Prototype of the readout based on COTS components.

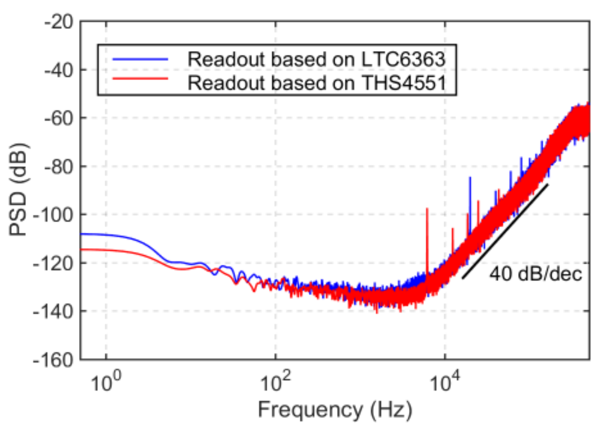


Fig. 11. FFT analysis of the bitstream of the proposed readout based on two different main Opamps.

To characterize the performance of the CT ΣΔ Modulator, the MPDP sensor is replaced by two 200 kΩ resistors. Fig. 11 shows the FFT results of the readout bitstream with two different main Opamps (LTC6363 and THS4551) at a sampling frequency of 2 MHz. It can be seen that both have -40 dB/dec noise shaping. As shown in Eq. 4, the $1/f$ noise in both cases is mainly contributed by the $1/f$ current noise of the main Opamps. The measured noise performance is in both cases in good agreement with the calculated results based on the datasheets [19, 20]. The integrated noise over 2 kHz bandwidth is 306 pA, when LTC6363 is used, and 252 pA, when THS4551 is used. Fig. 12 shows the INL measurement of the readout up to the full-scale input, which is ±5 V. The linearity is mainly limited by the offset of the main Opamp and the asymmetric PCB layout, resulting in an INL of about 95 ppm, which is at least ten times lower than the intrinsic nonlinearity of the MPDP sensor (1500 ppm).

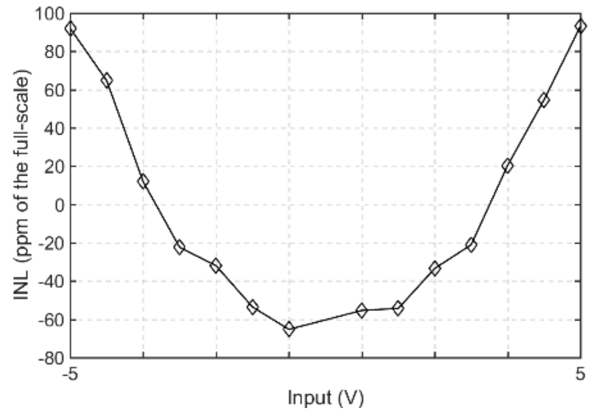


Fig. 12. Measured INL of the readout without the MPDP sensor.

The transfer characteristic is measured by applying differential pressure to the inputs of the MPDP sensor. The differential pressure is generated by a U-tube manometer filled with water, as shown in Fig. 13. The water level difference between the two legs of the manometer is manually set using a precision linear stage. Although the full-scale input pressure range of the readout with the MPDP sensor is ±1000 Pa, the maximum pressure difference that can be produced by the setup is 220 Pa because the effective travel length of the linear stage is 22 mm.

Fig. 14 shows the output of the readout, decimated by a sinc^3 filter, in response to real-time pressure steps of 10 Pa and 5 Pa within a range from -110 Pa to +110 Pa. From these measurements, the pressure transfer characteristic is obtained (Fig. 15a), showing a sensitivity of 0.1/100 Pa. Fig. 15b shows a nonlinearity in the pressure measurement of about 0.6 %, which is probably due to the non-idealities caused by the setup and the MPDP sensor.

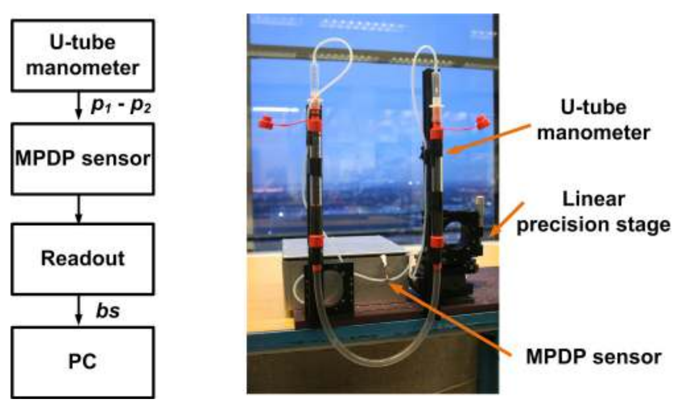


Fig. 13. Differential pressure measurement setup.

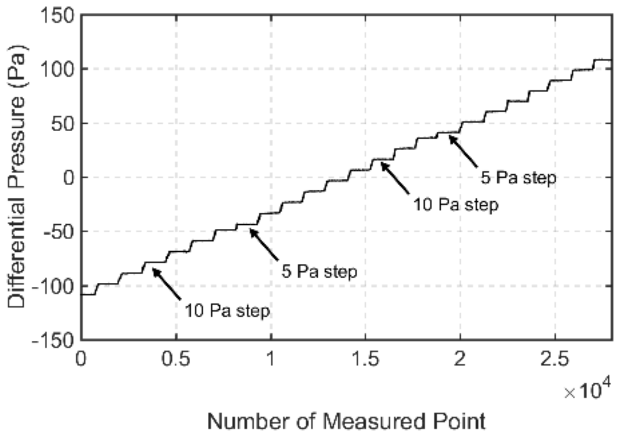


Fig. 14. Measured output of the readout in repsonse to differential pressure steps.

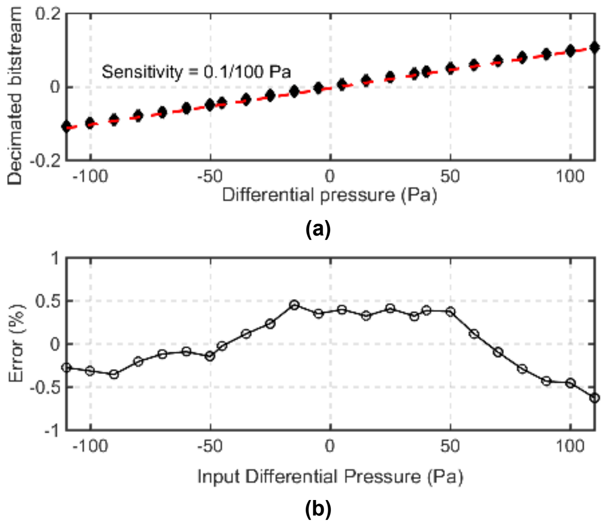


Fig. 15. (a) Measured pressure transfer characteristic and (b) nonlinearity error of the system.

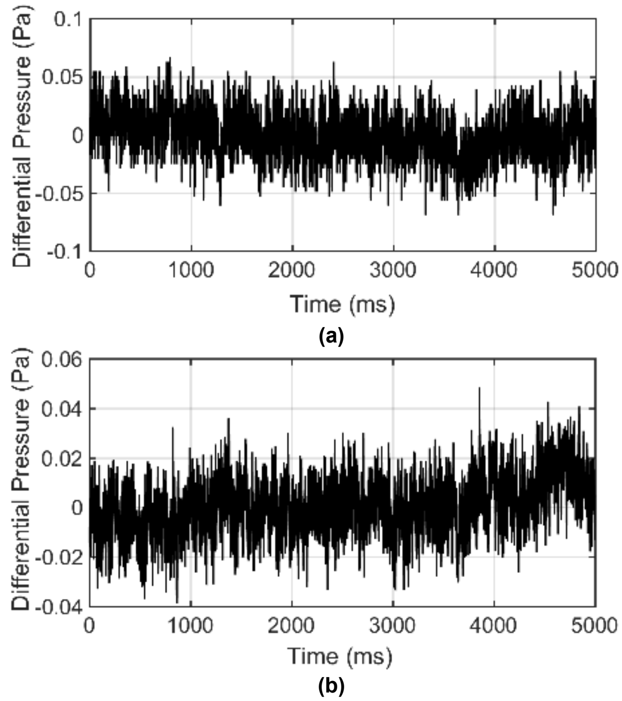


Fig. 16. Measured RMS pressure noise of the sensing system with a shorted (0 Pa) input for (a) LTC6363 and (b) THS4551.

In order to measure the resolution of the sensing system (MPDP sensor and readout), the inputs of the MPDP sensor are shorted (Fig. 13) to avoid any mechanical interference from the measurement environment. Fig. 16 shows the rms noise of the output of the system, which is obtained by calculating the standard deviation from 10000 samples for each case (LTC6363 and THS4551). The resolution of the sensing system using LTC6363 is 16.6 $\mathrm{mPa_{rms}}$ with a 0.5 ms conversion time. In the case of THS4551, the resolution is 12.7 $\mathrm{mPa_{rms}}$.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON OF RECENTLY PUBLISHED READOUT STUDIES BASED ON COTS COMPONENTS

	Output type	Readout mode	Core elements	Biasing voltage (V)	Power supply[1] (mW)	Bridge resistance (kΩ)	ENOB	Conversion time (ms)	Resolution (mΩ)
This work	Digital	Current	LTC6363 × 1	5	12.20	3.3	16.1[2]	0.5	0.47
			THS4551 × 1		9.55		16.3[2]		0.41
Design example	Analog	Current	THS4551 × 1	5	6.85[1]	3.3	- -	- -	- -
[5]	Digital	Voltage	OP07 × 2	2.5	29.17[1]	0.291	12.6	285	0.06
[11]	Analog	Current	Ad844 × 2	+/− 15	390[1]	1.08	- -	- -	1

1. Calculated based on datasheets.
2. Results were obtained by a 3.3 kΩ bridge used by discrete resistors.

In Table II, the performance of the readout is summarized and compared to several previously published readout studies and design examples of Wheatstone bridge sensors. To make a fair comparison, the power consumption of the reference voltage generators (one voltage reference is needed in our case) is not included. Compared to voltage mode readouts, the proposed readout consumes less power and achieves better resolution since only one main Opamp, which dominates the noise and the power dissipation in the readout, is required in the readout. Compared to current mode readouts with analog output (TIA-based design example), this readout directly provides digital values, which is more robust and more desirable in industrial applications, without significantly increasing the power consumption. Moreover, comparing LTC6363 and THS4551 indicates that the performance of the proposed readout can be further improved by using a better main Opamp, which may be available in the future.

VI. Conclusion

This paper presents a high-performance current-mode readout approach for MEMS Piezoresistive Differential Pressure sensors and the implementation details of a prototype. By digitizing the output signal of piezoresistive sensors embedded in a continuous-time sigma delta converter, in the current mode, the noise performance becomes dominated by a single opamp of the first integrator. Compared to conventional voltage mode readout, this approach requires fewer active input stages and thus consumes less power. Moreover, the measured results of the paper show that the performance of the readout approach can be significantly improved by using a better main Opamp. The key performance in combination with the MPDP sensor are evaluated. The prototype readout together with the MPDP sensor achieves a 12.7 $\mathrm{mPa_{rms}}$ resolution with a 0.5 ms conversion time. These features make the proposed readout approach a promising candidate for high-precision mechatronic systems.

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