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A Power-Efficient Wireless Capacitor Charging System Through an Inductive Link

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Abstract

A power-efficient wireless capacitor charging system for inductively powered applications has been presented. A bank of capacitors can be directly charged from an ac source by generating a current through a series charge injection capacitor and a capacitor charger circuit. The fixed charging current reduces energy loss in switches, while maximizing the charging efficiency. An adaptive capacitor tuner compensates for the resonant capacitance variations during charging to keep the amplitude of the ac input voltage at its peak. We have fabricated the capacitor charging system prototype in a 0.35-μm 4-metal 2-poly standard CMOS process in 2.1 mm^2 of chip area. It can charge four pairs of capacitors sequentially. While receiving 2.7-V peak ac input through a 2-MHz inductive link, the capacitor charging system can charge each pair of 1 μF capacitors up to ±2 V in 420 μs, achieving a high measured charging efficiency of 82%.

Keywords

Adaptive capacitor tuning; capacitor charger; charging efficiency; inductive power transmission

I. Introduction

Inductive power transmission across the skin is currently the only viable solution to deliver sufficient power to implantable medical devices (IMDs) without imposing size and capacity constraints of rechargeable batteries [1]. In these IMDs, large capacitors have been utilized as temporary energy sources, which supply the low-power IMDs or augment the inductive power when it is interrupted or insufficient [2], [3]. Capacitors are also used in neural stimulation by storing charge and transferring it to the tissue periodically at high efficiency [4], [5]. Therefore, it is important to rapidly charge implanted capacitors efficiently not from batteries but directly through inductive transcutaneous links, while reducing the IMD size and the risk of tissue damage from overheating.

Charging capacitors from a voltage source through a switch achieves maximum 50% efficiency, wasting half of input energy in the switch. On the other hand, charging capacitors with a current source can minimize the switching loss as the fixed charging current becomes smaller [6]. Fig. 1 shows the conventional Li-ion battery charging techniques in inductively powered devices. AC–DC converters, e.g., a rectifier or a voltage doubler, convert an ac input voltage from an inductive link to a dc supply voltage V_{DD}, resulting in ac–dc power loss [7]. In Fig. 1(a), the current source (CS) charges the capacitor directly without switches by controlling its gate voltage [8]. However, the current source still wastes energy because

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of the difference between supply and capacitor voltages $V_{DD} - V_C$. Generating an adaptive supply voltage AV_{DD} in Fig. 1(b)−keeps the dropout voltage of the current source small $AV_{DD} - V_C$, while suffering from the additional dc–dc power loss [9]. The charging system in Fig. 1(c) utilizes a back telemetry link to control the inductive power, adjusting V_{DD} depending on the V_C level to reduce the voltage drop across the current source [10]. However, it requires additional sensing and control circuits as well as an external feedback loop through an optical link.

In this brief, we propose a novel capacitor charging system, which charges a bank of capacitors efficiently with a fixed charging current, directly from an ac input voltage through an inductive link. A series charge injection capacitor following the secondary L_2C_2 tank generates a predefined charging current, like a current source, while the voltage drop across this capacitor does not dissipate power. Consequently, the fixed charging current reduces the energy loss in the charger switches, boosting the capacitor charger efficiency. The proposed system can be utilized for a power-efficient neural stimulator which efficiently charges capacitor banks and injects charge into the neural tissue periodically [5]. In the rest of this brief, Section II describes the concept and implementation of the proposed wireless capacitor charging system. Section III presents circuit details and design considerations, including an active switch driver, an adaptive capacitive tuner, and a dual-output V_{TH}-compensated rectifier. Measurement results are in Section IV, followed by conclusions in Section V.

II. System Architecture

A. Capacitor Charging Concept

The concept of the proposed capacitor charging system starts from utilizing a series charge injection capacitor as a current source, which generates a fixed amount of predefined charging current. Fig. 2 shows the simplified circuit diagram of the inductive capacitor charging system, which charges a pair of positive and negative capacitors C_P and C_N, respectively. The secondary coil L_2 and its parallel resonant capacitor C_2, which generate a coil voltage V_{COIL}, are followed by a series charge injection capacitor C_S, which provides an input voltage V_{IN} to C_P and C_N through switches SW_P and SW_N, respectively. SW_P turns on when $V_{IN} > V_{CP}$ form positive C_P charging, and SW_N turns on when $V_{IN} < V_{CN}$ for negative C_N charging with respect to the ground GND. When $V_{CN} < V_{IN} < V_{CP}$, both switches turn off, and V_{IN} follows V_{COIL}. Then, when either SW_P or SW_N turns on, the switch connects V_{IN} to a positive or negative capacitor voltage V_{CP} or V_{CN}, holding V_{IN} relatively constant and generating a fixed charging current I_{CH} through C_S. For example, when $V_{IN} > V_{CP}$, SW_P connects V_{IN} to V_{CP} to hold V_{IN} around V_{CP}, while V_{COIL} keeps increasing. Thus, the voltage variation across C_S, $V_{COIL} - V_{IN}$, generates the positive I_{CH} until V_{COIL} reaches its positive peak.When V_{COIL} starts decreasing from its peak, V_{IN} also decreases below V_{CP}, and SW_P turns off. The charging current I_{CH} can be expressed as

$$I_{CH} = C_S \times d\left(V_{COIL} - V_{IN}\right)/dt. \quad (1)$$

The I_{CH} value can be adjusted by choosing proper C_S, which will be discussed in Section II-B. Fixed I_{CH} minimizes the switch loss, while unlike a real current source, the voltage drop across C_S does not dissipate power, improving the charging efficiency from L_2 to the capacitor pair.

B. Charging Time and Efficiency Analysis

The smaller the charging current, the higher the capacitor charging efficiency and the smaller the power loss in switches, leading to longer charging time. Hence, the charging

current I_{CH} should be optimized to charge the capacitors efficiently within a desired period. We modeled the charging time and efficiency depending on I_{CH} with simplified voltage and current waveforms of the capacitor charging system in Fig. 3. In this analysis, f_c is the carrier frequency that is received via V_{COIL}, n is the number of charging cycle, and $t[n]$ is the transition time of V_{IN} when $V_{CN} < V_{IN} < V_{CP}$. In this simplified model, we assume the following: 1) V_{COIL} is sinusoidal with a constant peak voltage V_{Peak}; 2) switches turn on and off at ideal times, and V_{IN} becomes equal to V_{CP} or V_{CN} with negligible voltage drop across closed switches when connected to capacitors; 3) during each charging cycle, V_{CP} and V_{CN} are constant, and small voltage increments ΔV_{CP} and ΔV_{CN} are added to V_{CP} and V_{CN} at the end of each cycle, respectively; and 4) C_P and C_N are equal and charged by the same amount of I_{CH}, i.e., $V_{CP} = -V_{CN}$.

When V_{IN} is connected to V_{CP} or V_{CN} for charging, V_{COIL} and I_{CH} can be expressed as

$$V_{\mathrm{COIL}}(t) = V_{\mathrm{Peak}} \sin(2\pi f_c t) \quad (2)$$

$$I_{\mathrm{CH}}(t) = 2\pi f_c C_S V_{\mathrm{Peak}} \cos(2\pi f_c t). \quad (3)$$

V_{CP} at the nth charging cycle $V_{CP}[n]$ can be obtained from

$$V_{\mathrm{CP}}[n] = \sum_{i=1}^{n} \Delta V_{\mathrm{CP}}[i] \quad (4)$$

where $\Delta V_{CP}[n]$ is the V_{CP} increment at the nth charging cycle, from the initial condition of $V_{CP}[0] = V_{CN}[0] = 0$ V.

At the nth charging cycle, $t[n]$ is equal to the transition time, in which V_{IN} increases from $V_{CN}[n-1]$ to $V_{CP}[n-1]$. Therefore,

$$\begin{aligned} V_{\mathrm{CP}}[n-1] - V_{\mathrm{CN}}[n-1] &= 2V_{\mathrm{CP}}[n-1] \\ &= [V_{\mathrm{COIL}}(t)]_{\frac{n}{f_c}-\frac{1}{4f_c}+t[n]}^{\frac{n}{f_c}+\frac{1}{4f_c}} \\ &= V_{\mathrm{Peak}}[\sin(2\pi f_c t)]_{\frac{n}{f_c}-\frac{1}{4f_c}+t[n]}^{\frac{n}{f_c}+\frac{1}{4f_c}}. \end{aligned} \quad (5)$$

In (5), $t[n]$ can be written as

$$t[n] = \frac{\sin^{-1}\left(-1+\frac{2V_{\mathrm{CP}}[n-1]}{V_{\mathrm{Peak}}}\right)}{2\pi f_c} + \frac{1}{4f_c}. \quad (6)$$

With $t[n]$ in (6), $\Delta V_{CP}[n]$ can be derived as

$$\begin{aligned} \Delta V_{\mathrm{CP}}[n] &= \frac{1}{C_P}\int_{\frac{n}{f_c}-\frac{1}{4f_c}+t[n]}^{\frac{n}{f_c}+\frac{1}{4f_c}} I_{\mathrm{CH}}(t)\,dt \\ &= \frac{C_S}{C_P} V_{\mathrm{Peak}}[\sin(2\pi f_c t)]_{\frac{n}{f_c}-\frac{1}{4f_c}+t[n]}^{\frac{n}{f_c}+\frac{1}{4f_c}} \\ &= 2\frac{C_S}{C_P} V_{\mathrm{Peak}}\left(1 - \frac{V_{\mathrm{CP}}[n-1]}{V_{\mathrm{Peak}}}\right). \end{aligned} \quad (7)$$

Therefore, the charging period T_{CH} during which C_P and C_N are charged to a target charging voltage $\pm V_{TG}$ at the n_{CH}th charging cycle, can be obtained from

$$T_{CH}=\frac{n_{CH}}{f_c}, \quad \text{where} \quad V_{CP}[n_{CH}]=\sum_{i=1}^{n_{CH}}\Delta V_{CP}[i]=V_{TG}. \quad (8)$$

The total energy loss in SW_P and SW_N during n_{CH} charging cycles $E_{SW}[n_{CH}]$ can be calculated as a sum of switching energy losses in each cycle $\Delta E_{SW}[n]$

$$\Delta E_{SW}[n]=2\int_{\frac{n}{f_c}-\frac{1}{4f_c}+t[n]}^{\frac{n}{f_c}+\frac{1}{4f_c}} I_{CH}^2(t)\times R_{SW}\,dt \quad (9)$$

$$E_{SW}[n_{CH}]=\sum_{i=1}^{n_{CH}}\Delta E_{SW}[i \quad (10)$$

where R_{SW} is the switch resistance.

The capacitor charging efficiency η_{CAP} from L_2 to the C_P and C_N pair of capacitors can be expressed as

$$\eta_{CAP}=\frac{E_{CP}+E_{CN}}{E_{CP}+E_{CN}+E_{SW}[n_{CH}]+E_{SYS}} \quad (11)$$

where E_{CP} and E_{CN} are the stored energies in C_P and C_N, respectively, which are $E_{CP}=C_P V_{TG}^2/2$ and $E_{CN}=C_N V_{TG}^2/2$, respectively, and E_{SYS} is the energy consumed by the rest of the system during n_{CH} charging cycles.

Smaller I_{CH} increases T_{CH} in (4)–(8), while smaller I_{CH} and R_{SW} increase η_{CAP} in (9)–(11). Therefore, when the maximum tolerable T_{CH} is known, I_{CH} can be selected to be as small as it takes T_{CH} to charge C_P and C_N for C_S and V_{Peak} values in (3)–(8). C_S should be smaller than C_R, and $V_{Peak} > V_{TG}$.

C. Implementation of the Capacitor Charging System

The overall architecture of the proposed capacitor charging system is shown in Fig. 4. A power transmitter drives the primary coil L_1 at the designated carrier frequency f_c, which induces V_{COIL} across L_2. The capacitor charger consists of switches driven by high-speed active drivers to charge a bank of four pairs of capacitors C_P and C_N. A control unit sets a user-defined target charging voltage V_{TG} and generates a sequence signal S_{CH} to operate the four-channel capacitor charger sequentially, which can be utilized in a programmable multielectrode neural stimulation [5]. When charging, the capacitor charger connects V_{IN} to positive and negative capacitors alternately to hold V_{IN} at V_{CP} or V_{CN}, while generating the fixed charging current I_{CH} through C_S. In other words, C_S operates like a current source that does not dissipate power, while reducing the switching loss in the capacitor charger and significantly improving the charging efficiency from L_2 to the capacitor bank.

In this capacitor charging system, the secondary resonance capacitance C_R, connected across L_2, can be expressed as

$$C_R = C_2 + C_A + \frac{C_S C_{\text{Eff}}}{C_S + C_{\text{Eff}}} \quad (12)$$

where C_2 is the parallel resonant capacitor, C_A is the adaptive tuning capacitor, and C_{Eff} is the effective capacitance of the capacitor bank, which varies as the capacitor bank voltage and switching duty cycle change. An adaptive capacitor tuner compensates for C_{Eff} variations by automatically adjusting C_A to keep C_R constant. Therefore, the secondary L_2C_2 tank is maintained at resonance during charging, while maximizing V_{COIL}. After the charging cycle, an end-of-charge (EOC) signal connects V_{IN} to GND, and the adaptive capacitor tuner is deactivated, setting $C_R = C_2 + C_S$. A dual-output V_{TH}-compensated rectifier followed by low-dropout regulators generates the supply voltages V_{DD} and V_{SS} from V_{COIL}, which has little effect on the charging operation as long as the V_{COIL} amplitude is kept constant by the adaptive capacitor tuner.

III. Circuit Details and Design Considerations

Fig. 5 shows the schematics of the capacitor charger and one of its active switch drivers. In Fig. 5(a), if $V_{\text{TG}} > V_{\text{CP}}$ and S_{CH} = high, the capacitor charger starts charging the capacitor bank C_P and C_N, with EN = high. When $V_{\text{IN}} > V_{\text{CP}}$, the active switch driver DRV_P turns on the switch P_1 with V_P = low to provide the positive charging current $+I_{\text{CH}}$ to C_P with a small switch loss. Fig. 5(b) shows the active switch driver (DRV_P) in which P_2, P_3, N_2, and N_3 form a common-gate comparator, whose inputs are connected to V_{CP} and V_{IN}. Since the current drawn from V_{IN} is much smaller than the charging current, it has little effect on the charging operation. An offset block, which consists of current sources P_4 and N_4 and control switches P_5 and N_5, injects additional positive or negative offset current, depending on a feedback voltage V_F, to expedite V_O transition for fast P_1 switching, maximize the forward current delivered to the capacitor, and minimize the back current to improve the charging efficiency [11]. Since the V_O level depends on V_{IN} amplitude, which varies during charging, shoot-through limited inverters level-shift V_O to supply levels to drive P_1 with proper V_P levels. An offset reset switch N_{10}, which is driven by V_N, resets the offset by pulling V_F = low after P_1 turns off and $V_{\text{IN}} < V_{\text{CN}}$ for the next C_P charging cycle. Here, the timing of the reset signal depends on V_{IN}, which, unlike the process-dependent inverter delay in [11], is independent of process variations. DRV_N has a symmetrical structure with respect to DRV_P.

Fig. 6 shows the schematic diagram of the adaptive capacitor tuner. A dynamic bias and envelope detector sense the positive V_{COIL} amplitude and compare it to a threshold window around V_{REF} =1.2 V. If V_{COIL} is outside a designated window (2.7–2.8 V_P), UP or DN signals from comparators CMP_1 or CMP_2 trigger a 7-bit up/down counter to progressively adjust a 7-bit binary-scaled set of tuning capacitors C_A =0~127×(8 pF), between V_{COIL} and GND, to bring V_{COIL} amplitude back within this window. C_A can accommodate the capacitance variations in (12), which result from C_S (=1 nF in this system) in series with C_{Eff} as it varies with $V_{\text{CP,CN}}$. The switches for tuning capacitors P_{17} to P_{23} are driven by V_{DDH}, which is the higher voltage between V_{DD} and V_{COIL}, to ensure proper turnoff.

Fig. 7 shows the schematic diagram of the dual-output V_{TH}-compensated rectifier. V_{COIL} is converted to two half waves V_{INP} and V_{INN} to prevent overvoltage across the following transistors that constitute a positive and negative rectifier pair, generating V_{RECP} and V_{RECN}, respectively. In the positive rectifier, $V_{\text{TH}(P28)}$ of the diode-connected transistor P_{28} compensates for $V_{\text{TH}(P27)}$ of the rectifying switch P_{27}, resulting in a small voltage drop of $V_{\text{GS}(P27)} - V_{\text{GS}(P28)}$ and high ac–dc power conversion efficiency. R_4 reduces the gate voltage of P_{27} by discharging C_6 in case V_{RECP} decreases.

IV. Measurement Results

A. Chip Micrograph and Measured Waveforms

The four-channel capacitor charging system was fabricated in the TSMC 0.35-μm 4M2P n-well standard CMOS process, occupying 2.1 mm^2. Fig. 8 shows the chip micrograph and floor plan of the charging system along with the inductive powering setup. A class-E power amplifier on the transmitter side drives the primary coil (L_1 = 6.8 μH and $\varnothing_1 = 4$ cm) at 2 MHz and delivers power across a 15-mm gap to the secondary coil (L_2 = 1.2 μH and $\varnothing_2 = 1$ cm).

The waveforms in Fig. 9 show how the capacitor bank is being efficiently charged from V_{COIL}. In Fig. 9(a), the peaks of V_{IN} follow V_{CP} and V_{CN} traces during charging because the fixed charging current I_{CH} results in a small constant voltage drop across the capacitor charger switches P_1 and N_1. With $C_P = C_N = 1$ μF, each capacitor pair was charged to V_{CP} = 2 V and V_{CN} = –2 V in 420 μs when V_{COIL} = 2.7 V$_P$. Fig. 9(b) shows the active switching waveforms when $V_{CP,CN}$ = 0, ±1, and ±2 V. When $V_{IN} > V_{CP}$, P_1 turns on, holding V_{IN} to V_{CP} plus voltage drop across SW$_P$, and the voltage across C_S, $V_{COIL} - V_{IN}$, starts to increase, flowing $+I_{CH}$ into C_P. As V_{CP} increases, the switching duty cycle decreases while the slope of $V_{COIL} - V_{IN}$ remains almost the same, generating a fixed charging current.

Fig. 10 shows how the adaptive capacitor tuner compensates for the C_{Eff} variations and maintains V_{COIL} amplitude constant during charging. In Fig. 10(a), the UP signal triggers the up/down counter, automatically increasing the adaptive tuning capacitor C_A to 624 pF as V_{CP} increases. Therefore, C_A compensates for the C_{Eff} variations, and the secondary resonance capacitance C_R in (12) stays at $C_2 + C_S$ during charging, generating a relatively constant V_{COIL} with small ΔV_{COIL} = ±50 mV variations. In Fig. 10(b), where the adaptive capacitor tuner is deactivated, the V_{COIL} amplitude has dropped by 500 mV because of the resonance capacitor detuning, resulting in V_{DD} reduction and limitation of V_{CP} to only 1.8 V, instead of the 2-V target. Therefore, the adaptive capacitor tuner ensures proper charging operation with sufficient V_{COIL} amplitude against C_R detuning.

B. Capacitor Charging Time and Efficiency

Fig. 11 shows the measured, simulated, and calculated values of the capacitor charging time and efficiency, while sweeping the target charging voltage V_{TG} from ±1 to ±2 V, to verify the accuracy of our measurement as well as provide insight for further improvements. The calculated charging time and efficiency have been derived from (4)–(8) and (9)–(11) in Section II-B, respectively, with f_c = 2 MHz, C_S = 1 nF, $C_P = C_N = 1$ μF, and V_{Peak} = 2.7 V. We assumed that R_{SW} = 1.5–6 Ω depending on $V_{CP,CN}$ and the system supply power P_{SYS} = 400 μW from simulations. In Fig. 11(a), the 1-μF capacitor pair was charged up to ±2 V in 420 μs. The amount of charging current at each charging cycle gradually decreases as capacitors are charged up because V_{IN} needs longer transition time $t[n]$ in (6) before charging. Therefore, as the capacitor voltages increase, capacitors require longer charging time for the same amount of voltage increment. Shorter charging time in calculations is the result of the ideal switching of SW$_P$ and SW$_N$, regardless of $V_{CP,CN}$ levels, which also indicates the maximum possible capacitor charging efficiency.

In Fig. 11(b), the charging efficiency was defined as the stored dc energy in the capacitor bank over the total input ac energy of the capacitor charging system. The highest efficiency of 82% was measured when 1-μF capacitors were charged up to V_{TG} = ±2 V. Lower $|V_{CP,CN}$ increases R_{SW} of P_1 and N_1 switches, leading to larger switching loss and lower charging efficiency as V_{TG} decreases. Discrepancies between measured and simulated efficiencies mainly result from larger R_{SW} of the chip, which was estimated about 4–16 Ω by observing

voltage drops across switches, compared–to the simulated R_{SW} = 1.5–6 Ω. The calculated charging efficiency with R_{SW} = 4–16 Ω shows closer results to the measured efficiency. While R_{SW} can be further reduced by optimizing the switch sizes, the proposed capacitor charging system achieves a high measured charging efficiency of 63%–82% with $C_P = C_N$ = 1 μF charged up to ±1 ~ ±2 V in 132–420 μs. Table I summarized the specifications of the current inductive capacitor charging system prototype. Table II compares the estimated capacitor charging efficiencies η_{CAP} when the conventional Li-ion battery charging methods in Fig. 1 are applied to charge capacitors from 0 to 4.2 V in current source mode.

V. Conclusion

We have demonstrated a power-efficient wireless capacitor charging system for inductively powered applications. A fixed charging current generated by applying part of the coil voltage across a series charge injection capacitor charges a capacitor bank with small energy loss, improving the charging efficiency. During charging, an adaptive capacitor tuner maintains the inductive link at resonance, providing a constant coil voltage within a designated window. The charging time and efficiency of the system have also been analyzed to provide designers with better insight toward maximizing the charging efficiency for given charging time and capacitor bank values. This system is expected to improve the overall power efficiency in IMDs that utilize capacitor banks for energy storage and stimulation [5].

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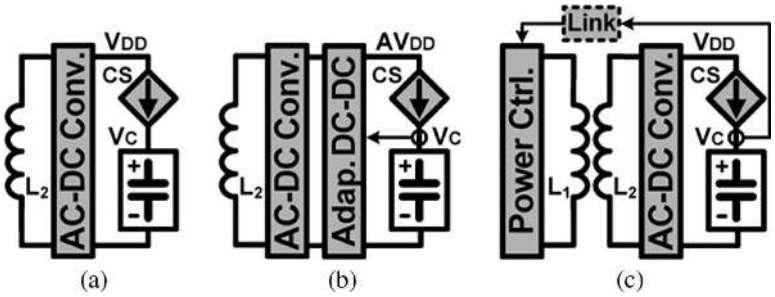

Fig. 1.

Conventional inductive Li-ion battery charging techniques in CS mode from (a) a fixed supply voltage [8], (b) an adaptive supply voltage [9], and (c) a supply voltage adjusted by an external control loop [10].

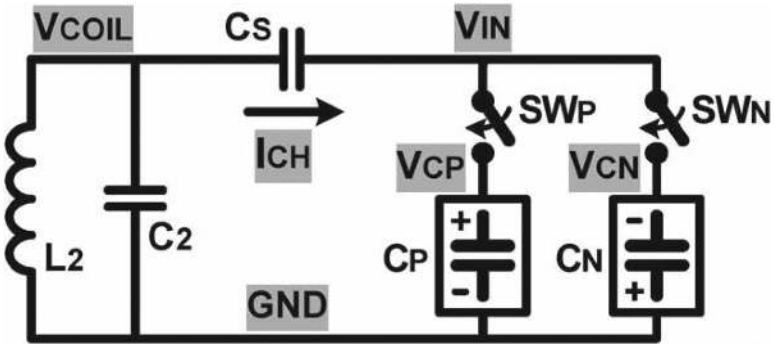

Fig. 2.
Simplified circuit diagram of the inductive capacitor charging system.

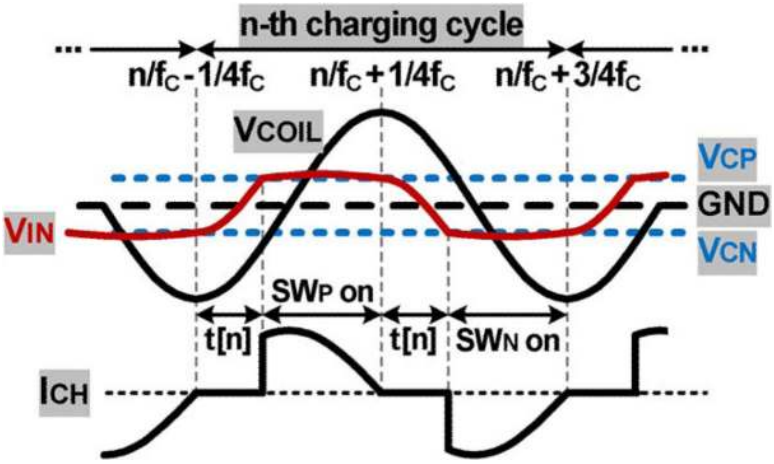

Fig. 3.
Simplified voltage and current waveforms of the capacitor charging system for modeling and theoretical analysis.

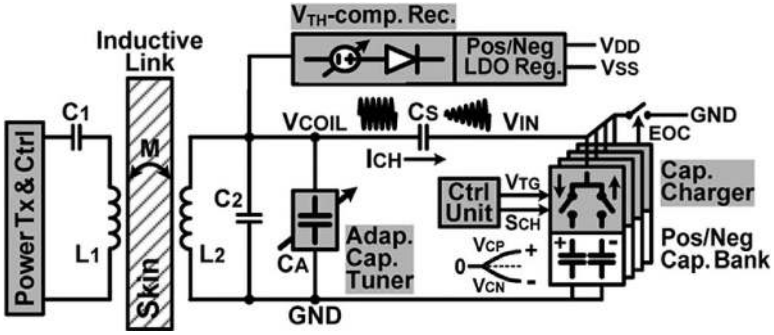

Fig. 4.
Overall architecture of the proposed power-efficient capacitor charging system through an inductive link.

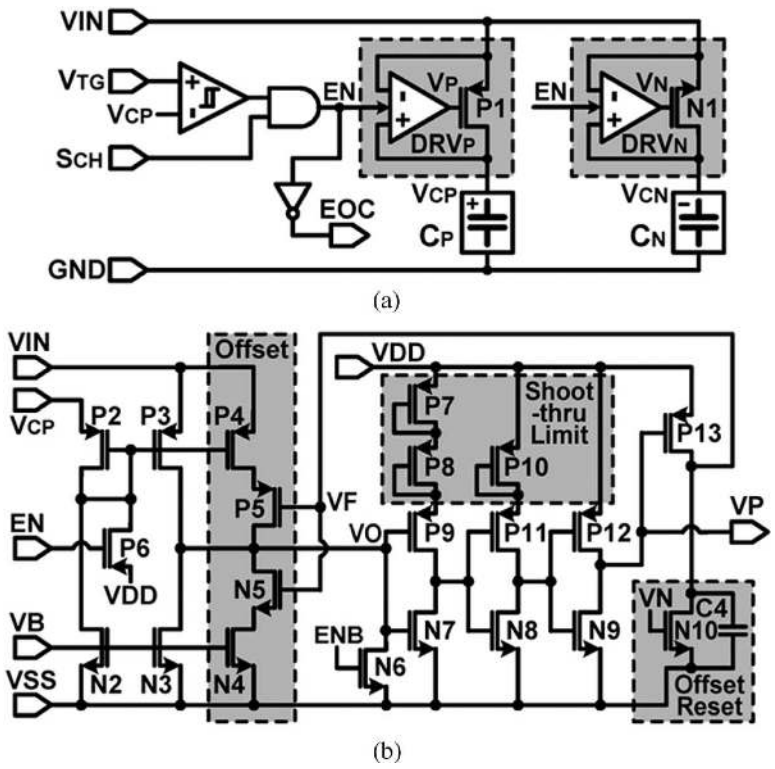

Fig. 5.
Schematic diagrams of (a) the capacitor charger and (b) one of its active switch drivers DRV_P.

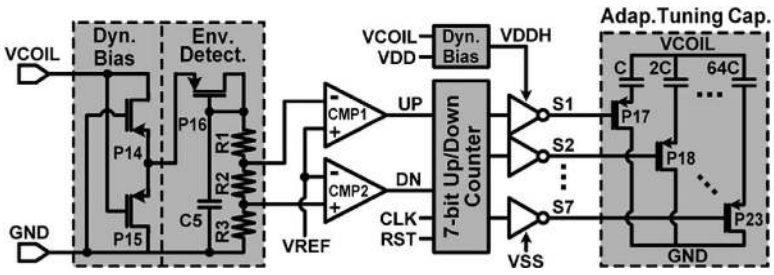

Fig. 6.
Schematic diagram of the adaptive capacitor tuner.

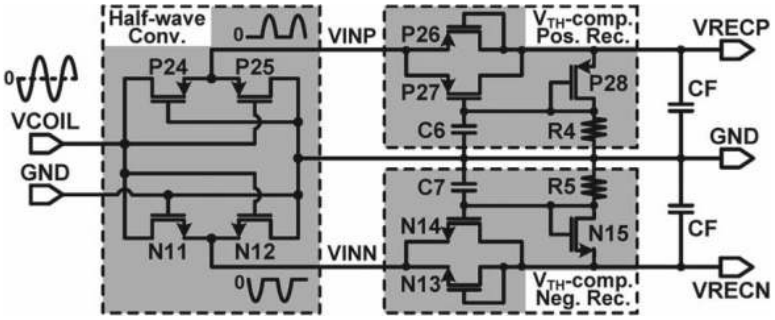

Fig. 7.
Schematic diagram of the dual-output V_{TH}-compensated rectifier.

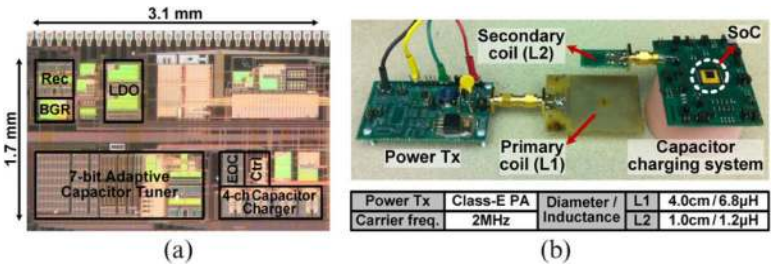

Fig. 8.
(a) Chip micrograph and (b) testing setup through an inductive link.

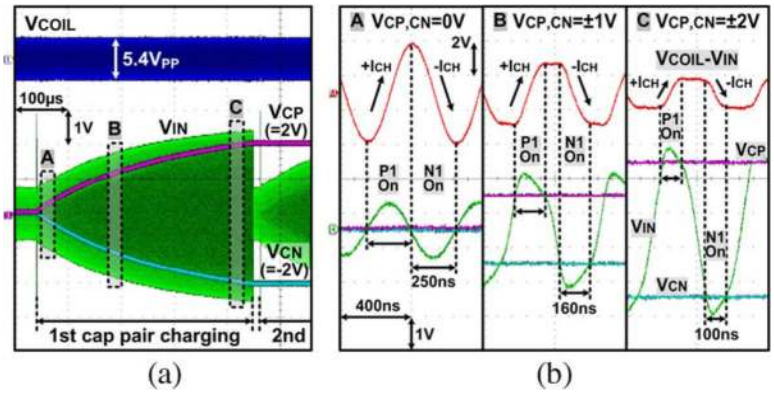

Fig. 9.

Measured waveforms of (a) the capacitor charger and (b) its zoomed-in switching as $V_{CP,CN}$ of 1-μF capacitor pairs reach ±2 V in 420 μs.

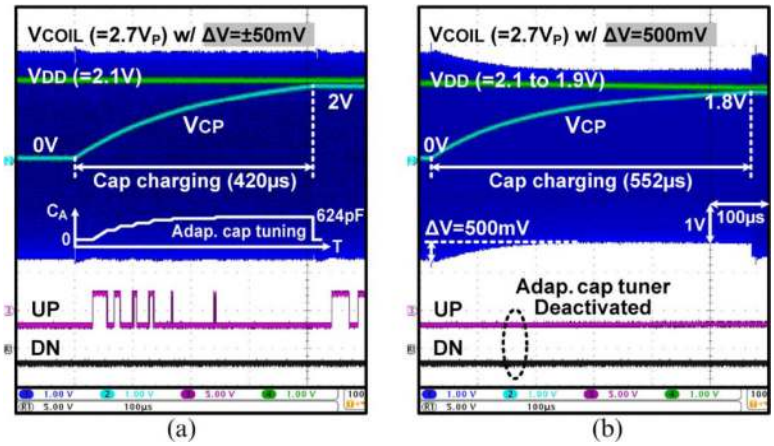

Fig. 10.

Measured waveforms of V_{COIL} and $V_{CP,CN}$ variations during capacitor charging (a) with and (b) without the adaptive capacitor tuning mechanism.

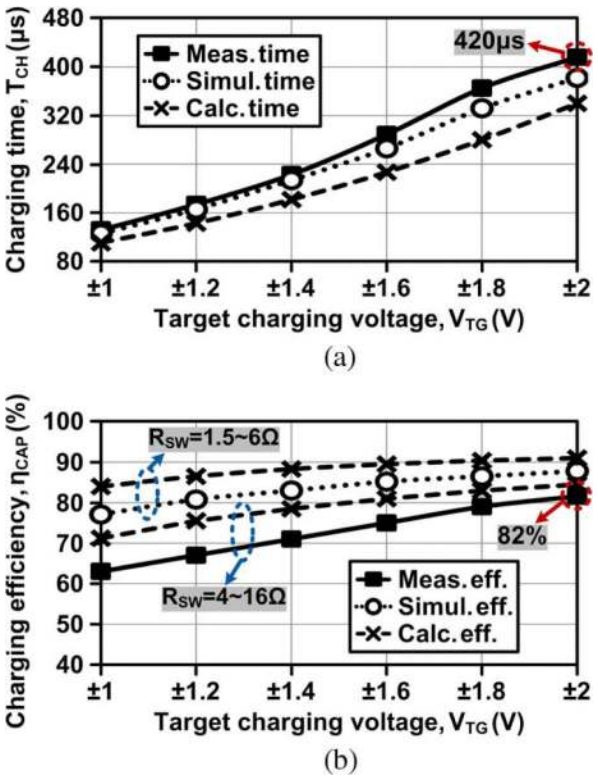

Fig. 11.

Measured, simulated, and calculated (a) capacitor charging time and (b) charging efficiency versus target charging voltage at f_c = 2 MHz, C_S = 1 nF, $C_P = C_N$ = 1 μF, and V_{Peak} = 2.7 V.

TABLE I

Capacitor Charging System Specifications

Overall System		**Capacitor Charger**	
Process	0.35 μm CMOS	# of channel	4
$L_2/C_2/C_S$	1.2μH / 4nF / 1nF	Target voltage	±1 ~ ±2 V
Carrier freq.	2 MHz	Charging off.	63 ~ 82%
Coil distance	1.5 cm	Charging time	132 ~ 420 μs
V_{coil} peak	2.7 V	C_P/C_N	1 μF / 1 μF
Area	2.1 mm^2	$P_{Supply}(Charging)$	240 μW
Rectifier / Regulator		**Adaptive Capacitor Tuner**	
V_{RECP} / V_{RECN}	2.25 V / -2.25 V	Tuning bit	7-bit
V_{DD} / V_{SS}	2.1 V / -2.1 V	Adaptive cap.	0 ~ 1024 pF
Rec. PCE	72% w/50 kΩ	P_{Static}	20 μW*

*Simulation

TABLE II

Benchmarking Capacitor Charging Efficiency

Ref.	V_C(V)	V_{DD}(V)	I_{CS}(mA)	η_{ACDC}(%)*	η_{DCDC}(%)	η_{CHG}(%)**	η_{CAP}(%)***
[8]	0~4.2	4.3	3	80	-	48.8	**39**
[9]	0~4.2	V_C+0.2	800	80	90	91.3	**65.7**
[10]	0~4.2	V_C+0.3	698	80	-	87.5	**70**
This work	0~±2	2.7V_{Peak}*AC* (V_{coil})	34 (max)	Not needed	-	82	**82**

* Power efficiency of the active rectifier in [7]

** Charger efficiency, ηCHG = avg (V_C / V_{DD})

*** $\eta CAP = \eta ACDC \times \eta DCDC \times \eta CHG$.