A Power-Optimized Widely-Tunable 5-GHz Monolithic VCO in a Digital SOI CMOS Technology on High Resistivity Substrate

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ABSTRACT
This paper describes the design and technology optimization of power-efficient monolithic VCOs with wide tuning range. Four 5-GHz LC-tank VCOs were fabricated in a 0.12-μm SOI CMOS technology that was not enhanced for RF applications. High and regular resistivity substrates were used, as were single-layer and multiple-layer copper inductors. Using a new figure-of-merit (FOM_T) that encompasses power dissipation, phase noise and tuning range, our best VCO has an FOM_T of -189 dBc/Hz. The measured frequency tuning range is 22 % and the phase noise is -126 dBc/Hz at 1 MHz offset for 4.5-GHz. Oscillation was achieved at 5.4-GHz at a minimum power consumption of 500 μW.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles – *Advanced technologies, RF Integrated Circuits*

General Terms: Design

Keywords
Low Power, SOI CMOS, RF Design, VCO, High Resistivity Substrate, Phase Noise, FOM

1. INTRODUCTION
The demand for high-speed, low-power analog technology is increasing due to emerging wireless and wired communications systems such as Bluetooth, wireless LAN, and other ISM band transceiver systems. The Bluetooth standard is intended for low-cost, short-range radio links at 1 Ms/s symbol rate, using 100 MHz signal bandwidth in the 2.4-GHz ISM band [7].

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These transceivers require monolithic integration to lower cost, and this necessitates the use of modern radio architectures such as those based on low-IF receivers or on direct conversion, as shown in Figure 1.

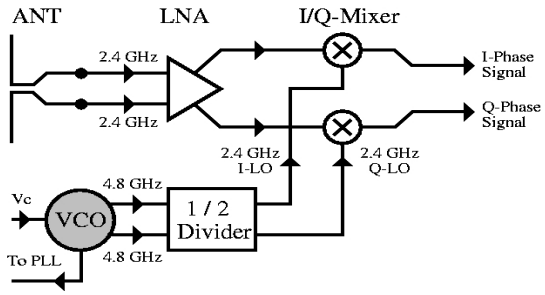


Figure 1 A 2.4-GHz ISM band receiver front-end

Such architectures require at least two local oscillator (LO) signals that are precisely orthogonal (0° phase and 90° phase) to each other. The efficient generation of these I (In-phase: 0°) and Q (Q-phase: 90°) signals is still a major subject of research in the system-on-chip (SOC) application of 2.4-GHz ISM band transceiver systems. A typical technique for achieving high I/Q phase accuracy is running an oscillator at twice the desired frequency and generating the I-signal and Q-signal through frequency division, as shown in Figure 1. The local frequency is generated by the frequency synthesizer, which includes a phase-locked loop (PLL) to stabilize the oscillating frequency.

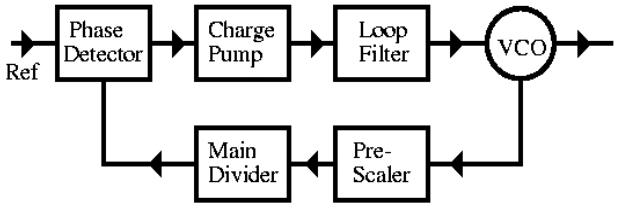


Figure 2 PLL block diagram

The PLL is composed of a phase detector, a charge pump, a loop filter, a prescaler, a main diver, and a VCO, as shown in Figure 2. The VCO is the most dissipative element in the PLL. Most

publications about VCOs focus on schemes for low phase noise and FOM [1-7]. Few papers treat power optimization, probably because previous silicon technologies have not offered the high-performance passive elements required to fully optimize analog and mixed signal circuits. In this paper, we discuss a power optimization scheme for VCOs fabricated in a 0.12-µm SOI (Silicon-on-Insulator) CMOS technology with high-quality passives that supports two different substrates: RRS (regular resistivity substrate), and HRS (high resistivity substrate) for enhancement of passives. We describe the simultaneous optimization of VCO tuning range, phase noise and figure of merit.

2. SOI CMOS TECHNOLOGY

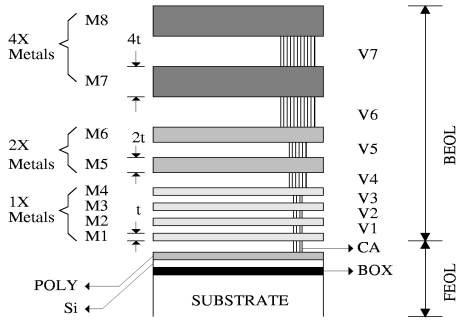


Figure 3 Cross-section of 0.12 µm SOI CMOS technology (BEOL: Back end of the line, FEOL: Front end of the line. Metal thicknesses are 4X = 1.2 µm, 2X = 0.6 µm, and 1X = 0.3 µm.)

Figure 3 shows the cross-section of the SOI CMOS technology. This technology offers eight levels of copper interconnect and the two types of substrate mentioned above: regular resistivity substrate (RRS: 10~20 Ω·cm) and high resistivity substrate (HRS: over 300 Ω·cm) [8].

3. LC-TANK VCO CIRCUIT

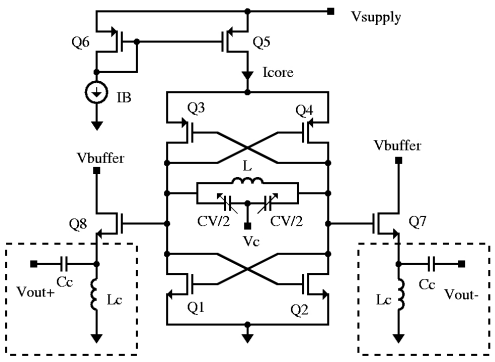


Figure 4 LC-tank VCO circuit schematic

Figure 4 shows a 5-GHz LC-tank VCO circuit. It consists of four main parts: a source of negative transconductance (g_m), an LC-tank circuit, a current source, and output buffers. The components enclosed in boxes are off-chip. We used a complementary topology to lower phase noise [10-12]. The current source is typical of those used in SOCs, and consists of a PMOS (Q_5 and Q_6) current mirror. The VCO core current (I_{core}) is controlled by the external current (I_B) through the current mirror. This current mirror degrades the phase noise because of the added noise of the current source [11], but this circuit is necessary for integration of the PLL and other circuits. In the VCO design, the complementary geometry includes NMOS (Q_1 and Q_2) and PMOS (Q_3 and Q_4), which set the DC level of the VCO output at Vsupply/2. The output buffer includes bias-tees and source followers, which have improved bandwidth due to the low diffusion capacitance of SOI technology. The LC-tank circuit is composed of an inductor (L) and two varactor capacitors ($C_V / 2$ and $C_V / 2$) for frequency tuning, as shown in Figure 4. The quality-factor (Q_{TANK}) of the LC-tank is roughly the same as the parallel combination of the inductor Q (Q_L) and the varactor Q (Q_C). Usually the inductor Q is lower and therefore dominant, because on-chip inductors typically suffer from losses in the substrate and thin wiring levels. However, Q_L can be increased through proper layout, by using thick wiring levels or multiple wiring levels in parallel, or by using a high resistivity substrate [8].

3-1. VCO Design Theory

A VCO has to fulfill the oscillation condition in order to oscillate properly. Equation 1 expresses this condition [10]:

$$g_{mDEVICE} \geq \chi \cdot g_{mTANK} \quad (1)$$

Here, $g_{mDEVICE}$ is the negative transconductance of the active device (Q_1 or Q_2), which is related to the device's aspect ratio (W/L). g_{mTANK} is the transconductance of the LC-tank at the resonant frequency. The literature [7, 10] suggests that χ, an adjustable constant, is about to 3, but based on the authors' experience with hardware, χ = 3 is too low for proper VCO operation. We recommend using a χ value of 3 to 5 during design. The power consumption of the VCO core is related to this adjustable constant. To reduce power dissipation, g_{mTANK} must be minimized so that $g_{mDEVICE}$ can be correspondingly lowered by operating at low current or low device width. The phase noise is another parameter that must be considered in VCO optimization. The phase noise is expressed in Equation 2 [13]:

$$L(\Delta\omega) = 10\log\left\{\left[1+\frac{f_0^{\,2}}{(2\Delta\omega Q)^2}\right]\left(1+\frac{\omega_0}{\Delta\omega}\right)\frac{FkT}{2P_{av}}+\frac{2kTRK_0^{\,2}}{\Delta\omega^2}\right\} \quad (2)$$

As shown in Equation 2, phase noise improves as oscillator Q (Q_{TANK}) increases, thus we can benefit from higher Q_{TANK}. Equation 2 also shows the trade-off between power dissipation and phase noise. Higher VCO gain (K_0) degrades drastically phase noise performance [13]. Frequency tuning range (FTR) is another important VCO parameter, and is directly related to the LC-tank. The oscillating frequency (fo) is expressed in Equation 3:

$$f_o = \frac{1}{2\pi\sqrt{L(C_V + \Delta C_V)}} \quad (3)$$

Here, ΔC_V is the varactor's capacitance range. Equations 2 and 3 impose a trade-off between the frequency tuning range and the phase noise. The FTR depends on the varactor characteristics as shown in Equation 4:

$$FTR \approx \frac{C_P + C_{V\,\max}}{C_P + C_{V\,\min}} \quad (4)$$

Here, C_P is the parasitic capacitance of the VCO circuit and C_V is the varactor capacitance. As shown in Equation 4, large FTR requires both a highly tunable varactor and small parasitic capacitance [10]. Accumulation MOS varactors can be used because they have a good ratio of C_{Vmax} / C_{Vmin}. The parasitic capacitances come from the active devices and the substrate capacitances of the on-chip passives. Overall, the three main VCO parameters are determined by the characteristics of the LC-tank. Therefore the LC-tank will be the focus of our optimization. Consequently, inductor is the dominant component of the resonator.

3-2. Design Strategy for Low Power

The circuit is designed to operate in current-limited regime [10] in order to use the current mirror for the bias current (I_B) with maximum efficiency.

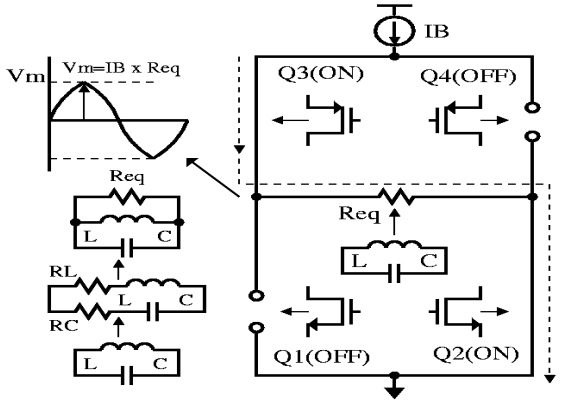
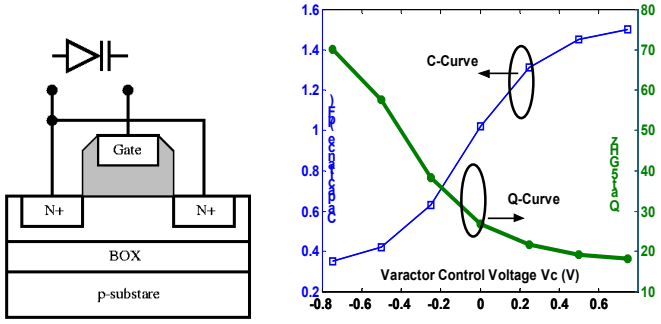


Figure 5 VCO operation schematic (We assumed Q_1 and Q_4 are off and Q_3 and Q_2 are on)

In this regime, the output differential amplitude (V_m) is approximately equal to the product between the LC-tank and the equivalent resistance as shown in Equation 5, and the current IB as shown in Figure 5.

$$R_{eq} = \frac{\omega_o L Q_L Q_C}{\omega_o^2 L C Q_L + Q_C} = \omega_o L Q_{TANK} = \frac{Q_{TANK}}{\omega_o C} \qquad (5)$$

Here, $Q_{TANK} = (Q_L // Q_C)$ and $\omega o^2 = (1/LC)$. The noise due to LC-tank losses (R_L and R_C) improves when the inductance value increases. For this reason, VCO designers tend to use large inductance values and small capacitor values. However, the minimum capacitance value is limited by the parasitic capacitance, and as the varactor capacitance decreases and parasitic capacitance remains constant, *FTR* reduces. To get a feeling for the amount of parasitic capacitance that can be tolerated, assume that the designed inductor has a moderate nominal value of 0.8 nH and further assume that the actual inductance value (L) is 10% greater than nominal value. Then the total capacitance (C) must be 1.15 pF to achieve the targeted operating frequency of 5-GHz. Since we are using a varactor with a tuning range C_{Vmax} / C_{Vmin} of about 3.5 (see Figure 6), we can tolerate about 0.8 pF of parasitic capacitance while achieving 20% tuning range and 5 GHz center frequency. This is an optimistic assumption, because it assumes oscillation is possible over the entire capacitor tuning range. The total parasitic capacitance is composed of many distributed capacitances in the inductor (L in Figure 4), the active devices (Q_1 to Q_4), and the output buffer amplifiers. We estimate its value to be about 0.4 pF. The parasitic capacitance between the VCO outputs and the output buffers is 0.16 pF (each port has 0.08 pF) due to the input capacitance of the buffer amplifiers. The remaining parasitic capacitance (0.24 pF) is from the all distributed components besides the output buffer amplifiers. The varactor capacitor is realized with an accumulation-depletion mode device whose cross section is illustrated in Figure 6 (a). Figure 6 (b) shows the capacitance and the quality-factor versus V_C, where V_C is the control voltage between gate and diffusions.



(a) **(b)**

Figure 6 (a) Cross section of accumulation-mode varactor (b) CV-curve and quality-factor versus control voltage

The varactor series resistance (R_C in Figure 5) causes the Q-factor at 5-GHz to vary from 15 to 75 as shown in Figure 6 (b). Two varactors are connected in series to allow DC decoupling of the control voltage port. The on-chip inductor of the LC-tank is laid out as a single turn of multiple metal levels strapped in parallel, and has complete symmetry [8]. In the 4 to 5-GHz frequency range the quality-factor (Q) varies from 8 to 50, depending on the number of strapped metal levels and the substrate resistivity. The loss is represented by the series resistance R_L, as shown in Figure 5. Figure 5 shows a schematic diagram of VCO operation to understand the output waveform generation. The critical performance factors are the phase noise ($L(\Delta\omega)$), the frequency tuning range (*FTR*), and the power consumption (the oscillation amplitude) [11]. The design goals for 5-GHz VCO are shown in Table 1.

Table 1 5-GHz VCO specifications

Regime	Items	Specification
I	fo	5-GHz
I	Tuning range	Over 15 %
I	Phase noise	-115 dBc/Hz @ 1MHz
I	Output power	Min. -8 dBm
I	Power consumption	Below 12 mW
II	Inductance / Q	0.8 nH / Min. 20
II	Varactor capacitor / Q	1.5 pF / Min. 40
II	*gmdevice* (W/L)	> 5·*gmtank*
II	Current source	Current mirror

To meet the specifications, a good understanding of how these performance factors is correlated together.

$$V_m = I_B \cdot R_{eq} \approx I_B \cdot (\omega_0 \cdot L \cdot Q_{TANK}) \qquad (6)$$

The oscillation amplitude (V_m) can be obtained by Equation 6. g_{mTANK} can be also computed by Equation 7 and the higher Q_{TANK} can reduce g_{mTANK}.

$$g_{mTANK} = \frac{1}{R_{eq}} = \frac{1}{(\omega_0 \cdot L \cdot Q_{Tank})} \quad (7)$$

The phase noise of an LC-tank oscillator can be estimated by Equation 8 [11].

$$L(\Delta\omega) = \frac{kT}{I_B{}^2 Q_{TANK}{}^2} \cdot \left(\frac{\omega_0}{2\Delta\omega}\right)^2 \cdot \left(\frac{2}{3} g_{mB} + g_{mc} + \frac{2}{3} g_{m0}\sqrt{\alpha}\right) \quad (8)$$

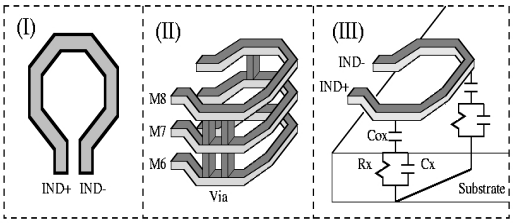
Here, g_{mB} and g_{m0} are the transconductance of the bias current source and the nominal transconductance of the switching transistors and α is the duty cycle of the switching transistor. The transconductance parts of Equation 8 can be estimated to be about $2 \cdot g_{mc}$ and Equation 8 can be rewritten as Equation 9.

$$L(\Delta\omega) = \frac{kT}{2 I_0{}^2 Q_{TANK}{}^3 (\omega_0 L)} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 \quad (9)$$

We can deduce low power design strategies for a LC-tank VCO based on the above equations.

- ***Strategy I:*** The LC-tank must be composed of a large inductor and a small capacitor since a large inductance can generate a large amplitude and low phase noise, as seen in Equations 6 and 9. However, lowering the capacitance reduces the frequency tuning range. Therefore, there is a trade-off between power consumption and tuning range.
- ***Strategy II:*** The capacitance value is directly related to the inductance value, and any increase in inductance demands a decrease in capacitance. However, the minimum capacitance value is limited by parasitic capacitances. Therefore the tuning range specification, shown in Table 1, fixes both the inductance and capacitance. The only way to maintain the phase noise is to increase the Q of the tank, as shown in Equation 9.
- ***Strategy III:*** Equation 9 shows how power dissipation and Q can be traded off at fixed phase noise. The current *Io* can be reduced by a factor of 5 if Q is increased by a factor of 2.9.
- ***Strategy IV:*** The active devices (Q_1 to Q_4) as shown in Figure 1 must be sized properly to avoid adding too much noise current. According to Equation 1, $g_{mDEVICE}$ should be about 3 to 5 times higher than g_{mTANK}.

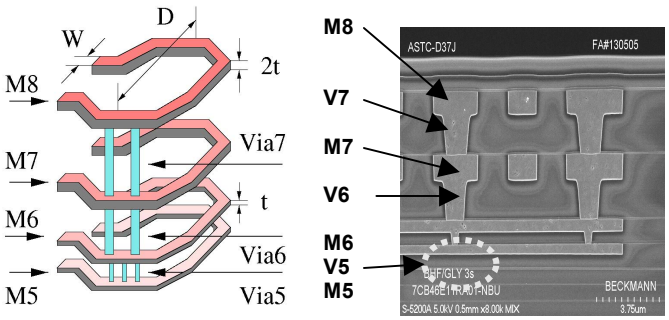
3-3. High-Q On-chip Inductor Design



(a) (b) (c)

Figure 7 Inductor design for maximizing Q on SOI: (a) Geometry scheme for Q-boosting and layout issue (b) Multi-metal layers for decrease DC-resistance (c) High resistivity substrate (HRS)

In carrying out the above strategies, the most important task is to design the on-chip high-Q inductor. Three important design aspects are diagramed in Figure 7 [8]. The first aspect is inductor geometry, which must be compatible with the overall circuit geometry [7]. The second aspect is the metal stacking scheme. To achieve highest Q at the expense of wafer area, a single turn of multiple layers strapped in parallel ("STP" type [8]) is the best design point.



(a) (b)

Figure 8 Inductor geometry and parallel metal stack (a) 3-Dimensional view (b) cross-section view

A diagram of an STP inductor, showing its single turn of multiple levels strapped together, is shown in Figure 8. This scheme improves metal conductance, which is further enhanced by the use of copper [8, 9]. We stacked up to 4 metals, M8 to M5, to obtain high Q. The vias V5-V7, serve as the contacts between metal layers, as shown in Figures 3 and 8.

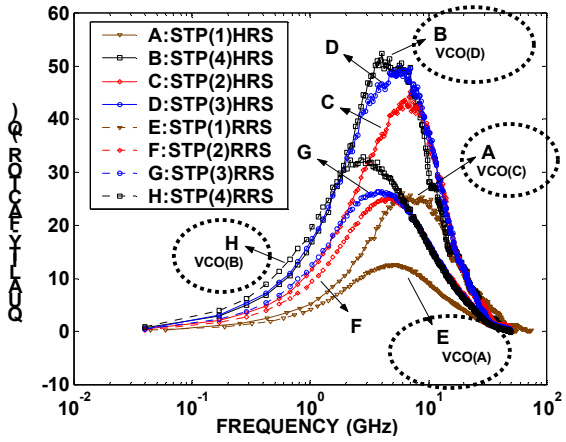


Figure 8 Measured Q of the STP inductors (The number in parenthesis refers to the number of metal levels in parallel; "2" refers to M7 and M8, "3" to M6, M7 and M8, etc.)

Figure 8 shows the measured quality-factor (Q) of the STP inductors. As the number of metal levels increases, the peak Q increases, but the self-resonant frequency (fo) decreases due to the increasing capacitance between the bottom metal layer and the substrate. HRS boosts inductor Q by at least 50 % by reducing substrate losses. The highest Q obtained is about 52 at 5-GHz with a 4-level STP inductor on HRS.

4. TEST VEHICLES

We designed 4 different VCOs to evaluate the performance due to different inductor combination. The VCOs are classified into 4 different types as shown in table 2.

Table 2 VCO types (VCO-I: STP1L with RRS, VCO-II: STP4L with RRS, VCO-III: STP1L with HRS, and VCO-IV: STP4L with HRS)

TYPE	VCO-I	VCO-II	VCO-III	VCO-IV
Inductor	STP1L	STP4L	STP1L	STP4L
L (nH)	0.8	0.8	0.8	0.8
Q	11	30	22	52
C (pF)	1.3	1.3	1.3	1.3
Substrate	RRS	RRS	HRS	HRS

VCO-I and VCO-II are fabricated on RRS while VCO-III and VCO-IV are fabricated on HRS. VCO-I and VCO-III and VCO-II and VCO-IV are identical except for the substrate resistance. VCO-I and VCO-III contain an STP1L inductor which is single turn of the top metal level only. VCO-II and VCO-IV contain an STP4L inductor which is single turn of the top four layers in parallel.

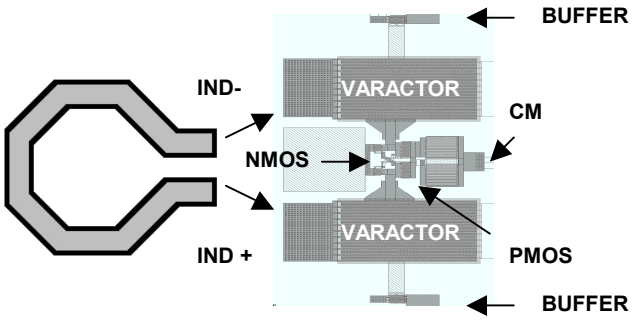
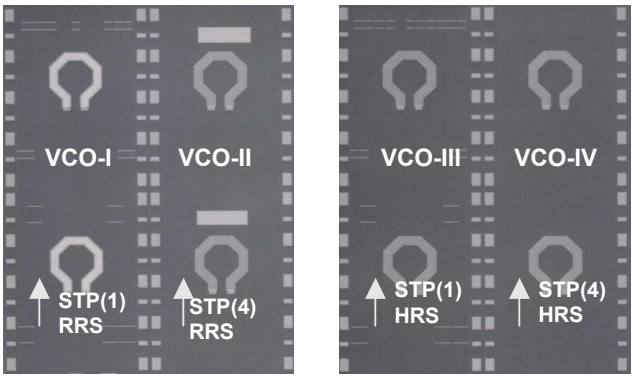


Figure 9 VCO core layout view (IND + and IND – are the ports of the on-chip inductor).

Figure 9 shows the VCO core layout view. The inductor shape must be symmetric structure to connect to the terminals "IND+" and "IND-". It can be seen that the inductor shape dominates the VCO core circuit layout. Figure 10 shows microphotographs of the four different types of LC-tank VCOs.



(a) (b)

Figure 10 Microphotographs of 5-GHz VCO test set (a) With RRS substrate (b) With HRS substrate

5. MEASUREMENT RESULTS

Figure 11 shows phase noise measurement at 1MHz offset frequency versus different core currents (I_{core}).

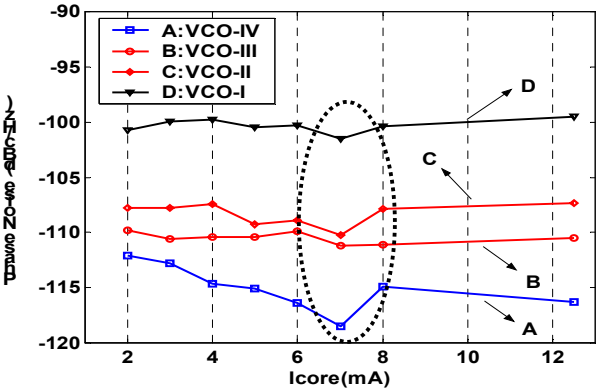


Figure 11 Phase noise measurement results at 1MHz offset frequency versus I_{core}.

Phase noise differences are 8 dB, 9 dB, and 18 dB for the comparison of test vehicles at I_{core} of 7 mA. Figure 12 shows frequency tuning range for I_{core} currents of 3 mA and 7 mA versus control voltage (V_C). The maximum deviation of frequency tuning range is 3 % for highest value of 25 % and lowest value of 22 %.

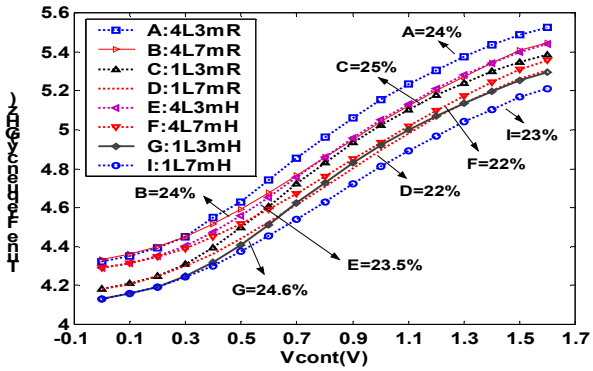


Figure 12 Tuning range versus control voltage with different I_{core} currents (Notation: 4L3mR means 4-metal layers inductor, I_{core} of 3 mA, and based on RRS and 1L7mH means single layer inductor, I_{core} of 7 mA, and based on HRS).

Phase noise and frequency tuning range are both critical VCO specifications and these are closely correlated to each other. Therefore, to evaluate VCO performance with phase noise and power consumption as well as frequency tuning range (*FTR*), we propose a new figure-of-merit (FOM_T) as shown in Equation 10.

$$FOM_T = L(\Delta\omega) - 20\cdot\log\left(\left(\frac{\omega_0}{\Delta\omega}\right)\cdot\left(\frac{FTR}{10}\right)\right) + 10\cdot\log\left(\frac{P_{diss}}{1mW}\right) \quad (10)$$

In Equation 10, $L(\Delta\omega)$ is measured phase noise. The second term of the right hand side of Equation 10 is added to *FTR* for fair comparison. The third term of the right hand side of Equation 10 is also included to consider the power consumption. Figure 13 shows *FOM* and FOM_T versus I_{core} currents. Figure 14 shows the best phase noise result with supply voltage of 2.2 V and I_{core} of 9 mA.

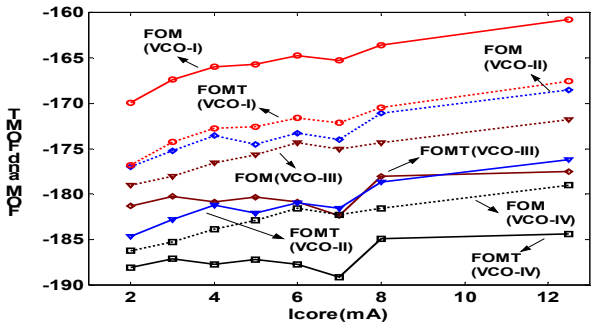


Figure 13 FOM and FOM_T versus I_{core} currents

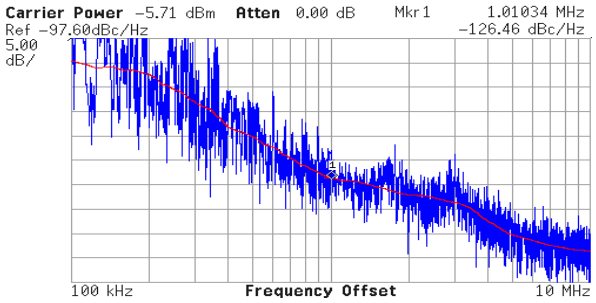


Figure 14 Measured phase noise with the best set-up (Test vehicle is with VCO-IV type and power consumption is 20 mW.)

Table 3 summarizes a comparison of the presented VCO with other published 5-GHz VCOs. The proposed test vehicles are considerably better in terms of tuning range and phase noise.

Table 3 Comparison with published 5-GHz VCO

[R]	Tech	FTR (%)	Phase Noise (dBc/Hz)	Power (mW)	FOM (dBc/Hz)	FOM_T (dBc/Hz)
[1]	CMOS	6%	-90.5	13 mW	**-153.3**	**-148.9**
[2]	Bipolar	7%	-95.5	30 mW	**-154.7**	**-151.6**
[3]	SiGe	12%	-118	15 mW	**-180.7**	**-181.8**
[4]	CMOS	7%	-101	5 mW	**-167.9**	**-164.8**
[5]	SiGe	3%	-103	40 mW	**-161.9**	**-150.5**
[6]	CMOS	4%	-110	11 mW	**-173.5**	**-165.6**
[7]	CMOS	18%	-114	14 mW	**-176.5**	**-181.6**
I	SOI(R)	22%	-101	10 mW	**-164.9**	**-171.8**
II	SOI(R)	24%	-110	10 mW	**-173.9**	**-181.6**
III	SOI(H)	23%	-111	10 mW	**-174.9**	**-182.2**
IV	SOI(H)	22%	-119	10 mW	**-182.9**	**-189.8**

(I: VCO-I type, II: VCO-II type, III: VCO-III type, and IV: VCO-IV type)

Summarizing measured data, the VCO test vehicle with higher on-chip inductor Q has better performance than others because LC-tank Q is optimized to follow the low power strategies.

6. CONCLUSION

Design strategies for a 5-GHz LC-tank VCO oriented low power scheme were discussed and test vehicles to prove these proposals were fabricated in a 0.12 μm SOI CMOS technology. The test vehicle (VCO-IV) with highest inductor Q (Peak Q = 52 at 5-GHz with STP(4) based on HRS) has frequency tuning range of 22 %, phase noise of -119 dBc/Hz, and FOM_T of -189. To boost LC-tank Q with STP(4)HRS, VCO-IV has better phase noise and figure-of-merit than other test vehicles. The quality-factor of the on-chip inductor can be increased dramatically through multi-metal layers stacking to decrease DC resistance and HRS to decrease the substrate effect. We proved that the inductor Q can improve the phase noise of VCO and decrease power consumption to achieve the phase noise specification.

7. ACKNOWLEDGEMENT

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8. REFERENCES

[1] C. Lam and B. Razavi, "A 2.6-GHz/5.2-GHz CMOS Voltage Controlled Oscillator," ISSCC Digest of Technical Papers, pp. 402-403, Feb. 1999.

[2] S. Loo, B. G. Colpitts, "Fully-integrated bipolar differential VCOs at 2.95 and 5.7 GHz," Proceedings of IEEE 2000 Canadian Conference on Electrical and Computer Engineering, vol. 2, pp. 797-801, 2000.

[3] J. Plouchart, H. Ainspan, M. Soyuer, "A fully-monolithic SiGe differential Voltage-Controlled Oscillator for 5 GHz wireless applications," Proceedings of IEEE 2000 RFIC Symposium, pp. 57-60, 2000.

[4] H. R. Rategh and T. H. Lee, "A CMOS frequency synthesizer with an injection locked frequency divider for a 5 GHz Wireless LAN receiver," IEEE Journal of Solid-State Circuits, vol. 35, no. 5, pp. 780-787, May 2000.

[5] G. Gtau, U. Langman, W. Winkler, D. Knoll, J. Osten, and K. Pressel, "A current-folded up-conversion mixer and VCO with center-tapped inductor in a SiGe-HBT technology for 5 GHz Wireless LAN applications," IEEE Journal of Solid-State Circuits, vol. 35, no. 9, pp. 1345-1352, Sep. 2000.

[6] P. Kinget, "A fully integrated 2.7 V 0.35 μm CMOS VCO for 5 GHz wireless applications," ISSCC Digest of Technical Papers pp. 226-227, Feb. 1998.

[7] C. Samori, S. Levantino, "A -94 dBc/Hz@100 kHz, fully-integrated, 5 GHz, CMOS VCO with 18 % tuning range for Bluetooth applications," Proc. of IEEE 2001 Custom Integrated Circuits Conference, pp. 201-203, 2001.

[8] J. Kim, J. Plouchart, N. Zamdmer, "High-performance Three-Dimensional On-chip Inductors in SOI CMOS Technology for Monolithic RF Circuits Applications," IEEE RFIC Symposium, June 2003.

[9] N. Zamdmer, JO. Plouchart, J. Kim, "Suitability of Scaled SOI for High-Frequency Analog Circuits," IEEE ESSDER., pp. 511-514, Sep. 2002.

[10] M. Hershenson, A. Hajimiri, and T. Lee, "Design and optimization of LC oscillators," Digest of Technical Papers, IEEE/ACM International Conference, pp. 65-69, 1999.

[11] Dirk Pfaff and Qiuting Huang, "A Quarter-Micron CMOS, 1 GHz VCO/Prescaler-Set for Very Low Power Application," Proc. of IEEE 1999 Custom Integrated Circuits Conference, pp. 649-652, 1999.

[12] J. Rael and A. Abidi, "Physical Processes of Phase Noise in Differential LC Oscillators," Proc. of IEEE 2000 Custom Integrated Circuits Conference, pp. 569-571, 2000.