A PRACTICAL FLOATING-GATE MULLER-C ELEMENT USING νMOS THRESHOLD GATES

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Abstract:

This paper presents the rationale for νMOS-based realizations of digital circuits when logic design techniques based on threshold logic gates (TGs) are used. Some practical problems in the νMOS implementation of threshold gates have been identified and solved. The feasibility and versatility of the proposed technique as well as its potential as a low-cost design technique for CMOS technologies have been shown by experimental results from a multi-input Muller C-element. The proposed new realization exhibits better performance related to delay, area and power consumption than the traditional logic implementation.

I. Introduction

Neuron MOS (νMOS) transistor principle [1] has been identified as one of the most promising ways to realize ultra large logic circuits [2-5], because the enhancement in the functional capability of an elemental transistor makes it very effective in reducing the complexity of the total circuit. The νMOS transistor has a buried floating polysilicon gate and a number of input polysilicon gates that couple capacitively to the floating gate [1-3]. The voltage of the floating

gate becomes a weighted sum of the voltages in the input gates, and hence, is this sum which controls the current in the transistor channel.

Logic design techniques for implementation of νMOS circuits have been carried out by Shibata [2,3], but their usefulness is limited because, in general, it leads to complex circuit configurations which require handling 2^n logic states for an *n*-input logic function. This imposes stringent constraints on process tolerances, not realizable by present technologies for even a relative small *n*.

A different and more powerful approach for the logic design takes advantage of the fact that the functionality of νMOS circuits is closely related to that of a threshold logic gate (TG) [5, 14]. The existence of logic design techniques which use TGs as building blocks [6, 7, 8] eases the synthesis of complex functions. Threshold logic gates have *n* two-valued inputs $x_1, x_2, \ldots, x_n$ and a single two-valued output, *y*. They are defined by *n*+1 real numbers: threshold *T* and weights $w_1, w_2, \ldots, w_n$, where weight w_i is associated with variable x_i. The input-output relation of a threshold gate is defined as $y=1$ *iff* $\sum_{i=1}^{n} w_i x_i \geq T$ and $y=0$ otherwise. Sum and product are the conventional, rather than the logical, operations. The set of weights and threshold can be denoted in a more compact vector notation way by $[w_1, w_2, \ldots, w_n; T]$.

In this paper we report on a working νMOS-based logic circuit specifically devised to validate the design approach using νMOS-based TGs. The paper is organized as follows. Section II describes the implementation of TGs with νMOS transistors, first at a theoretical level and then, discussing practical considerations. The design and experimental results for an 8 input Muller C-element are given in Section III, and finally, some conclusions are discussed in Section IV.

II. νMOS Implementation of Threshold Gates

A) Theoretical background

The most simple νMOS-based threshold gate (νMOS-TG) is the complementary inverter using both *p*- and *n*-type νMOS devices. A schematic of this TG is shown in Fig. 1. It consists

in a floating gate, which is common to both the PMOS and the NMOS transistors, and a number of input gates (V_{x1}, V_{x2}, ..., V_{xn}), corresponding to the threshold gate inputs plus an extra input (indicated by Vc in the figure) for logic threshold adjustment as will be explained later. Without using the extra control input, and assuming the charge in the floating gate is zero, the voltage in the floating gate is given by $V_F = \left(\sum_{i=1}^{n} C_i V_{xi} \right) / C_{tot}$, where C_i is the coupling capacitance between the *i*-th input and the floating gate, and C_{tot} is the total capacitance, including the parasitic capacitances at the floating gate C_c, $C_{tot} = \sum_{i=1}^{n} C_i + C_c$. As V_F becomes higher than the inverter threshold voltage, V_{TH}, the output switches to logic 1.

A CMOS TG has digital entries, i.e., $V_{xi} = x_i V_{DD}$, where V_{DD} is the power supply and $x_i \in \{0, 1\}$. A relation between the expression for V_F and that of the definition of the TG can be established as the weighted summation in the TG, $\sum_{i=1}^{n} w_i x_i$, is implemented by the capacitive network in the νMOS device, $\left(\sum_{i=1}^{n} C_i x_i V_{DD} \right) / C_{tot}$. The weight for each input is proportional to the ratio between the corresponding input capacitance C_i and C_{tot} ($w_i = C_i V_{DD} / C_{tot}$). Thus, design involves mapping the logical inequalities $\sum_{i=1}^{n} w_i x_i \geq T$ and $\sum_{i=1}^{n} w_i x_i < T$ to the electrical relations $\left(\sum_{i=1}^{n} C_i x_i V_{DD} \right) / C_{tot} > V_{TH}$ and $\left(\sum_{i=1}^{n} C_i x_i V_{DD} \right) / C_{tot} < V_{TH}$ through capacitance sizing and tuning of the threshold voltage of the inverter.

When logical threshold *T* is not centred (i.e., *T* is far from $\left(\sum_{i=1}^{n} w_i \right) / 2$), the threshold voltage of the inverter would have to be also non centred (near 0 or V_{DD}). This can be achieved using extra inputs. For example, let us assume a single control input with capacitance $C_{Control}$. If *Vc* is applied to this control input, the new V_F is:

$$V_F = \left(\sum_{i=1}^{n} C_i x_i V_{DD} \right) / C_{tot} + (C_{Control} Vc) / C_{tot}$$

where $C_{tot} = \sum_{i=1}^{n} C_i + C_c + C_{Control}$

From the point of view of the TG a comparison is performed between $\left(\sum_{i=1}^{n} C_i x_i V_{DD}\right)/C_{tot}$ and $V_{TH} - (C_{Control} Vc)/C_{tot}$. Thus, the effective threshold voltage of the inverter has been modified. In practical digital design analog voltages are avoided and so the role of the analog extra input *Vc* is realized by a set of digital inputs with the appropriate coupling capacitances.

Clearly, practical design requires considering second order effects not included for simplicity in the above expressions. The main issue for the circuit in Fig. 1 is related with the coupling effect produced when switching on the power supply. Transistor capacitances C_{fd} (between floating gate and drain) and C_{fs} (between floating gate and source) are responsible for these couplings which introduce additional terms in V_F. Sizing of input capacitors and transistors should be performed on the basis of reducing these extra terms, or also of adequately controlling the effective inverter threshold voltage. In addition, there could be parasitic charge in the floating gate after fabrication and it is obvious that the circuit operation is sensitive to it. For this effect, UV erasure is recommended.

B) Practical design aspects

Beside the theoretical background for the realization of TGs with νMOS devices, practical design and implementation of these gates require taking into account and solving the following issues.

a) *Signal regeneration*. Clearly these TGs exhibit reduced noise margins as a consequence of the electrical operation of the circuit. On the other hand, some input combinations can produce output voltages different from *VDD* or ground. These two considerations are specially critical when logic networks are built up interconnecting νMOS-TGs. Thus the inverter *I* in Figure 1 should be seen as an inverting signal regeneration stage.

b) *Electrical simulation*. During the design phase, electrical simulations for validation must be performed, and hence, good models for floating-gate MOSFETs should be used. Since man-

ufacters do not provide these models, techniques to simulate floating gate devices with standard MOS models must be devised. Other of the difficulties in simulating floating gate devices relies on the inability of the simulator to converge when floating nodes exist. An initial operating point of the circuit must be introduced. Previous approaches for this problem are given in [9, 10]. They use an additional network formed by resistors and VCVSs (Voltage Controlled Voltage Sources) to establish the initial floating-gate voltage value. The main problem of these approaches is that an operation point is previously determined to fix the value of the voltages at the VCVS control terminals. Those values are then assumed constant for all the rest of the circuit operation. This last is not completely correct because of the nonlinear relationship between the floating-gate voltage and the voltages in the other device terminals (drain, source), depending on the transistor operation region. The simple procedure we have devised [11] overcomes the above problem. It is based on performing a transient analysis which starts with all the power supplies and circuit inputs set to zero. Thus, initial condition for the floating-gate voltage provided to the simulator is zero. Afterwards, in the same transient analysis, power and inputs are set to their values. The stationary state reached provides the correct initial operation which can be used for the rest of simulations. In order to illustrate the accuracy of our method the circuit shown in Fig. 2(a) has been designed and fabricated. It consists of two cascaded inverters. The first one is implemented using νMOS devices and the second is a conventional logic CMOS inverter for signal regeneration. The circuit has two inputs *Vin* and *Vc* with equal coupling capacitances (C=70fF). It behaves like an inverter with input *Vin* and threshold voltage varying with *Vc*. Both inverters are equally sized. In Fig. 2(b), one of the simulations performed for obtaining the transfer characteristics for nodes V_{out1} and V_{out} is shown to illustrate our simulation approach. Notice that the initial value of V_F is provided by the simulator taking into account all the parasitic coupling effects. Figure 3 compares the experimental measurements obtained after UV erasure with the simulation results obtained following our technique and the approach in [9]. Input-output char-

acteristics for different values of *Vc* (0, 1, 2, 3, 4 and 5 volts) are shown. Agreement between simulation with our technique (Figure 3a) and experimental (Figure 3c) is observed. However the results obtained with the technique in [9] (Figure 3b) differ from the experimental ones since the simulated threshold voltages of the inverter appear shifted to the right. The feasibility of the proposed simulation technique to analog circuits has been also experimentally verified [11].

III. Application Example: A Multi-Input Muller C-element

A Muller C-element (where the C stands for concurrence) is a circuit widely used in the design of self-timing circuits to perform the function "*and*" of events (transitions $1\rightarrow0$ or $0\rightarrow1$). Its output is made equal to the value of input after all the input reach the same value; otherwise, the output remains the same. It has been proven [12] that an *m*-input Muller C-element can be implemented using a single threshold gate with (*m*+1) inputs, and the simplest solution is obtained when the primary inputs have an associated weight of 1, the (*m*+1)-th input (the feedback input) is affected by a weight of (*m*-1), and the threshold of the TG is *m*, as shown in Figure 4a.

The complexity of this logic element is high enough for serving as a good demonstrator of the feasibility of the proposed design approach based on νMOS-TG. On one hand, it shows that a complex functionality can be implemented by a single inverter. On the other, the existence of a feedback loop with a high associated weight (*m*-1) allows testing the signal regeneration capability that would guarantee the correct operation of threshold networks.

Figure 4b depicts the νMOS realization we propose for the logic diagram shown in Figure 4, when *m*= 8. This circuit has been designed and fabricated in an 0.8μm double poly CMOS technology. Operation under process and ambient parameters has been validated through extensive HSPICE simulations of the extracted circuit including Monte Carlo simulations and simulations using different standard worst case device parameters. Figure 5 shows the responses obtained in the laboratory. Waveform at the bottom trace is the circuit output and the remain-

ing waveforms correspond to the circuit signal inputs. Notice that operation is correct. This correct operation has been observed in the laboratory with the supply voltage down to 3V.

For comparison purposes we have also designed and laid-out a conventional 8 input Muller C-element following the structure proposed in [13] which has been shown to be very efficient. Table I compares the area, time performance and power consumption of both Muller C-elements.

IV *Conclusions*

We have exploited the relationship between the νMOS transistor principle and the threshold gate concept. On its basis a new νMOS realization for multi-input Muller C-elements has been proposed and its feasibility demonstrated with an eight input Muller C-element working in silicon. Compared to a conventional gate-based implementation, the νMOS design is very efficient. It occupies half the area than its conventional counterpart, exhibits better time performance and consumes significantly less power. In addition, an electrical simulation technique for floating gate devices has been described and its accuracy has been proven experimentally.

References

1 T. Shibata, T. Ohmi, "A functional MOS transistor featuring gate level weighted sum and threshold operations", *IEEE J. Solid-State Circ.*, vol. 39, pp. 1444-1445, 1992.

2 -------, "Neuron MOS binary-logic integrated circuits- Part I: Design fundamentals and soft-hardware-logic circuit implementations", *IEEE Trans. Electron Devices*, vol. 40, pp. 570-576, 1993

3 -------,"Neuron MOS binary-logic integrated circuits- Part II: Simplifying techniques of Circuit Configuration and their Practical Applications", *IEEE Trans. Electron Devices*, vol. 40, pp. 974-979, 1993.

4 W. Weber, et al., “On the application of the Neuron MOS Transistor Principle for Modern VLSI Design”, *IEEE Tran. Electron Devices*, vol. 43, No. 10, pp. 1700-1708, October 1996.

5 K.F. Goser, C. Pacha, A. Kanstein, and M.L. Rossmann, “Aspects of Systems and Circuits for Nanoelectronics”, *Proc. of the IEEE*, Vol. 85, No. 4, pp. 558-573.

6 S. Muroga, *Threshold Logic & its Applications*, New York: John Wiley & Sons, 1971.

7 A. L. Oliveira and A. Sangiovanni-Vincentelli, LSAT- An Algorithm for the Synthesis of Two Level Threshold Gate Networks, *Proc Int. Conf. on Computer Aided Design*, pp. 130-133, 1991.

8 K. Siu and V.P. Roychowdhury, An Optimal-depth Threshold Circuit for Multiplication and Related Problems, *SIAM Journal of Discrete Mathematics*, **7**, (2): 284-292, 1994

9 J. Ramirez-Angulo, G. Gonzalez-Altamirano and S.C. Choi, “Modeling Multiple-Input Floating-Gate Transistors for Analog Signal Processing”, *IEEE Int. Symp. on Circuits and Systems*, pp. 2020-2023, 1997.

10 L. Yin, S.H.K. Embabi and E. Sánchez-Sinencio, “A Floating-Gate MOSFET D/A Converter”, IEEE International Symposium on Circuits and Systems, pp. 409-412, 1997.

11 E. Rodriguez-Villegas “Working with FGMOS”, Internal Report, Instituto de Microelectronica de Sevilla, IMSE-CNM, 1998.

12 J.M. Quintana, M.J. Avedillo, A. Rueda y S. Baena, “Practical Low-Cost CMOS realization of Complex Logic Functions”, *Proc. of European Conf. on Circuit Theory and Design*, ECCTD’95, pp. 51-54.

13 T.-Y. Wuu and S.B.K. Vrudhula, “A Design of a Fast and Area Efficient Multi-Input Muller C-element”, *IEEE Trans. on VLSI Systems*, vol. 1, no. 2, pp. 215-219, June 1993.

14 M.J. Avedillo, J.M. Quintana, and A. Rueda, “Threshold Logic”, *Wiley Encyclopedia of Electrical and Electronics Engineering*, J.G. Webster, *Ed*., Vol. 22, pp. 178-190, 1999.

Captions to the Figures:

Figure 1: vMOS threshold gate schematic

Figure 2: a) Floating-gate CMOS inverter with threshold control;

b) Transient simulation performed to obtain transfer characteristic of circuit in Figure 2a for Vc = 3V

Figure 3: Simulation and experimental input-output characteristics for the circuit in Fig. 2a:

a) Simulation results with our technique;

b) Simulation results with the technique in [9];

c) Experimental results

Figure 4: a) Threshold-gate-based m-input Muller C-element realization;

b)Electrical diagram of vMOS-based 8 input Muller C-element

Figure 5: Experimental waveforms of vMOS-based 8 input Muller C-element

Captions to the Tables:

Table I: Performance parameters for vMOS and conventional 8-input Muller C-elements

FIGURES

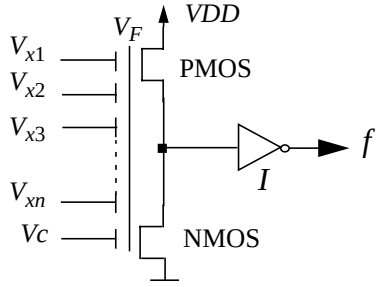

Figure 1

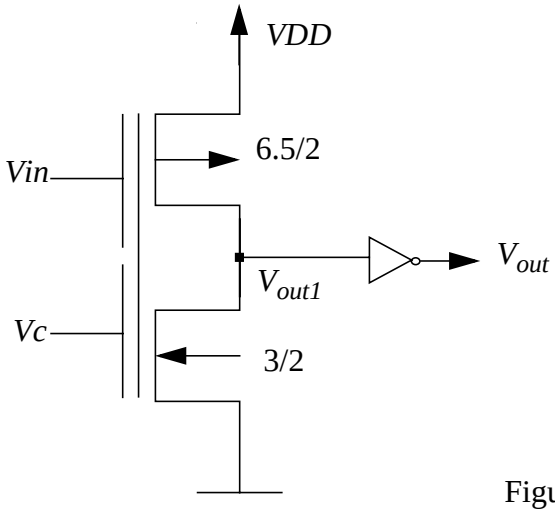

Figure 2a

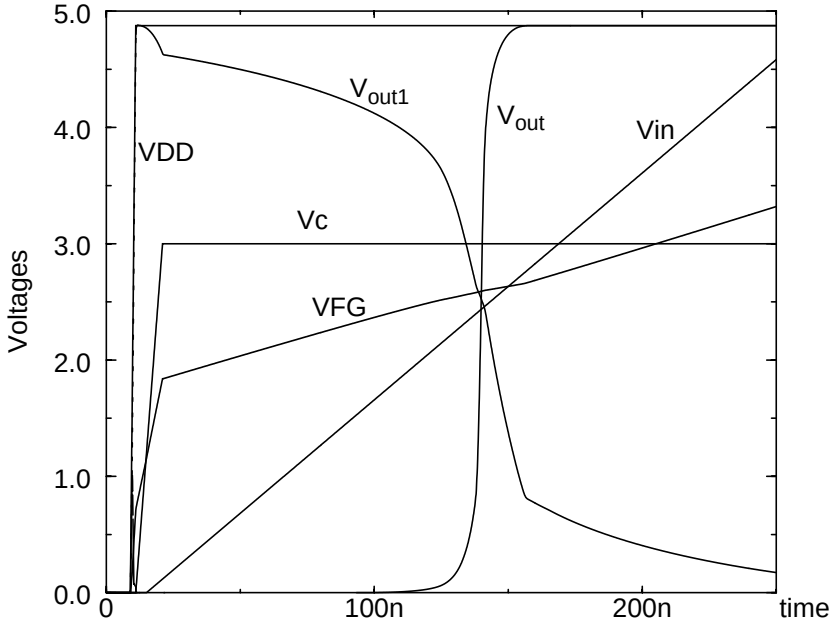

Figure 2b

	area	worst case delay	power consumption (@100MHz)
νMOS	4927 μm^2	1.8 ns	0.03 mw
conventional	9942 μm^2	3.2 ns	0.54 mw

Table 1:

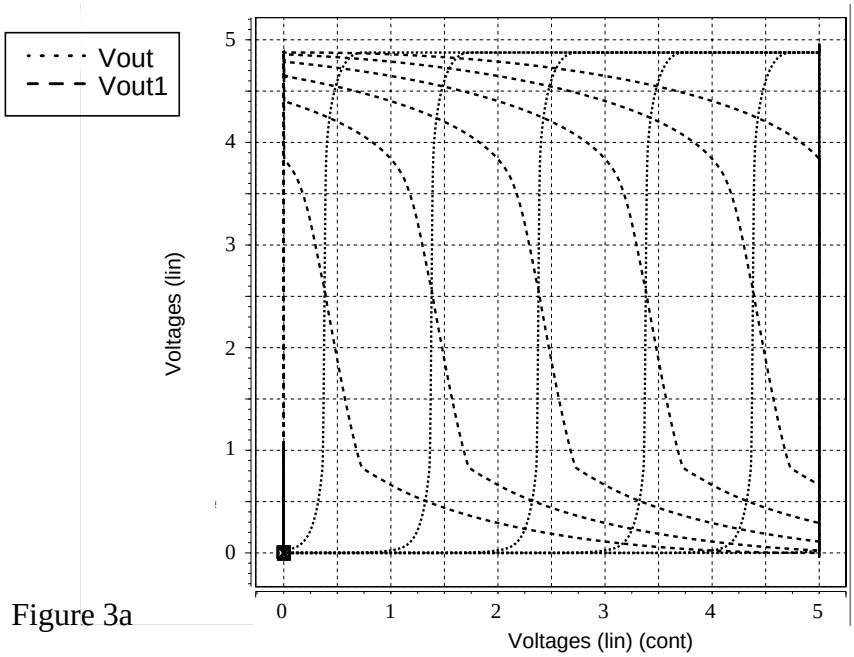

Figure 3a

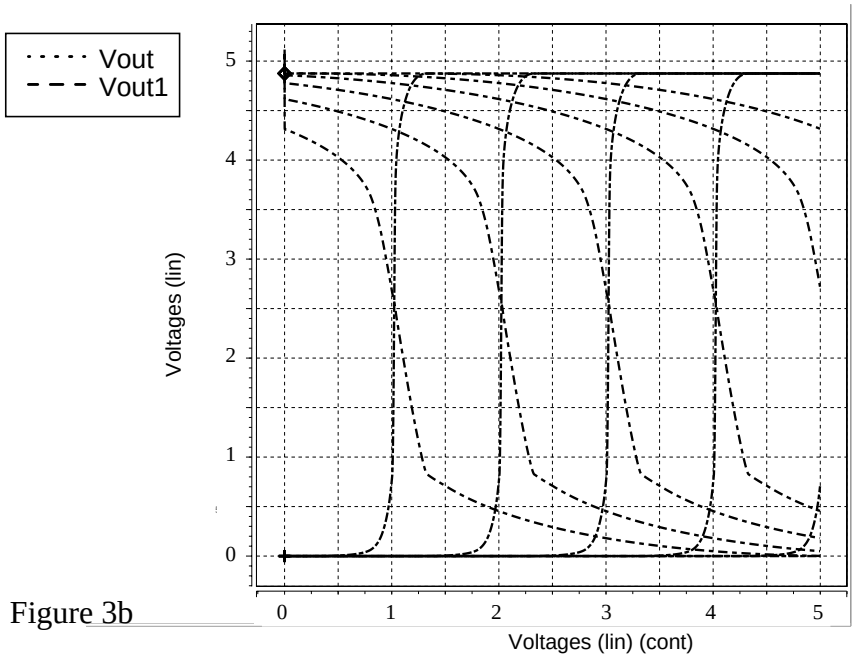

Figure 3b

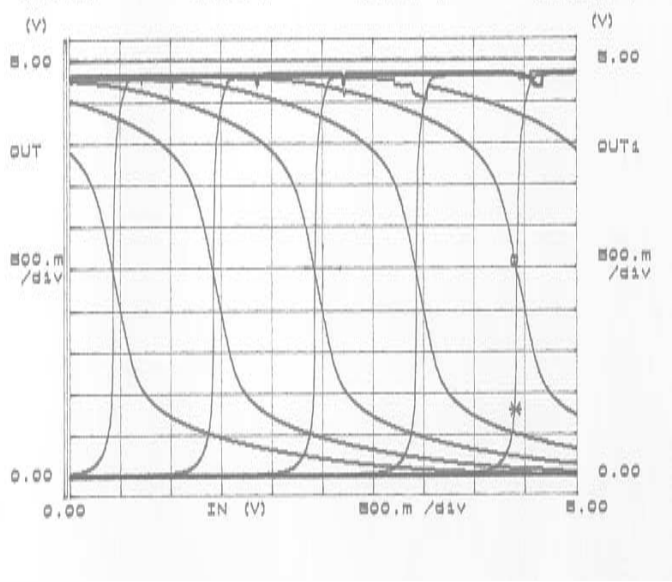

Figure 3c

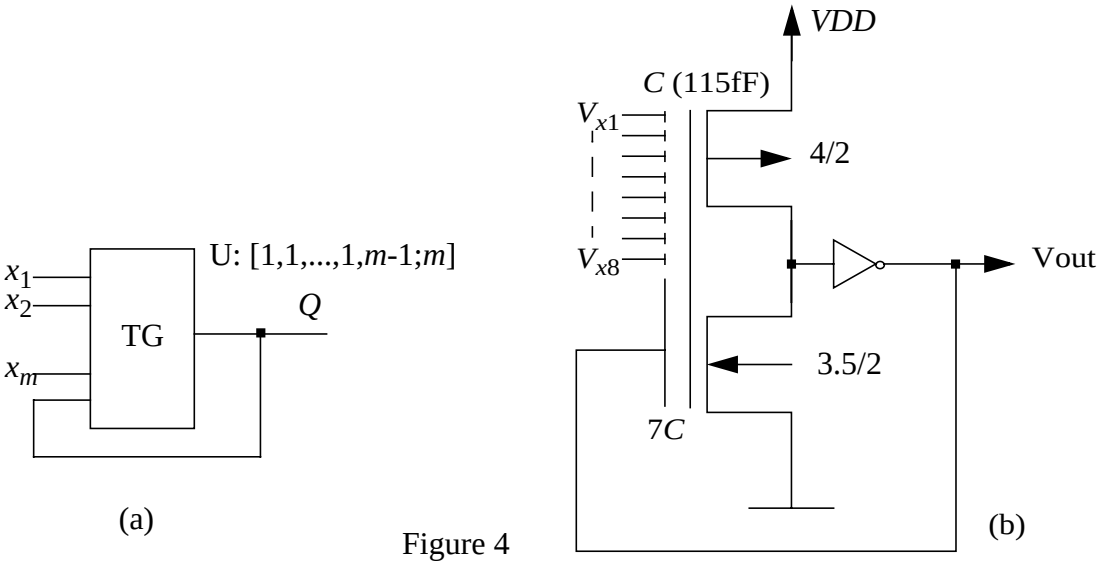

Figure 4

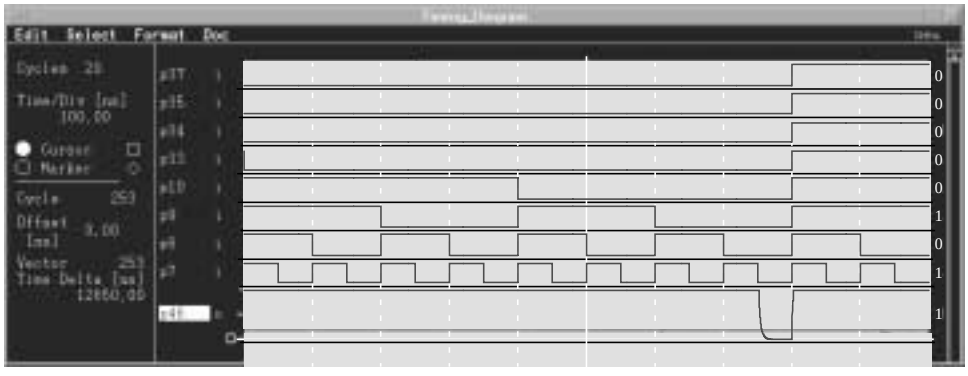

Figure 5