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A practical guide for the fabrication of microfluidic devices using glass and silicon

Ciprian Iliescu,^{1,a)} Hayden Taylor,^{2,3,a)} Marioara Avram,⁴ Jianmin Miao,² and Sami Franssila⁵

¹*Institute of Bioengineering and Nanotechnology, 31 Biopolis Way, The Nanos #04-01, 138669, Singapore*

²*School of Mechanical and Aerospace Engineering, Nanyang Technological University, 50 Nanyang Avenue, 639798, Singapore*

³*Singapore–MIT Alliance for Research and Technology, 3 Science Drive 2, 117543, Singapore*

⁴*National Institute for Research and Development in Microtechnologies, Bucharest, Romania*

⁵*Department of Materials Science and Engineering, School of Science and Technology, Aalto University, FI-00076 Aalto, Finland*

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This paper describes the main protocols that are used for fabricating microfluidic devices from glass and silicon. Methods for micropatterning glass and silicon are surveyed, and their limitations are discussed. Bonding methods that can be used for joining these materials are summarized and key process parameters are indicated. The paper also outlines techniques for forming electrical connections between microfluidic devices and external circuits. A framework is proposed for the synthesis of a complete glass/silicon device fabrication flow. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.3689939>]

I. WHY USE SILICON AND GLASS IN MICRO- AND NANO-FLUIDIC APPLICATIONS?

Micro- and nano-fluidic technology continues to be embraced by biologists,^{1–3} chemists,⁴ and engineers throughout academia and industry. As its applications have expanded, there has been an explosion in the range of materials and processes used to fabricate these devices. The earliest microfluidic devices (e.g., gas⁵ and liquid⁶ chromatography devices) were made from silicon and glass and borrowed processes directly from semiconductor and microelectromechanical systems (MEMS) manufacturing.⁷ Now, however, many researchers have moved away from silicon and glass, and instead use cast elastomers such as polydimethylsiloxane (PDMS)—which is ideal for swift prototyping—or thermoplastic polymers, which can be hot-embossed or injection-molded and are well suited to inexpensive manufacturing. Yet, there remain many applications where glass and silicon offer advantages over polymeric materials. In this paper, we highlight these advantages and offer a framework for selecting fabrication processes when using silicon and glass.

A. The dominance of soft lithography

Over the last decade, PDMS has become virtually the default material for forming microfluidic devices,⁸ because of the sheer ease with which it can be cast on to a micro-scale mould and then strongly bonded to glass.⁹ The elastomeric nature of the material has been exploited to integrate fluidic valves and pumps on-chip and has simplified the production of multi-layer devices because the soft layers readily conform to each other.^{10,11} Yet, the low stiffness (usually <1 MPa) of PDMS relative to amorphous thermoplastics, silicon, and glass has its own

^{a)}Authors to whom correspondence should be addressed. Electronic addresses: ciliescu@ibn.a-star.edu.sg and hkt@ntu.edu.sg.

drawbacks. High aspect-ratio channels are notoriously difficult to fabricate in PDMS because of their propensity to collapse.¹² Moreover, difficulties in automating the handling of such a soft material have hampered efforts to scale up PDMS device manufacturing. Meanwhile, PDMS's high oxygen and water permeabilities have proved both a blessing and a curse in different applications.

The hydrophobic nature of PDMS can be an important consideration for some biological applications. In drug screening applications, for example, hydrophobic drugs as well as metabolites (urea or albumin) can be absorbed into the device's material due to hydrophobic–hydrophobic interactions. Moreover, the limited repeatability of the PDMS fabrication process remains a big challenge that makes the material more suitable for research labs than for industrial applications.¹³

Alternative elastomers for microfluidics include off-stoichiometric thiol-ene (OSTE)¹⁴ and thermoplastic elastomers.¹⁵ Compared with PDMS, these materials allow a wider range of property tailoring (e.g., stiffness and permeability) and potentially faster processing.

B. Exploration of alternative polymeric materials

Attention has turned in recent years to harder, less permeable, and amorphous thermoplastic polymers that can be micro-embossed or injection-moulded—such as polymethylmethacrylate (PMMA), polycarbonate, and cyclic olefin (co)polymers.¹⁶ Injection moulding tooling costs are high—\$20k–30k is typical—and, therefore, short production runs are expensive, even compared to silicon and glass processing. For hot micro-embossing, meanwhile, cheaper masters can be used, but the cycle time of embossing is slower: often 5–10 min vs. 5–10 s for injection moulding.

Amorphous polymers can form features with higher depth-to-width aspect ratios than are possible with PDMS. Moreover, because of the higher stiffness of thermoplastics, channels of a given aspect ratio are more collapse-resistant than those made from PDMS. Thermoplastics, however, do not lend themselves as well as PDMS to making multi-layer devices or to the integration of valves and membranes. The robust integration of electrodes with both PDMS and thermoplastic devices remains a challenge: metal films deposited on flexible substrates are highly susceptible to fracture. Although thermoplastic fabrication technologies are very promising, the production of devices using these materials is still at an early stage of development.

The negative-tone epoxy photoresist SU-8 has also been widely used in microfluidics. SU-8 is simple to pattern by photolithography,¹⁷ can readily be bonded to itself,¹⁸ and offers a reasonable combination of mechanical strength and chemical tolerance. For example, the mechanical properties of SU-8 have been exploited to make check valves.¹⁹ Its surface properties have been exploited to make capillary electrophoresis chips.²⁰ Its ease of precise patterning has enabled the fabrication of electrospray tips.²¹ Its good thermal stability and compatibility with electrode integration have enabled its use in polymerase chain reactors.²²

More recently, paper and woven fabrics have emerged as inexpensive substrate materials for simple fluidic devices.²³ Sub-millimeter channel structures can be defined on paper by the printing of hydrophobic (e.g., wax) patterns.

C. The remaining advantages of silicon and glass

Certain micro- and nano-fluidic applications demand high temperature resilience (e.g., for chemical synthesis⁴), the precise definition of nano-scale channels or pores,^{24,25} high aspect ratio structures (usually up to 20:1), the integration of electrodes, or even integration with electronic circuits. In these cases, the higher costs of materials, energy, and capital equipment involved in silicon or glass processing may be warranted.

In some applications, the high thermal conductivity of silicon is of use in ensuring a uniform temperature distribution.²⁶ In contrast, when thermally insulating substrates like glass are used, large temperature gradients can be generated. One special benefit of silicon is the ability to fabricate thin membranes, which reduce thermal mass and enable high temperature ramp-rates.²⁷ Meanwhile, the mechanical properties of silicon have been exploited to fabricate pumps²⁸ and valves,²⁹ and in

making complex 3D structures, for example nebulizer chips,³⁰ microreactors,²⁷ cell growth chambers,³¹ and electrospray tips.³² Glass has been used in applications ranging from capillary electrophoresis³³ to polymerase chain reactions (PCR)³⁴ and to gas chromatographs.³⁵

Hybrid silicon–glass, silicon–polymer, or glass–polymer devices can be made, but the differences in material properties need to be understood. For example, in a comparison of capillary electrophoresis chips made of single materials vs. bonded dissimilar materials, the single-material devices performed better.³⁶

In this article, we detail the advantages offered by glass and silicon and suggest a framework for selecting fabrication processes. We also describe key considerations for designing a glass and/or silicon process flow.

II. DEVICE DESIGN APPROACHES

In fabricating a glass and/or silicon device, three basic approaches can be taken: *surface micromachining*, *buried-channel* techniques, and *bulk micromachining*.

In surface micromachining, a sacrificial layer is patterned to define the desired fluidic channels, a structural layer is deposited, and the sacrificial layer is then etched away. Surface micromachining offers greater potential for making multi-layer devices than does bulk micromachining, but involves more process steps per layer. A number of promising surface-micromachined microfluidic devices have been reported (e.g., Refs. 37 and 38). Surface micromachining is particularly attractive for the fabrication of nano-channels³⁹ because the thickness of the sacrificial layer, and hence the final channel height, can generally be controlled during deposition or growth within a few nanometres. Bulk micromachining cannot offer such precise control of channel height because of spatial etch-rate variations.

In buried-channel technology, a deep, vertical access trench is etched into silicon by anisotropic deep reactive ion etching (DRIE), its sidewalls are passivated by chemical vapour deposition (CVD), and a circular channel is then etched isotropically, centred on the bottom of the access trench.^{40,41} This technology works best when very deep, narrow access features are used, necessitating micron-scale lithography and high aspect-ratio DRIE. More recently, a variant of the technique has emerged in which isotropic DRIE is used to etch bulk silicon beneath a perforated silicon nitride mask, and CVD then seals the access holes in the mask.⁴² Unlike traditional surface micromachining, the silicon bulk itself is used as a sort of sacrificial layer and the channel height can be many micrometers. The mechanical stability of the thin-film roof is a limitation in some applications.

The most prevalent fabrication approach, however, is bulk micromachining, in which micro- and nano-fluidic channels are formed by removing material from a wafer and bonding or adhering it to another wafer to encapsulate the channels. In the rest of this paper, we focus on bulk micromachining.

III. PROCESS SELECTION

In this section, we address the selection of patterning, bonding, and electrode integration processes in turn. A process-selection framework is presented in Table I.

In choosing a patterning method, the capabilities of candidate processes need to be evaluated against target feature dimensions, their tolerances, and any limitations on surface roughness. Quinn *et al.* propose a systematic approach to choosing micropatterning processes for MEMS,⁴³ which could be valuable for designing micro- and nano-fluidic process flows. Here, we discuss in detail the capabilities of wet and dry etching of bulk glass and silicon.

All of the etching processes that we describe require the etched material to be *masked* with an etch-resistant layer. The mask must be patterned to expose those regions of the underlying material that are to be etched. As we explain below, the mask might be a metallic, ceramic, or polymeric layer, or a multi-layer combination of these material types. To pattern the mask layer, it is usual to apply a photoresist layer and expose it by photolithography before chemically developing the photoresist and etching the mask. The narrowest feature size that can be patterned using photolithography is limited by diffraction to around 0.5 μm for contact

TABLE I. Selection of the fabrication process according to the requirements of the application (optical, geometrical, electrical, and thermal).

Step	Selection to be made		Possible processing routes and criteria for their selection (preferred process options are shown in bold)		
			Route A	Route B	
1	Materials involved in the microfabrication process		<ul style="list-style-type: none"> ● Glass/glass (take this route if the application requires optical transparency of the device) 	<ul style="list-style-type: none"> ● Glass/silicon (a more common and well established route) 	
2	Patterning method	Microchannels	<ul style="list-style-type: none"> ● Wet etching in HF/HCl ● Dry etching (recommended only if vertical walls or high aspect ratio structures are required) 	<ul style="list-style-type: none"> ● Dry etching of the silicon ● For complex microfluidic devices requiring multiple channel layers, the silicon wafer can be patterned on both sides and via holes etched through the wafer to connect them; alternatively, the glass can be patterned (by wet etching) as well as the silicon. 	
		Through-holes for fluidic ports	<ul style="list-style-type: none"> ● Wet etching ● Sand-blasting ● Drilling 	<ul style="list-style-type: none"> ● Dry etching ● Laser-drilling ● Sand-blasting 	
3	Bonding method	No electrical connection	The device operates above $\sim 200^\circ\text{C}$	<ul style="list-style-type: none"> ● Fusion bonding ● Anodic bonding with metallic or a:Si layer 	<ul style="list-style-type: none"> ● Anodic bonding
			The device operates at or below $\sim 200^\circ\text{C}$	<ul style="list-style-type: none"> ● Adhesive bonding ● Anodic bonding with metallic or a:Si layer ● Fusion bonding 	<ul style="list-style-type: none"> ● Anodic bonding ● Adhesive bonding
		With electrical connection	The device operates above $\sim 200^\circ\text{C}$	<ul style="list-style-type: none"> ● Anodic bonding (the thickness of the metallic layer can be critical) ● Bonding using an intermediate layer 	<ul style="list-style-type: none"> ● Anodic bonding (the thickness of the metallic layer can be critical)
			The device operates at or below $\sim 200^\circ\text{C}$	<ul style="list-style-type: none"> ● Adhesive bonding ● Anodic bonding (the thickness of the metallic layer can be critical) 	<ul style="list-style-type: none"> ● Adhesive bonding ● Anodic bonding (the thickness of the metallic layer can be critical)
4	Fluid connections		<ul style="list-style-type: none"> ● Permanent: push-fit tubing into polymer ports (optionally fix with glue or PDMS) ● Permanently attached ferrule with removable capillary tubing (e.g., Nanoport) ● Temporary: push-fit capillary tubing into PDMS device (permanent if PDMS is plasma-treated) ● Mechanically clamped chip-holder 		

photolithography and to around $0.3 \mu\text{m}$ for projection photolithography.⁴⁴ When even smaller features are required, electron-beam or nanoimprint lithography may be used instead. The resolution of the lithography step usually provides a *lower bound* on the minimum feature size that can be achieved in the glass or silicon. Lateral etching of the mask or bulk material will generally increase the smallest achievable channel size.

A. Glass patterning

1. Wet etching

The wet-etching of glass is isotropic and is usually done with solutions of hydrofluoric acid. Glass is a mixture of oxides whose composition affects etching behavior.⁴⁵ It is preferable to use glass with a low content of any oxides that give insoluble products after reaction with HF. Such oxides include CaO, MgO, and Al₂O₃. To remove any insoluble products, HCl (Ref. 46) or H₃PO₄ (Ref. 47) can be added to the etching solution. The etch rate is a parabolic function of HF concentration and is strongly dependent on the glass composition; for Corning 7740, the etch rate in 49% concentration HF is around $8 \mu\text{m}/\text{min}$ (Ref. 48), while for quartz, the etching rate in the same solution is $1.3 \mu\text{m}/\text{min}$. Etch rate can be increased by raising the temperature of the solution, by using ultrasonic agitation or by annealing the glass wafer before etching.⁴⁹ Etch rate can be reduced by diluting the solution. Dilution with NH₄F is preferred to dilution with water because the ammonium fluoride buffer stabilizes and increases the HF₂⁻ content. Moreover, the presence of NH₄F stabilizes the pH value of the solution, ensuring a constant etch rate.⁵⁰ Particular safety precautions must be taken when using HF solutions because of the chemical's ability to permeate skin insidiously and dissolve bone.

A key issue in the micropatterning of glass is the masking layer. It is important to control the magnitude and sign (compressive or tensile) of any residual stress in the mask, as well as any stress gradient,⁵¹ and the hydrophobicity of the masking layer.⁴⁹ A small defect in a masking layer with tensile stress can generate cracks. If the masking layer presents a hydrophilic surface, the etching solution will easily penetrate through this crack and generate a pin-hole. Many masking materials for wet etching of glass have been reported in the literature, including photoresist,⁵² amorphous Si deposited at low (200°C)⁵³ or high temperatures (570°C),⁵⁴ LPCVD polysilicon,^{55,56} Cr/Au,⁵⁷ Cr/photoresist,⁵⁸ bulk Si,⁵⁹ amorphous SiC/PECVD,⁶⁰ Ag,⁶¹ Mo,⁶² and Ti.⁶³ A detailed analysis of masking materials used in wet etching of glass is presented in Ref. 45. The use of a photoresist mask is limited to shallow etching (up to a 2-min etching process in 49% HF). Photoresist, Ti, Ag, bulk Si, or even amorphous SiC masks lead to an increased isotropy of the etching process (i.e., an increased lateral etch rate), and for this reason, their application is limited. The most successful solutions involve multilayer depositions of Cr/Au/Cr/Au with photoresist,⁶⁴ a Cr/Au (50:1 μm) multilayer deposition with photoresist,⁴⁹ polished polysilicon (1.5 μm -thick) with SU-8 photoresist (50 μm -thick),⁵⁷ low stress amorphous Si/photoresist,⁵³ and low-stress (LS) amorphous Si/low-stress SiC/photoresist.⁶⁵ The presence of photoresist (hard-baked) is essential due to its hydrophobic nature: the penetration of the etchant through any small defects in the masking layer becomes difficult.

The difficulties associated with forming a resilient etch-mask can be avoided by using photosensitive glass such as Foturan[®],⁶⁶ which is directly exposed with patterned ultraviolet light in the wavelength range 290–330 nm. Silver atoms form in the exposed regions of the glass, promoting crystallization when the material is subsequently heated to $500\text{--}600^\circ\text{C}$. The crystallized regions exhibit a 20 times higher etch-rate than the unexposed regions when etched in 10% HF at room temperature. An exposure energy density of approximately $2 \text{ J}/\text{cm}^2$ has been found sufficient to pattern a 1 mm-thick plate of this material. Feature sizes of $25 \mu\text{m}$ and a surface roughness of $1 \mu\text{m}$ are claimed by the material's supplier.⁶⁶ It has also been shown that buried 3D structures such as channels, lenses, and waveguides can be directly written inside a single Foturan[®] sheet using a femtosecond laser.⁶⁷ Such an approach can eliminate the need for two glass layers to be bonded, albeit at the expense of using a serial exposure technique that would be expected to be slower and more expensive than photolithography.

2. Dry etching

Micropatterning of glass using dry etching processes is recommended only when an anisotropic etching profile is required on a transparent substrate. Compared to wet etching, the dry etching of glass is a relatively slow process, with etching rates of 0.5–0.7 $\mu\text{m}/\text{min}$ and poor selectivity relative to the mask. Moreover, the process, which is usually performed in inductively coupled plasma deep RIE reactors, is limited by the large amount of energy transferred to the glass material, which generates strong temperature gradients (the thermal conductivity of glass is 100 times lower than that of silicon). These temperature gradients can lead to poor control of the process and a reduced etch selectivity for glass over the masking material. They can also promote fracture of the wafer during processing. The process requires a low pressure of 5–10 mTorr, since ion bombardment of the material (physical etching) plays an important role. The gas precursors used for deep etching of glass are SF_6 ,^{68,69} C_4F_8 ,^{53,70} CF_4 ,⁷¹ or CHF_3 .⁷² Additional gases such as He, H_2 , O_2 , or Ar may be added to control chamber pressure or for improving the quality of the etching process. Since the selectivity of the etching process is low, a relatively thick masking layer is required, such as electroplated Ni (20 μm -thick) for SF_6 chemistry, bulk silicon,⁷¹ PECVD amorphous silicon (12 μm -thick),⁷⁰ or even a thick layer of SU-8 photoresist.⁷⁰ The selectivity of the etching rate (glass/mask) is about 4:1 and 2.5:1 for Si and SU-8 masks, respectively.

B. Silicon patterning

Silicon patterning methods suitable for microfluidic applications can be divided in two main groups, namely dry and wet etching processes. The most common, fastest, and therefore, recommended process is deep dry etching (the *Bosch process*), which is now routinely used for microfluidic applications.

1. Dry etching

Dry etching processes used in microfabrication can be divided according to whether they are anisotropic or isotropic. A common isotropic dry etch uses XeF_2 as the precursor.⁷³ The process is mainly used for dry-release in surface micromachining.

There are two main techniques for achieving high aspect ratio structures in silicon: the Bosch process (which is the more prevalent)⁷⁴ and *cryogenic* etching. The Bosch process is a two-step technique involving alternate passivation and etching. For the passivation step, a C_4F_8 -based plasma generates a conformal coating of a polytetrafluoroethylene (PTFE)-like fluorocarbon polymer over the exposed surfaces. In the next step, which uses fluoride chemistry (SF_6), the fluoropolymer deposited on the horizontal surfaces is removed by ion bombardment and the silicon is then isotropically etched for a period of a few seconds. By repeating the passivation/etch cycles and controlling the etch time, the degree of lateral etch is limited, allowing a trench to be etched vertically through the wafer. The most common masking layers used are photoresist (selectivity 50:1) and SiO_2 (selectivity 200:1). In the cryogenic deep RIE process, the wafer is chilled to around -110°C . The process uses SF_6/O_2 to provide fluorine radicals for silicon etching. At the above-mentioned temperature, a layer of SiO_xF_y forms, providing sidewall passivation. The etched profile is very sensitive to the pressure as well as to the SF_6/O_2 ratio. For both Bosch and cryogenic techniques, appropriate process parameters depend on the reactor design. A review of cryo-DRIE and Bosch-DRIE can be found in Ref. 75.

Oxidation of silicon after etching can help circumvent the feature-size limitations of photolithography. The growth of the oxide reduces the widths of trenches etched in silicon, which can be valuable for producing nanofluidic channels.^{24,25}

2. Wet etching

There are two main options for the wet etching of silicon: orientation-dependent etching and isotropic etching. Wet etching of silicon is recommended only when a dry process is not available.

The *isotropic etching* of silicon is performed in HNA solutions (a mixture of HNO_3 , HF, and CH_3COOH). In this redox etching reaction, HNO_3 oxidizes the Si surface, while HF

dissolves the generated oxide layer, and CH_3COOH acts as a diluent. The HNA etching solution is very aggressive and the etching rate is strongly dependent on the concentration and temperature of the acid.⁷⁶ A mixture of HNO_3 (69%) with HF (49%) in a ratio 2:1 gives etch rates of around $50 \mu\text{m}/\text{min}$.⁷⁷ The aggressive etching characteristic of HNA solution reduces the range of masking layers that can be used. The best masking layer for HNA solution is LPCVD Si_3N_4 , which has an etching rate of 1–10 nm/min.⁴⁴

The *orientation-dependent etching* of silicon⁷⁸ relies on the selective etching of different crystallographic planes. A number of etchants have been used for orientation-dependent etching of silicon, the best known being aqueous potassium hydroxide (KOH) solution, most likely due to the high etching ratio of about 400 between the (100) and (111) crystallographic planes. A KOH solution of at least 20% concentration is required for a good etching process; below this concentration, the surface becomes rough and insoluble residues can be found on the surface. Another characteristic of the process is the ability to stop the etch by inserting a heavily boron-doped layer in the silicon: the etch rate reduces greatly when the doped layer is reached.

Table II summarises the capabilities of the etchants described above. We recommend wet etching of glass and deep RIE of silicon as being the most versatile and reliable of these processes. Any choice of process will, of course, depend on the application, the availability of equipment, and the total cost involved.

C. Through-holes for fluid ports

Etched through-holes can be achieved in glass by deep wet etching (a process described above). In this case, suitable masks are Cr/Au/photoresist or LS amorphous Si (a:Si)/photoresist. Even better results can be achieved with LS a:Si/LS a:SiC/photoresist.⁶⁵ Highly concentrated HF solution must be used as the etchant. The back-side of the wafer can be protected with a

TABLE II. Summary of glass and silicon etchants.

Etched material	Process	Suitable etchants	Suitable masking layers	Etch rate	Remarks
Glass	Wet	HF/HCl (10/1) HF HF/ NH_4F	<ul style="list-style-type: none"> • Cr/Au/Photoresist • Amorphous Si • Molibdenum/photoresist • Amorphous Si/Amorphous SiC/Photoresist 	Up to 7–8 $\mu\text{m}/\text{min}$ (for Corning 7740)	The process is strongly dependent on glass composition
	Dry	SF_6 , C_4F_8 , CF_4 , CHF_3	<ul style="list-style-type: none"> • Ni plated • Thick amorphous Si • SU8 resist 	Up to 0.5–0.8 $\mu\text{m}/\text{min}$	The process is strongly dependent on glass composition
Silicon	Dry	Bosch	<ul style="list-style-type: none"> • Photoresist • SiO_2 (wet or PECVD) 	2–30 $\mu\text{m}/\text{min}$	Most recommended
		Cryogenic	<ul style="list-style-type: none"> • SiO_2 (wet or PECVD) • Metal 	Up to 7 $\mu\text{m}/\text{min}$	Smooth walls
	Wet	HNA (HNO_3 +HF+ CH_3COOH)	<ul style="list-style-type: none"> • Si_3N_4 (LPCVD) 	4–90 $\mu\text{m}/\text{min}$	Isotropic
		KOH	<ul style="list-style-type: none"> • Si_3N_4 (LPCVD, PECVD) • SiO_2 (thermal/wet) • SiC (PECVD) 	1.4 $\mu\text{m}/\text{min}$ in (100) direction	Anisotropic
		EDP	SiO_2 , Si_3N_4 , Ta, Au, Cr, Ag, Cu	1.25 $\mu\text{m}/\text{min}$ in (100) direction	Anisotropic
		TMAH	SiO_2 , Si_3N_4	1 $\mu\text{m}/\text{min}$ in (100) direction	Anisotropic

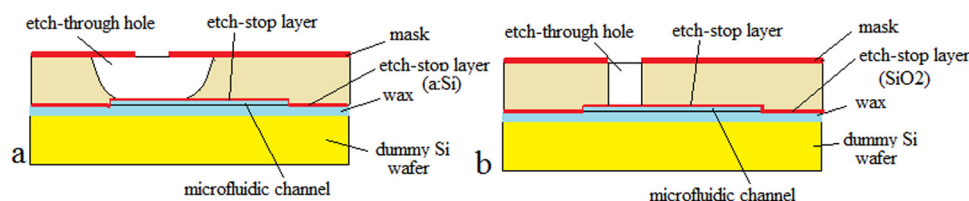


FIG. 1. Setup for etching through-holes in (a) glass and (b) silicon.

dummy silicon wafer bonded using wax (Figure 1(a)). Meanwhile, an etch-stop layer (amorphous silicon) is strongly recommended to protect the pattern on the other side of the wafer. Due to the isotropy of the process, the diameter of the generated hole is at least the diameter of the hole in the mask plus twice the wafer thickness. Several other methods have been used for patterning glass in microfluidic applications. Through-glass holes for fast prototyping can be achieved using sand-blasting,⁷⁹ laser-drilling,⁸⁰ electrochemical discharge,⁸¹ or drilling with diamond beads.⁸²

For silicon, well-dimensioned through-holes aligned within a few micrometers can be achieved using a deep RIE process. For the masking layer, 2–3 μm -thick SiO_2 , 10–15 μm -thick photoresist (according to the wafer thickness), or a double-layer mask (photoresist + SiO_2) can be used. Such an arrangement is presented in Figure 1(b). As an etch-stop layer, SiO_2 (PECVD) or tetraethyl orthosilicate (TEOS) can be used (0.2–0.5 μm thick). This layer helps to avoid deterioration through the notching effect of the structure on the back of the wafer. For the final part of the etching process (the last 50–100 μm), a dummy handle wafer can be attached with wax in order to avoid deterioration of the wafer's chuck.

D. Bonding

Wafer-bonding methods suitable for microfluidic applications can be categorized as *direct* (including fusion processes), *anodic*, and *adhesive*. Several factors must be taken into account in choosing a bonding process. These factors include the thermal coefficients of expansion of the materials to be bonded, their surface chemistries, temperature limitations resulting from earlier steps in the fabrication process, the presence of any metallic layers, price, throughput, and yield. Bonding processes are summarised in Table III.

1. Direct bonding

Two glass surfaces, mirror-polished ($R_a = 1.5\text{--}2$ nm) and with good planarity placed in contact at room temperature, will adhere due to the van der Waals force. In this case, the bond strength is weak (the shear stress supported by such a bond has been measured as 0.6 MPa (Ref. 83)). Direct bonding requires a good cleaning procedure to avoid contamination, and for this reason, it can be helpful to bring the surfaces to be bonded into contact under a continuous flow of deionised water. The bonding strength can be increased by activation of the surfaces and by annealing. Allen and Chiu⁸⁴ propose activation of the glass surface in a calcium solution followed by annealing for 1–2 h at 115 $^\circ\text{C}$. Plasma activation, which is frequently used for PDMS/glass bonding,⁸⁵ can also be used to increase the bond strength. Howlader *et al.* propose nitrogen radical activation of the glass surfaces in a microwave reactor after an oxygen RIE treatment.⁸⁶ They found that the glass must be subsequently heated to above 400 $^\circ\text{C}$ with the surfaces in contact to bring about a significant increase of the bond strength. With an annealing temperature of 600 $^\circ\text{C}$, a bond strength of around 24 MPa was attained.

Fusion bonding of Pyrex glass wafers (Corning 7740) can be performed at a temperature of 650 $^\circ\text{C}$.^{54,87,88} The wafers can be bonded in an annealing furnace. A slow cooling rate is required because glass wafers may fracture if exposed to substantial temperature gradients. The wafers must be horizontally supported during bonding to avoid deformation.⁸⁹ At 650 $^\circ\text{C}$, the glass is softened and the two surfaces to be bonded can readily conform, compensating for any roughness or the presence of metallization patterns at the interface.

TABLE III. Summary of bonding techniques with typical parameters (parameters may need to be varied according to the application).

Method	Materials		Process parameters	Remarks
Direct bonding	Plasma-activated bonding	Glass/glass	115–400 °C, N ₂ /O ₂ plasma activation of the surface	Weak bonding, the quality of the bonding process can be improved by annealing at 600 °C
	Fusion bonding	Glass/glass	650 °C	Strong bonding, special attention must be given to the plastic flow of the glass
Anodic bonding		Glass/silicon	305–350 °C, 0.05 MPa, 1000 V	Strong bonding with a good yield can be performed over SiO ₂ layers (up to 600 nm thick)
		Glass/silicon/glass	First bonding: 305–350 °C, 0.15 MPa, 1000 V Second bonding: 450 °C, 0.3 MPa, 1500 V	First bonding must be incomplete in order to keep the glass wafer conductive at relatively high temperature
Adhesive bonding	SU8	Glass/glass or glass/silicon	150 °C, 0.15 MPa N (4 in. wafer), 30 min	The SU8 layer can be imprinted on the surface to be bond
	Parylene		280–350 °C, 0.15 MPa, 2 μm-thick parylene	Good quality bonding with high yield can be performed over metals layers
	BCB		200–300 °C, 1–2 h, 0.15–0.25 MPa, in vacuum	Good quality bonding can be performed over metals layers
	Polyimide		180–400 °C, 1–3 h, in vacuum, 0.15–0.35 MPa surface preparation (O ₂ plasma)	Bond strength ~8 MPa, Recommended at chip size

2. Anodic bonding

Anodic bonding is a process that can be used to seal a glass cover to a patterned silicon wafer.⁹⁰ It is the simplest way of achieving a glass/silicon microfluidic device. The thermal expansion coefficient of the glass wafer must match that of the silicon in order to avoid cracks in the bonded wafers. Not all types of glass are bondable to silicon, a condition being the presence of Na₂O in the glass composition. Under the high voltage and temperature, Na⁺ migrates to the negative electrode, generating a strong electrostatic force and an irreversible chemical bonding between the substrates. The most commonly used are: Corning 7740, Borofloat and Tempax (Schott), and SD2 and SD4 (Hoya). The cleaning process of the wafer before bonding is a critical step for a good anodic bonding process.

Early work on the optimization of anodic bonding conditions for low residual stress is presented by Rogers and Kowal.⁹¹ The necessary bonding conditions depend on the glass material used. For Corning 7740, the optimal conditions are 305–350 °C and 500 V for 15 min (Ref. 92) and the necessary applied pressure is 0.05 MPa. At this bonding temperature, the expansions of silicon and glass are sufficiently similar. Meanwhile for Corning 7070, a glass with high resistivity, the optimal conditions were found to be 400 °C and 4 kV applied for 20 min at similar applied pressure. The presence of any dielectric layer (SiO₂) on the silicon substrate may require a higher applied voltage.⁹³

Glass/glass anodic bonding can also be carried out using Ti (80 nm thick) as a metallic intermediate layer.⁹⁴ The bonding connections reported for this work were a temperature of 530 °C and an applied voltage of 100 V; Corning 0021 microscope slides were used. With the Ti thickness of 80 nm, the bonded sample was still transparent. A *patterned* Ti/Pt intermediate layer has been used to form electrodes in a glass device, at the same time as enabling anodic

bonding of the glass layers.⁹⁵ Amorphous silicon has also been used as an intermediate layer for anodic bonding processes.^{96,97}

3. Glass/silicon/glass structures

Another structure of interest for transparent microfluidic devices is glass/silicon/glass,^{98,99} where the glass layers form the ceiling and the floor of the microfluidic channel, while the silicon defines the walls. The microfluidic channels are defined using a deep RIE process (in this case, a small notching effect can occur at the silicon-glass interface¹⁰⁰). In order to perform a double anodic bonding, the first bonding process must be incomplete so that the wafer pair remains somewhat conductive. This can be accomplished by stopping the first bonding process when the current has fallen to ~40% of its initial value. A low bonding temperature of 305 °C and an applied pressure of 0.15 MPa must be used. For the second bonding, the temperature is increased to 450 °C, the voltage to 1500 V, and the applied pressure to around 0.3 MPa, to allow some plastic flow of the glass and compensate for the deformation of the bonded wafers. Higher temperature also increases the conductivity of the stack, promoting the anodic bonding process.¹⁰⁰

4. Adhesive bonding

Adhesive bonding is well suited to microfluidic applications, because the adhesive layer between the bonded wafers is able to conform easily to the topography of any metallization layer patterned at the interface. Moreover, adhesive bonding is a simple, robust, and low-cost process. A review of the use of adhesive bonding in MEMS is presented in Ref. 101. The polymers used in adhesive bonding for microfluidic applications are usually thermoplastic materials (which can be repeatedly softened by heating and solidified by cooling) or thermosetting materials (which form a 3D network by cross-linking and cannot be remelted). Various adhesives have been used in microfluidic applications, including Parylene C, UV-curing epoxies (e.g., SU-8), benzocyclobutene (BCB), and polyimide. The main steps of an adhesive bonding process are

- surface cleaning,
- surface treatment (some polymer surfaces need to be treated with an adhesion promoter),
- coating with the adhesive layer (on one or both surfaces),
- baking process (optional),
- patterning (optional),
- bonding (usually using a bonding tool, under vacuum and an applied pressure).

A contact imprinting process has been demonstrated in which a SU-8 adhesive layer is applied only to those regions of the wafer that are to be bonded, keeping the adhesive out of the microfluidic channels.^{65,102} The bonding is performed at 150 °C for 30 min with an applied pressure of 0.15 MPa. The quantity of SU-8 applied must be very well controlled in order to avoid flow of the adhesive material into the microfluidic channels, and the technique depends on the operator's skill. A similar "stamp-and-stick" procedure using UV-curable adhesive to bond glass devices has also been presented.¹⁰³

Parylene is a thermoplastic material which has been used in MEMS wafer-bonding processes.¹⁰⁴ The material has been applied to microfluidic device fabrication for bonding glass to glass¹⁰⁵ and glass to silicon¹⁰⁶ at temperatures of 280–350 °C. Parylene has seen other microfluidic applications as well.^{107,108} The main advantages of Parylene C are its good thermal stability, good chemical resistance, and relatively strong bonding compared with SU-8: pull tests have shown a bonding strength of around 10 MPa and a maximum burst pressure of 7.6 MPa (Ref. 106). Parylene can be deposited in thin layers by chemical vapour deposition and can be patterned by dry etching through a photoresist mask. We have found that, with parylene, an areal bonding yield of greater than 90% is possible, which is comparable with anodic bonding.¹⁰⁶

BCB is another polymer that has been used for wafer bonding.¹⁰⁹ It can be made photosensitive or can be patterned by dry etching through a photoresist mask. BCB offers good chemical

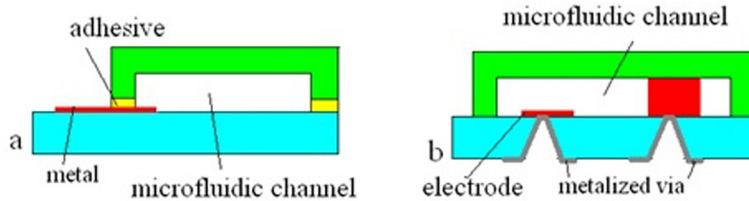


FIG. 2. Electrical feedthrough approaches: (a) lateral and (b) vertical. After the principle described by Esashi in Ref. 121.

resistance to acids, alkalis, and solvents, and is transparent to visible light. BCB can be applied by spin-coating and its use in microfluidic applications is presented in Refs. 110 and 111. The material is applied on one or both surfaces and is then pre-baked for a few minutes at 100–170 °C in order to remove the solvent, yet avoid cross-linking. Good bonding can be achieved at temperatures of 200–300 °C for 1–2 h, in vacuum with an applied pressure of 0.15–0.5 MPa,^{102,112} at these temperatures, the material reaches a low-viscosity state while cross-linking.

Polyimides are thermosetting and thermoplastic materials, suitable for microfluidic applications.^{113,114} During the curing process, voids tend to form in the polymeric film, and for this reason, polyimide is recommended for bonding at the chip scale.¹⁰² Polyimide can be spin-coated, followed by a baking process. Both surfaces to be bonded must be coated with polyimide. Depending on the material characteristics, the curing temperature can be 150–400 °C applied for 1.5–3 h at a pressure of 0.15–0.35 MPa (Ref. 115).

E. Electrode integration

Some microfluidic applications require the incorporation of electrodes. Examples are the electrical characterization of biological samples by impedance spectroscopy,¹¹⁶ particle manipulation by dielectrophoresis,^{117–119} and microfluidic fuel cells.¹²⁰ Any electrodes placed inside microfluidic channels must usually be connected to the outside world. As described by Esashi,¹²¹ there are two main techniques that can be used for such connections

Lateral feedthrough techniques (Figure 2(a)). Corman *et al.*¹²² have demonstrated anodic bonding over a metallization layer patterned on the glass substrate. The thickness of the metal layer was 25 nm (Cr/Au). Alternatively, most adhesive bonding methods can accommodate lateral feedthrough of metallization.^{40,80,81}

Vertical feedthrough techniques (Figure 2(b)). Methods for making electrical connections through via-holes have been proposed.¹²³ In one example, metallized via holes were fabricated in a glass substrate that had been polished to a thickness of 100–150 μm (Refs. 124 and 125) followed by isotropic wet etching through a Cr/Au mask. The electrodes themselves served as an etch-stop for the backside glass etching process. This approach, however, is more complex to achieve than lateral feedthrough.

IV. WORLD-TO-CHIP CONNECTIONS

In deciding how to connect a silicon/glass microfluidic device to the outside world, several questions must be answered

- Is the microfluidic device re-usable or disposable? In other words: how frequently do world-to-chip connections need to be broken and re-made?
- Will the connections be made to the edge or the surface of the device (*in-plane* or *out-of-plane*)?
- Does the world-to-chip connection system need to be reconfigurable or is it application-specific?

Additional factors to be considered include:

- the amount of chip area used by the interconnections;
- any requirements imposed by the connection system on the chip fabrication process;
- pressure tolerance;

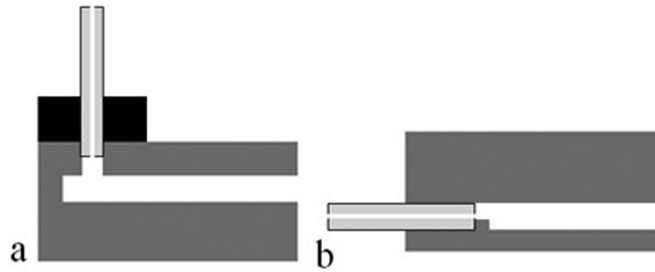


FIG. 3. Basic configurations of fluidic interconnects: (a) out-of-plane (top connector) and (b) in-plane (edge connector). The capillary is drawn showing both inner and outer diameters.

- temperature tolerance;
- compatibility of materials used;
- dead volume;
- price;
- usability.

Fluidic ports are often fabricated by conventional machining techniques, such as drilling or powder-blasting, and, if so, their dimensional and positional accuracies are much less than those of the microfluidic channels. As shown in Figure 3(a), port-to-microchannel misalignment can lead to dead volume.

Permanent attachment comes in two major forms: direct attachment of capillary tubing to the chip or permanent attachment of a fitting (or ferrule) to the chip, with the capillary being either permanently or temporarily attached to the fitting. It is sometimes possible to make out-of-plane connections by a simple push-fit between the capillary-tube and the chip, but such an attachment is usually mechanically too weak (polymer chips which can easily be 2–5 mm thick are more amenable to this sort of tube fitting¹²⁶). Gluing, melting,¹²⁷ and PDMS casting can be used to reinforce the connection, but may clog delicate microfluidic channels, leading to yield losses.

Commercial fittings from Upchurch,¹²⁸ Swagelok,¹²⁹ and Valco¹³⁰ are available for out-of-plane connections. They are universal in the sense that the fluidic design is done completely independently of the connectors. These fittings allow for detachment of tubing. The two basic varieties of tube contact are flat and coned; the coned variety is suitable for higher pressures. Individual connectors cost up to \$20, which can constitute a sizable portion of a fluidic system's cost.

Non-permanent attachment often makes use of the self-adhesive property of PDMS. In one implementation (Figure 4), an anisotropically etched silicon chip was itself used as a master

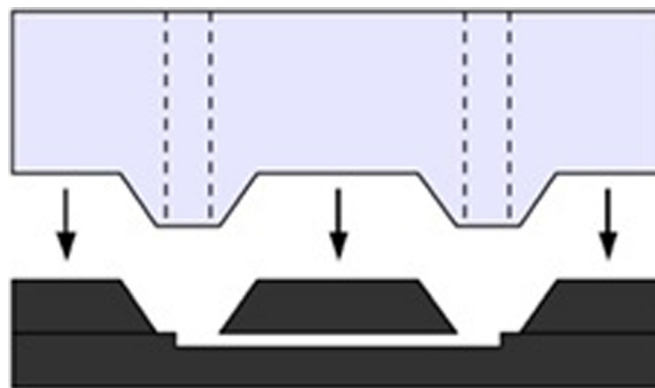


FIG. 4. A PDMS connector makes intimate contact with the silicon chip because a dummy replica of the chip itself was used as a mould master Reprinted with permission from Saarela *et al.*, *Sens. Actuators B* **114**, 552 (2005). Copyright © 2005, Elsevier.

mould for creating a matching PDMS piece.¹³¹ Dummy capillaries were inserted into the PDMS before curing. Both the connector and the capillaries can be detached and reinserted as long as the PDMS remains clean enough. If higher pressure tolerance is required, PDMS may be plasma-treated, but then a permanent bond is created. This connector results in extremely small dead volumes because all the structures are microfabricated. Non-permanent connectors have also been demonstrated using polyolefin heat-shrink tubing.¹³²

Various custom-made chip holders are in use. These holders are typically made of steel, brass, or ceramics like Macor, and incorporate o-rings for sealing and some sort of mechanical tightening.¹³³ This approach can benefit from inlet/outlet standardization: if inlets/outlets are only allowed at predetermined positions, the same holder works for many designs. An alternative, which is suitable for fast-changing prototype designs, is to use magnetic connectors.¹³⁴ A capillary is inserted inside a ring magnet, which is held in place by placing another magnet on the opposite side of the chip. This approach allows quick and easy testing. Limitations include magnet-magnet interactions, which limit closely spaced inlets, and the inability to handle fluids containing magnetic particles. Fluidic probe stations¹³⁵ resemble electric probe stations. Fluidic (and also electrical) connections are made with probe-heads, similar to electric probe needles, and pressure is applied mechanically to ensure leak-free connection. The system is best suited for applications with few inlets/outlets. Mechanical non-permanent connectors are difficult to implement for high-density inlets.

In-plane (edge) connection can be done simply by inserting the capillary into the on-chip fluidic channel (Figure 3(b)). Capillary outer diameters (ODs) are in the range of 100–300 μm , and fluidic channels must match those dimensions, which may add process steps in chip fabrication. Additionally, capillary inner diameters are typically 50 μm , and considerable dead volume may be introduced when a large OD capillary must be matched with much smaller on-chip channels. Another feature that might be needed is an on-chip stopper structure (Figure 3(b)). This stopper ensures that capillary insertion is self-limited and reproducible. Gluing is often used to fix the capillary in place. Dicing of silicon and glass is well established, and the high quality of diced edges allows them to be used as active parts of devices, including as interconnection sites.

Fluidic connections must sometimes sustain considerable pressures, e.g., in liquid chromatography. Pressures in the 100 bars range pose no problems for silicon and glass devices themselves; rather the connections become the limiting factor. For instance, soft o-rings, which accommodate surface irregularities, are not applicable in high-pressure applications.

Materials compatibility is especially important when aggressive solvents or high temperatures are used. Glues or PDMS can leach into fluidic channels, potentially ruining sensitive analyses.

V. CONCLUDING REMARKS

This paper has reviewed the state of the art in glass and silicon bulk micromachining and has aimed to provide the reader with enough information to conceive a suitable process flow for their own glass/silicon microfluidic application.

There are three main approaches to making glass/silicon-based micro- and nano-fluidic devices: surface micromachining, “buried-channel” technologies, and bulk micromachining. In this paper, we have focused on bulk micromachining, which is the most widely used approach.

For bulk micromachining, our analysis of the available etching, bonding, and interconnection techniques suggests two basic processing routes: one in which the device is constructed from a pair of glass layers and another in which a glass layer is bonded to a silicon one. Recommended sets of processes for the two routes are summarised in Table I.

For patterning *glass*, wet HF/HCl etching is recommended. Plasma etching may offer more vertical feature sidewalls and higher aspect-ratio structures, but remains slow and hard to control for glass. For silicon, in contrast, deep reactive ion etching is now a mature process and is recommended over wet etching. Suitable wet and dry etchants and masking layers for both silicon and glass are summarised in Table II.

The choice of bonding method depends on the chosen materials, the device's final operating temperature, and the presence or absence of integrated electrodes. Adhesive bonding is generally inexpensive and can readily conform to a patterned electrode layer at the interface, but is appropriate only up to operating temperatures of $\sim 200^\circ\text{C}$. For higher operating temperatures, anodic or fusion bonding is preferred; if anodic bonding is used with two glass layers, an interfacial conductive layer is needed. Parameters are recommended in Table III.

For inserting and removing fluids to and from a device, a wide variety of permanent and re-adjustable attachment schemes has been tried. Although there have been some attempts to commercialise microfluidic packaging systems, there is still plenty of scope for innovation in this area.

This paper has focused mainly on the production of devices with features that are more than a micrometer in size. We have, however, also touched on *nanofluidic* applications in which channels need to be sub-micrometer in depth, width, or both. Bulk micromachining is not an attractive way of producing nanochannels with a precisely controlled *depth*; for that purpose, surface micromachining is more promising. For deeper, sub-micrometer-*width* channels, however, bulk micromachining can be appropriate if the lithography step offers sufficient lateral resolution, or if feature widths are reduced to the desired value by post-etching oxidation. There is much work to be done to develop micro- and nano-fluidic fabrication techniques further and to integrate features with widely ranging length-scales into glass/silicon devices.

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