A Predictive Switching Modulator for Current Mode Control of High Power Factor Boost Rectifier

Souvik Chattopadhyay, V. Ramanarayanan, and V. Jayashankar

Abstract—In this paper, a new variation of current mode control for high power factor operation of boost rectifier is presented. The general features are no input voltage sensing, no use of multiplier, and no inner loop current regulator. It therefore follows the same control structure as that of the linear peak current mode control and the non linear carrier control. However, it implements a different switching law for the modulator that extends the range of continuous conduction mode of operation. The switching principle of the modulator is predictive, as the actual current equals the reference current at the end of each switching period. The no. of reset integrators required in this modulator for generation of the carrier waveform is two. The steady-state stability analysis of the boost rectifier with the proposed predictive switching modulator (PSM) is presented in this paper. A low-frequency small-signal model of the boost rectifier switched by the PSM is developed for evaluation of the control transfer function. Experimental results on a 400-W boost rectifier prototype are presented.

Index Terms—Boost converter, boost rectifier, continuous conduction mode, diode bridge rectifier, NLC, PFC, PSM, steady-state stability analysis.

I. INTRODUCTION

A DIODE BRIDGE rectifier followed by a boost converter is a typical single phase power factor correction (PFC) rectifier. The controller of PFC should shape the input current (i_{in}) to follow the same waveshape as the input voltage (v_{in}). With this objective, remarkable simplification in the control structure of the PFC rectifier has been achieved by carrier controllers such as the linear peak current mode (LPCM) control [3] and the nonlinear carrier (NLC) [4] control. The boost rectifier power circuit and the general controller structure of the NLC and the LPCM are shown in Fig. 1.

The inner loop current regulator is eliminated and input voltage sensing is not required in the NLC and the LPCM controllers. The analog multiplier is not present because the dc reference does not have to be converted into sinusoidal reference. In effect, the duty ratio of the switch is calculated in the LPCM or the NLC controllers by solving an equation in the modulator. One side of the equation is a certain function of the sensed current (for example average of the switch current for the NLC) and the other side is the carrier waveform derived after processing the voltage regulator output. The difference between the NLC and the LPCM is this: through the generation
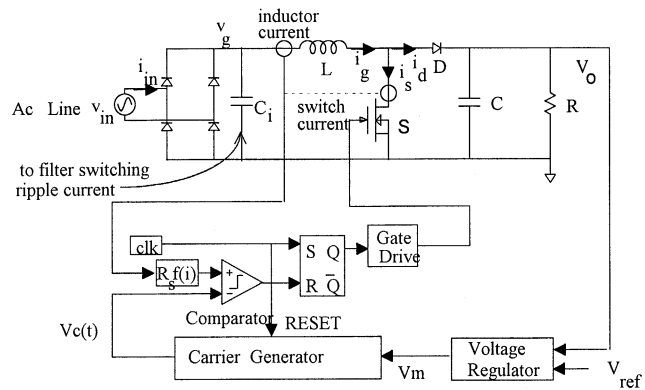
Fig. 1. Power circuit of the single phase PFC boost rectifier with the generalized control structure of the NLC, the LPCM, and the PSM.

of an appropriate carrier the NLC controller implements average current mode control whereas the LPCM controller would generate a different carrier waveform to implement the objective of peak current mode control.

In this paper, the predictive switching modulator (PSM) for current mode control of high power factor boost rectifier is proposed. In this strategy the duty ratio of the switch is controlled in such a way that the estimated inductor current will be proportional to the rectified input voltage at the end of the switching period (T_s). The estimation of the inductor current is possible since the input voltage is practically constant over a switching period. This enables us to predict the current ripple of the subsequent off period during the on time of the switch itself. The predicted off state ripple current can be added with the on state actual current to determine the current at the end of the switching period.

The input current waveform gets distorted in the discontinuous conduction mode (DCM) operation of the NLC controlled boost rectifier. The advantage of the PSM is the extended range of continuous conduction mode (CCM) of operation compared to the NLC. The PSM modulator has the structure of a standard current programmed controller with a compensating ramp that is nonlinear. The steady-state stability condition and the low-frequency small-signal model of the PSM switched boost rectifier are derived by applying standard graphical and analytical methods of the current mode control. The circuit realization of the PSM modulator is simple because only two numbers of reset integrators need to be used for the generation of the carrier waveform.

In Section II the control law of the proposed modulator—PSM is derived. Section III gives the steady-state
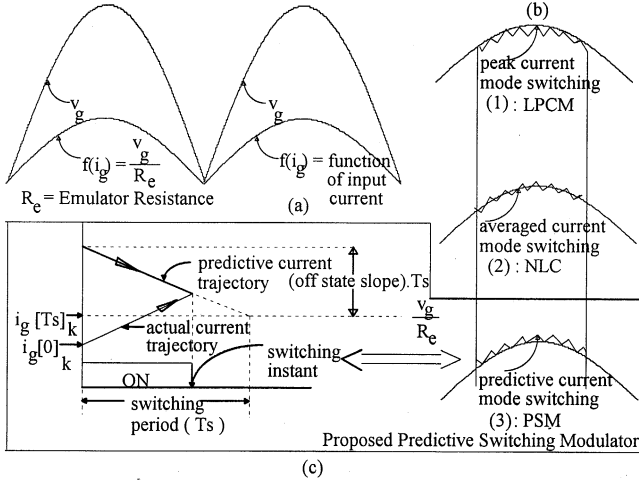
Fig. 2. (a) Generalized control objective of the carrier-based current mode controllers. (b) Switching laws of different types of carrier-based current mode controllers. (c) Operating principle of the PSM.

stability analysis of the PSM switched boost rectifier. Section IV defines the range of CCM. In Section V, the derivation of the low-frequency small-signal model is presented leading to the evaluation of the control gain transfer function. Section VI gives the experimental results of the PSM switched prototype boost rectifier with 400 W output.

II. PSM

The generalized control objective of a high power factor boost rectifier can be expressed as

$$f(i_g) = \frac{v_g}{R_e}. \tag{1}$$

R_e is the emulated resistance of the rectifier and $f(i_g)$ is a function of the inductor current i_g. This function can be different for different control strategies. For example NLC implements average current mode control, so for NLC (2) is the specific expression of $f(i_g)$. In the case of LPCM, this function represents peak current of the inductor, i_{gp}, in every switching period T_s, as given by (3). In a switching period the current in the inductor reaches its peak at the end of the ON time, dT_s, of the switch

$$f(i_g)_{nlc} = i_{g,av(T_s)} = \frac{1}{T_s} \int_o^{T_s} i_g \, dt \tag{2}$$

$$f(i_g)_{lpcm} = i_{gp} = i_g[dT_s]. \tag{3}$$

In the proposed modulator the duty ratio of the switch is controlled in such a way that the inductor current becomes proportional to the rectified input voltage at the end of each switching period. Therefore for PSM the function of i_g is given by (4)

$$f(i_g)_{psm} = i_g[T_s]. \tag{4}$$

Fig. 2(a) shows the generalized control objective of the boost rectifier. Fig. 2(b) illustrates the difference between the control objectives of:

1) LPCM;
2) NLC;
3) PSM.

For a boost rectifier the switch current is equal to the inductor current during ON time of the switch. In a switching period T_s,

instead of the inductor current, it is convenient to average the switch current i_s by carrying out integration only over the ON time of the switch because the switch current is zero during the rest of the period. Therefore the modulator of NLC implements the control law given by (5). For LPCM and PSM either the switch current or the inductor current can be sensed. It is advantageous to sense the switch current because of the simpler current sense method and the direct protection of the switching device. The control laws for LPCM and PSM in terms of the switch current are given by

$$di_{g,av(T_s)} = \frac{1}{T_s} \int_0^{dT_s} i_g \, dt = \frac{1}{T_s} \int_0^{dT_s} i_s \, dt = d \frac{v_g}{R_e} \tag{5}$$

$$i_g[dT_s] = i_s[dT_s] = \frac{v_g}{R_e} \tag{6}$$

$$i_g[T_s]_k = i_s[0]_{k+1} = \frac{v_g}{R_e}. \tag{7}$$

It may be noted that the inductor current at the end of period k is equal to the current at the beginning of the next period $k+1$, or, $i_g[T_s]_k = i_g[0]_{k+1}$. Since that switching frequency of the converter is much higher than the frequency of the input voltage we can assume that the input and the output voltages are constant in a switching period. Therefore, when the converter is operating in CCM the slope of the turn-off current can be predicted during ON time of the switch itself. Then instead of (7), (8) can be used for PSM

$$i_g[dT_s]_k = i_s[dT_s]_k = \frac{v_g}{R_e} + \left(\frac{V_o - v_g}{L}\right)(1-d)T_s. \tag{8}$$

Fig. 2(c) shows how the switching instant is determined in PSM. The expression on the right-hand-side of (8) represents the predictive current trajectory, whose initial value is $(v_g/R_e) + (V_o - v_g/L)T_s$ and the slope is equal to $(v_g - V_o)/L$, the slope of the off state inductor current. In PSM the switch turns off when the actual current equals the predictive current trajectory or (8) is satisfied.

We can use the boost converter continuous conduction mode input to output conversion equation of (9) to replace v_g in (8) by V_o and d. Then we get (10) as the duty ratio control function for the PSM

$$v_g = (1-d)V_o \tag{9}$$

$$i_g[dT_s] = I_{ref}(1-d) + \left(\frac{V_o T_s}{L}\right)d(1-d) \tag{10}$$

where

$$I_{ref} = \frac{V_o}{R_e} = \frac{V_m}{R_s}. \tag{11}$$

R_s is the current sense resistance of the converter and V_m is the input voltage to the modulator. Under closed loop operation V_m is obtained as the output of the voltage error amplifier loop. In [2] and [1], the right-hand-side expressions of (5) and (6) are converted into suitable carrier waveforms by replacing the duty ratio term d by t/T_s. Similarly the carrier waveform $I_c(t)$ for the predictive switching modulator can be expressed as

$$I_c(t) = \frac{V_c(t)}{R_s}$$

$$= I_{ref}\left(1 - \frac{t}{T_s}\right) + \left(\frac{V_o T_s}{L}\right)\frac{t}{T_s}\left(1 - \frac{t}{T_s}\right)$$

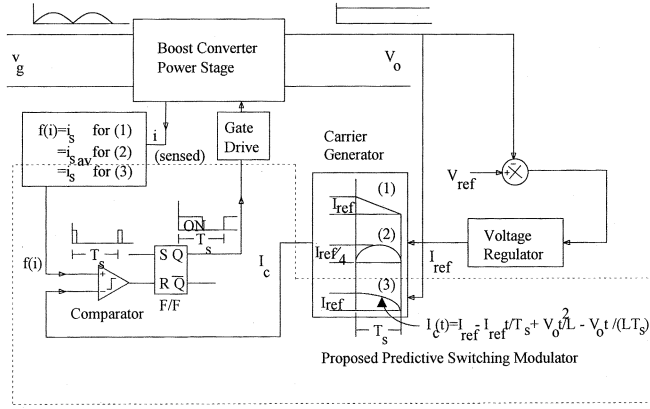$$\text{for } 0 \leq t \leq T_s. \tag{12}$$

Fig. 3. Block diagram of the carrier-based input-current-shaping controllers: 1) the LPCM; 2) the NLC; and 3) the PSM.

Fig. 3 shows the block diagram of the LPCM, the NLC and the PSM control schemes. The overall control scheme resembles that of a current mode control. In the PSM the switch is turned on at the beginning of every switching period and turned off when the duty ratio is such that the condition given by (10) is satisfied.

III. STEADY STATE-STABILITY CONDITION

Current mode control may exhibit steady-state stability problem under certain operating conditions because of the presence of a local feedback in its control structure [3]. The steady-state stability analysis presented in this section is graphical in nature. We have followed the same method that has been used in [3] for deriving the steady-state stability condition for the current mode controlled dc–dc converter. The objective here is to quantify the steady-state stability condition of the PSM switched boost rectifier in terms of circuit parameters and switching frequency of the converter.

The steady-state carrier waveform, shown in Fig. 4(a), is configured as a function of $d = t/T_s$, in the standard structure of

$$I_c(d) = I_{ref} + I_{comp}(d)$$
$$= I_{ref} - M_x T_s d - M_y T_s d^2, \qquad \text{for } 0 \le d \le 1 \quad (13)$$

where

$$I_{comp}(d) = -I_{ref} d + \frac{V_o T_s}{L} d - \frac{V_o T_s}{L} d^2$$
$$= -M_x T_s d - M_y T_s d^2, \qquad \text{for } 0 \le d \le 1 \quad (14)$$

and

$$M_x = \frac{I_{ref}}{T_s} - \frac{V_o}{L} \quad (15)$$

$$M_y = \frac{V_o}{L}. \quad (16)$$

The compensating waveform $I_{comp}(t)$ consists of components of linear and nonlinear ramps, as shown in Fig. 4(b). M_x and M_y are the coefficients of the linear and nonlinear ramp. Let ∇i_g be the initial perturbation in i_g and the perturbation in current becomes ∇i_{g1} at the end of the switching period. This is shown in Fig. 5(a). The steady-state duty ratio is d and under perturbed condition the duty ratio changes to d_1. The following
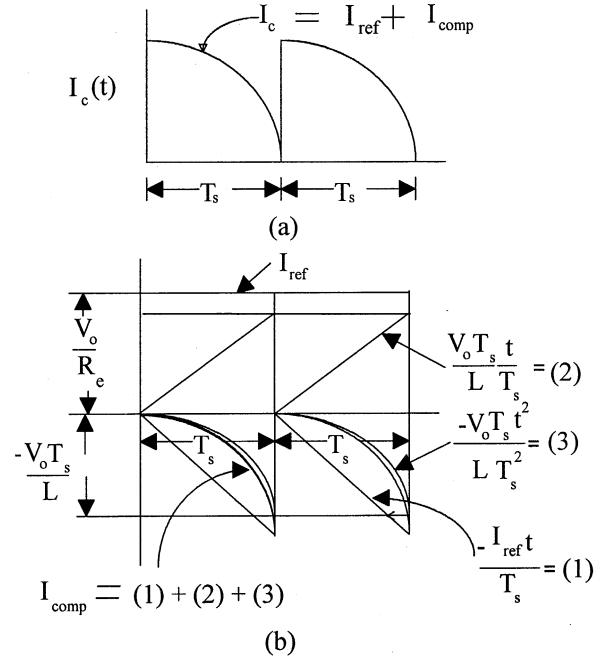

Fig. 4. (a) Carrier waveform of the PSM. (b) Current reference I_{ref} and different components of the compensating waveform I_{comp}.

equations define the switching characteristics of the converter under steady and perturbed state:

$$i_g + m_1 d T_s = I_{ref} - M_x d T_s - M_y d^2 T_s \quad (17)$$
$$i_g + \nabla i_g + m_1 d_1 T_s = I_{ref} - M_x d_1 T_s - M_y d_1^2 T_s \quad (18)$$
$$i_g + m_2(1-d)T_s = I_{ref} - M_x d T_s - M_y d^2 T_s \quad (19)$$
$$i_g + \nabla i_{g1} + m_2(1-d_1)T_s = I_{ref} - M_x d_1 T_s - M_y d_1^2 T_s. \quad (20)$$

$m_1 > 0$ and $m_2 > 0$ are magnitudes of the slopes in the inductor current during turn-on and turn-off intervals of the switch respectively. During the perturbation m_1 and m_2 are assumed to remain constant because the output voltage is constant and the input voltage is a slow varying quantity. For the boost converter m_1 and m_2 can be expressed as

$$m_1 = \frac{v_g}{L} = \frac{(1-d)V_o}{L} \quad (21)$$

and

$$m_2 = \frac{V_o - v_g}{L} = \frac{dV_o}{L}. \quad (22)$$

From (17)–(20) we can get

$$\frac{\nabla i_{g1}}{\nabla i_g} = -\frac{m_2 - M_x - M_y(d + d_1)}{m_1 + M_x + M_y(d + d_1)}. \quad (23)$$

In (23), we can replace m_1, m_2, M_x, M_y, and I_{ref} by the expressions of (11), (15), (16), (21), and (22), respectively, in order to obtain

$$\frac{\nabla i_{g1}}{\nabla i_g} = 1 - \frac{1}{d_1 + \frac{L}{R_e T_s}}. \quad (24)$$

Subharmonic oscillations in the boost rectifier can be avoided under the following condition:

$$\left| \frac{\nabla i_{g1}}{\nabla i_g} \right| < 1. \quad (25)$$
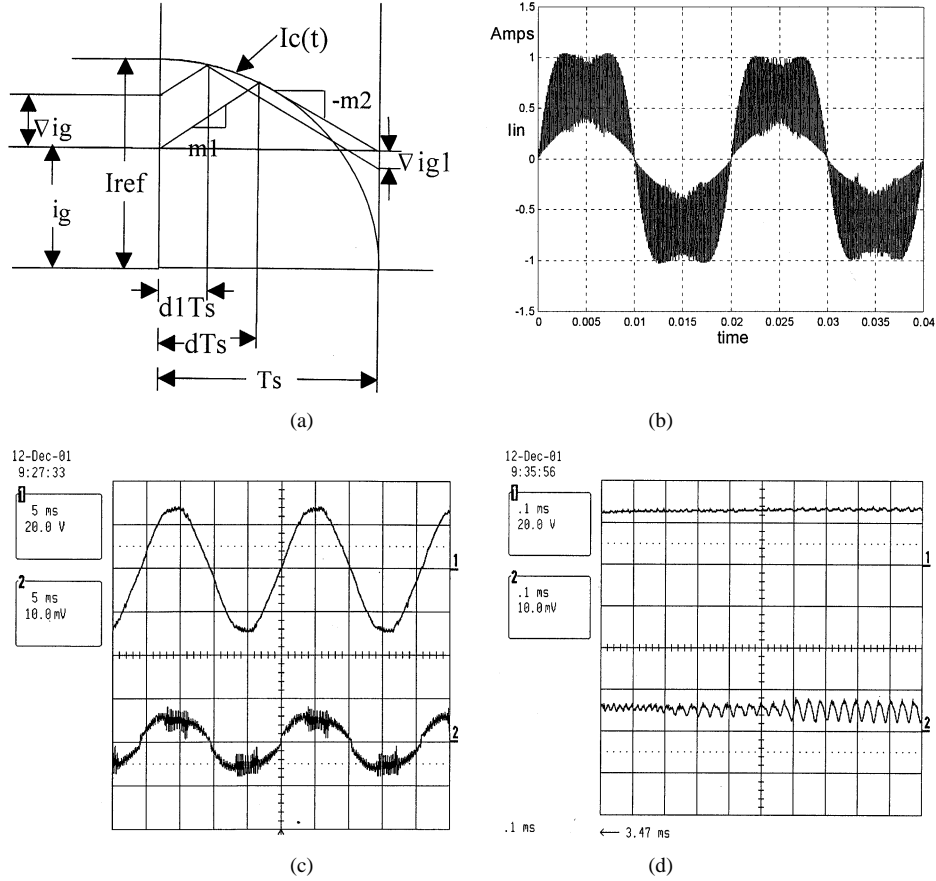
(a)

(b)

(c)

(d)

Fig. 5. (a) Analysis of the steady-state stability condition of the PSM switched boost rectifier. (b) Simulation result of the input current waveform shows distortion near the peak of the waveform due to violation of the steady-state stability condition. (c) Experimental results (the ripple is less because of the input filter capacitor C_{in}) show distortion in the input current verifying the analysis. Ch1: Input voltage $v_{in} - 230$ V/div. Ch2: Input current $i_{in} - 1.75$ A/div. (d) Ch1: Input voltage v_{in}. Ch2: The stability problem in the input current—i_{in}—is shown in expanded scale.

From (24) and (25), the steady-state stability condition for the PSM switched boost rectifier in terms of circuit parameters can be expressed as

$$\frac{2L}{R_e T_s} > (1 - 2d_1). \tag{26}$$

We assume that the perturbation ∇i_g is small, therefore $d_1 \approx d$. In CCM the duty ratio of the switch can be expressed as

$$d = (1 - m_g), \qquad \text{where } m_g = \frac{v_g}{V_o}. \tag{27}$$

By combining (26) and (27), the steady-state stability condition can be obtained as

$$\frac{2L}{R_e T_s} > (2m_g - 1). \tag{28}$$

We need to replace R_e in (28) by the load resistance R and other circuit parameters. For that the power balance condition $P_o = P_{in}$ between the input and output of the rectifier is used

$$\begin{aligned} P_{in} &= \frac{2}{T} \int_0^{T/2} v_g i_{g,\,av(T_s)} \, dt \\ &= \frac{2}{T} \int_0^{T/2} v_g \left[\frac{v_g}{R_e} + \left(1 - \frac{v_g}{V_o}\right) \frac{v_g T_s}{2L} \right] dt \\ &= \frac{V_{gm}^2}{2R_e} + \frac{V_{gm}^2}{2} \frac{T_s}{2L} - \frac{V_{gm}^3}{V_o} \frac{T_s}{2L} \frac{4}{3\pi} \end{aligned} \tag{29}$$

$$P_{out} = \frac{V_o^2}{R}. \tag{30}$$

Here, T is the period of the line voltage waveform. Therefore by equating the expressions of (29) and (30) we get

$$\frac{R}{R_e} = \frac{2}{M_g^2} - \frac{T_s R}{2L} \left(1 - M_g \frac{8}{3\pi}\right) \tag{31}$$

where M_g is defined as

$$M_g = \frac{v_{g,\,\max}}{V_o} = \frac{V_{gm}}{V_o}. \tag{32}$$

V_{gm} is the peak value of the rectified input voltage. We can also define K as

$$K = \frac{2L}{RT_s}. \tag{33}$$

By combining (28) and (31), the steady-state stability condition of the PSM switched boost rectifier can be expressed as

$$K > M_g^2 \left(m_g - M_g \frac{4}{3\pi}\right). \tag{34}$$

It can be seen from (34), that the right-hand side expression is maximum when m_g or the rectified input voltage in a line cycle is maximum. The condition for avoiding sub-harmonic oscillations in the PSM switched boost rectifier over the entire cycle of the input voltage waveform is given by

$$K > Ksp = M_g^3 \left(1 - \frac{4}{3\pi}\right). \tag{35}$$

In Fig. 5(b), the simulation result of the input current waveform is shown with the component values given by Table I. The dis-

TABLE I
COMPONENT VALUES

V_g	220 V
V_0	400 V
V_0	2.5 mH
F_s	50 KHz
K	0.208
C	470 μF
R	1200 Ω

Fig. 6.   Comparison of different critical K parameters: 1) K_{sp}: steady-state stability condition with the PSM; 2) K_{cp}: CCM operation with the PSM; and 3) K_{cn}: CCM operation with the NLC.

tortion near the peak of the waveform is due to the violation of the steady-state stability condition given by (34). The experimental result under the same operating condition is shown in Fig. 5(c) (the ripple is less because of the input filter capacitor C_{in} connected at the input). The distortion in the input current verifies the analysis presented above. In Fig. 5(d) the stability problem in the input current is shown in an expanded scale. It may be noted that the current distortion does not spread over the entire line half cycle, instead it gradually reduces in the region in which $K > M_g^2(m_g - M_g(4/3\pi))$.

IV. DCM

The modulator proposed in Section II is capable of shaping the input current like input voltage as long as the basic boost converter operates in the continuous conduction mode (CCM). The objective of the analysis presented in this section is to determine the condition for the DCM in the PSM switched boost rectifier.

In the DCM, the inductor current is zero at the beginning of a switching period. Therefore the duty ratio of the period is determined by the modulator equation

$$\frac{v_g d T_s}{L} = I_{ref}(1 - d) + \frac{V_o T_s}{L} d(1 - d). \qquad (36)$$

But in the DCM, (9) is no longer valid. Instead

$$v_g < (1 - d)V_o. \qquad (37)$$

Combining (36) and (37) we get (38) as the condition for the DCM

$$I_{ref} < 0. \qquad (38)$$

The expression of the average power $(\tilde{P})$ due to the ripple current in the inductor (for $I_{ref} = 0$) can be obtained from (29). It is given by

$$\tilde{P} = \frac{T_s}{2L} \frac{V_{gm}^2}{2} - \frac{T_s}{2L} V_{gm}^2 M_g \frac{4}{3\pi}. \qquad (39)$$

When the PSM switched boost rectifier is in the DCM, $I_{ref} < 0$, and the output power $(V_o^2/R) < \tilde{P}$. The condition for the DCM can be obtained as

$$K < K_{cp} = \left(\frac{M_g^2}{2} - M_g^3 \frac{4}{3\pi}\right). \qquad (40)$$

It can be concluded from (40), that if $K \geq ((M_g^2/2) - M_g^3(4/3\pi))$ the PSM switched boost rectifier remains in CCM over the entire duration, i.e., $T/2$, of the line half cycle. However, if the load resistance is such that
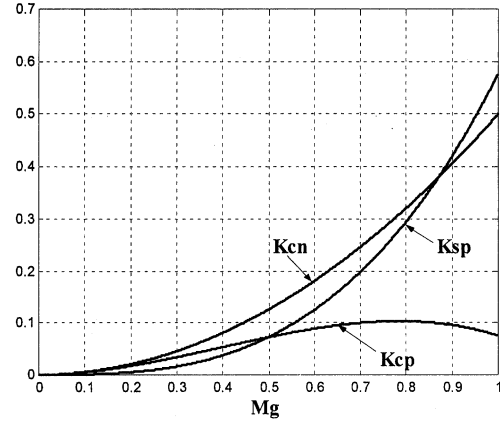
$K < ((M_g^2/2) - M_g^3(4/3\pi))$ then the boost rectifier will operate stably in the DCM. In this mode a low-frequency pattern will appear in the steady-state waveform of I_{ref}. The average value of I_{ref} will be negative in the DCM. The inductor current will not change its conduction state in every switching period T_s. Instead, for a few cycles of T_s, in which $I_{ref} > 0$, the inductor current will be continuous and in subsequent switching periods in which $I_{ref} < 0$ the boost switch will not conduct at all.

We need not avoid the DCM operation in the PSM switched boost rectifier. The power stage design gets affected if it becomes necessary to operate the rectifier in the CCM over the entire load range for best possible total harmonic distortion (THD) performance. We can find from the right-hand-side expression of (40) that the maximum value of K_{cp} is 0.1 in the voltage range $0 \leq M_g \leq 1$. If the maximum load resistance, $R_{\max}$, is known for a particular application, then the design coefficient $K = 2L/R_{\max}T_s$ should be >0.1 for CCM operation over the entire input voltage range (universal ac voltage application).

In comparison, the NLC [2] controlled boost rectifier should satisfy (41) to support CCM over the entire half cycle of the input voltage waveform

$$K > K_{cn} = \frac{M_g^2}{2}. \qquad (41)$$

K_{cp}, K_{cn} and K_{sp} as functions of M_g are plotted in Fig. 6. K_{sp} values are valid only in the range in which CCM operation occurs, because such a condition has been used in its derivation. It can be seen from this figure as well as from (40) and (41) that over the entire range of M_g (42) holds

$$K_{cp} < K_{cn}. \qquad (42)$$

Therefore, PSM offers wider range of continuous conduction mode of operation compared to NLC. This can also be seen from Fig. 6. However, in the range $0.5 > M_g > 1$, we find that $K_{sp} > K_{cp}$. In this range the rectifier will operate in the CCM but distortion near the peak of the input current waveform will occur if K is not greater than K_{sp}. It may also be noted from Fig. 6 that for $0 < M_g < 0.86$, the PSM offers a wider range of CCM operation in the stable operating mode compared to the NLC.
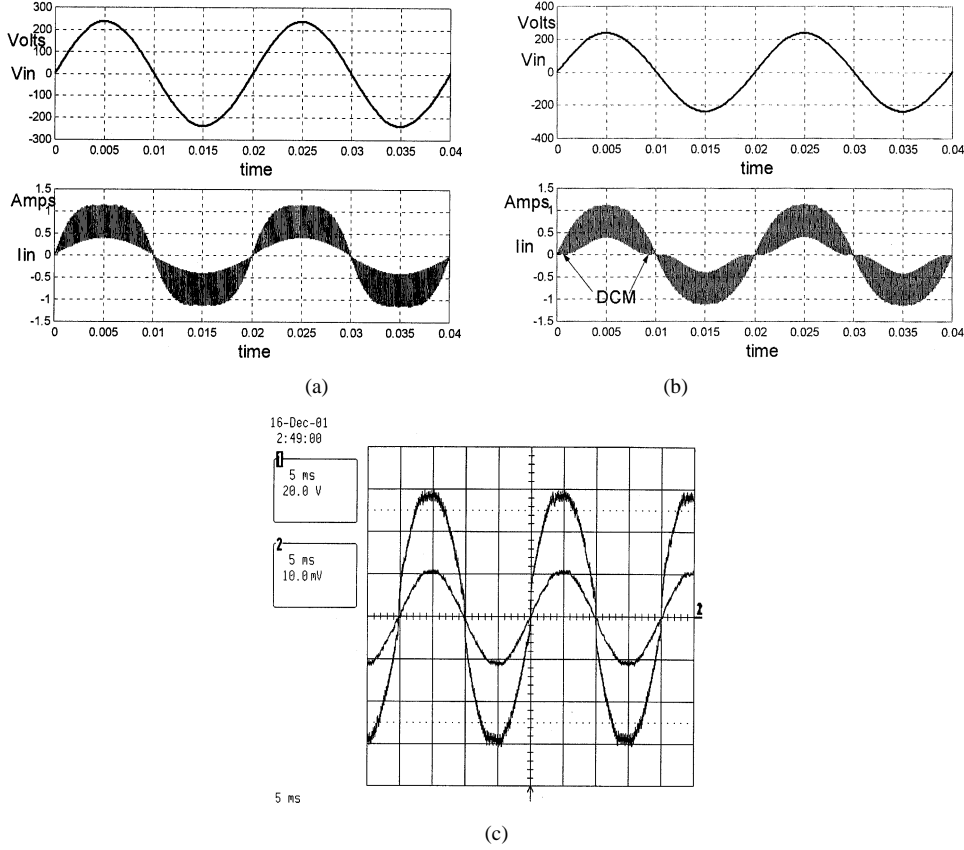
Fig. 7. Simulation results of the input voltage and the input current waveforms of the boost rectifier switched: (a) by the PSM; (b) by the NLC; and (c) the input v_{in} voltage and the input current i_{in} experimental waveforms, (ch1: 230 V/div, ch2: 0.3 A/div), of the PSM switched boost rectifier showing CCM operation for the entire line cycle at the operating condition described in Table II.

The simulation waveforms of the input current (i_{in}) and the input voltage (v_{in}) with the PSM are shown in Fig. 7(a). It verifies that, at $M_g = 0.6$ and $K = 0.15$, the CCM operation over the entire line half cycle is possible if the boost rectifier is switched by the PSM. The component values are listed in Table II. The experimental verification of the CCM operation under the same operating condition is shown in Fig. 7(c) for the PSM switched boost rectifier. In Fig. 7(b) the simulated input current waveform correspond to the NLC controlled boost rectifier under identical operating condition as in Fig. 7(a). It may be seen that near the zero crossings of the input current waveform the converter goes into DCM in the NLC controlled converter.

V. LOW FREQUENCY SMALL SIGNAL MODEL

In this section, we would like to develop a linear, low-frequency, small-signal model of the boost rectifier switched by the PSM. In a line cycle, the rectified input voltage v_g varies from 0 to V_{gm}. Under steady-state condition the inductor current i_g is proportional to rectified input voltage v_g and the volt-second balance for the boost inductor occurs at every switching period T_s.

However, the instantaneous input power $v_g i_g$ equals the output power V_o^2/R only at the period in which rectified input voltage is $V_{gm}/\sqrt{2}$. We therefore choose this switching period as the equivalent nominal operating point that represents the entire line cycle for the derivation of the small-signal model. The variables are expressed by capital letters (nominal as well

TABLE II
COMPONENT VALUES

V_g	168 V
V_0	400 V
L	2.5 mH
F_s	50 KHz
K	0.15
C	470 μF
R	1666 Ω

as DC) and small-signal deviations by ($\widehat{}$) on the top of the symbol. The control structure shown in Fig. 1 is that of a current mode controller. So the control gain transfer function is derived in two steps [3], [6]. First, the low-frequency small-signal model of the boost converter is obtained in the standard form in terms of duty ratio perturbation $\hat{D}$ as the control input. Subsequently the small-signal model of the modulator is derived in order to replace $\hat{D}$ by the perturbations in the error amplifier output voltage $\widehat{V_m}$ and other state variables $\widehat{V_o}$ and $\widehat{I_g}$. The state space averaged model of the boost converter power stage is given by [5]. We have used that model at the dc operating point of input voltage rms

$$\begin{bmatrix} \dfrac{dI_g}{dt} \\ \dfrac{dV_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{-(1-D)}{L} \\ \dfrac{(1-D)}{C} & \dfrac{-1}{RC} \end{bmatrix} \begin{bmatrix} I_g \\ V_o \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} [V_g]$$
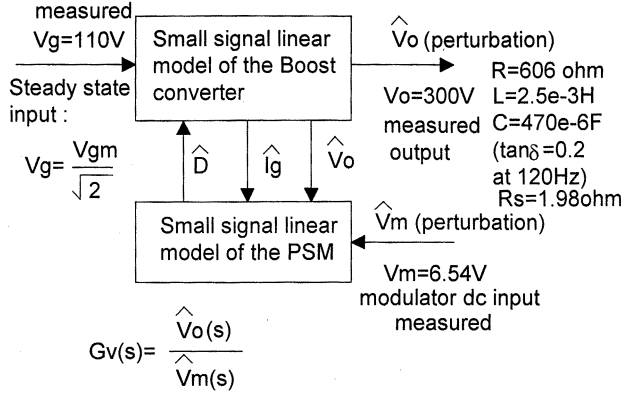
$$(43)$$

Fig. 8.   Schematic diagram for derivation of the small-signal linear model of the PSM switched boost rectifier for evaluation of the control gain transfer function $G_v(s)$. The operating point for experimental verification of $G_v(s)$ is also mentioned.

where

$$V_g = \frac{V_{gm}}{\sqrt{2}}. \qquad (44)$$

The steady-state values of V_o and I_g can be obtained from

$$V_o = \frac{1}{(1-D)} V_g \qquad (45)$$

$$I_g = \frac{V_g}{(1-D)^2 R}. \qquad (46)$$

The linear small-signal model of the boost converter is obtained by perturbing the state variables and the duty ratio input. Since our objective is to derive the control transfer function $G_v(s) = \widehat{V_o}(s)/\widehat{V_m}(s)$, the rectified input voltage V_g is not perturbed. Fig. 8 shows the schematic diagram of the method that has been used for deriving the control transfer function of the PSM switched boost rectifier

$$\begin{bmatrix} \dfrac{d\widehat{I_g}}{dt} \\ \dfrac{d\widehat{V_o}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{-(1-D)}{L} \\ \dfrac{(1-D)}{C} & \dfrac{-1}{RC} \end{bmatrix} \begin{bmatrix} \widehat{I_g} \\ \widehat{V_o} \end{bmatrix} + \begin{bmatrix} \dfrac{V_o}{L} \\ \dfrac{-I_g}{C} \end{bmatrix} [\hat{D}]. \qquad (47)$$

The modulator uses the inductor current I_g and the output voltage V_o for producing the duty ratio of the period according to

$$V_m(1-D) + \frac{V_o R_s T_s}{L} D - \frac{V_o R_s T_s}{L} D^2 = I_g R_s + \frac{V_g R_s T_s}{2L} D \qquad (48)$$

R_s is the sense resistance of the inductor current. The steady-state duty ratio D can be obtained (D is the positive real root and less than 1) by solving

$$\left[-V_m + \frac{V_g R_s T_s}{2L} \right] D^3 + \left[3V_m - \frac{V_g R_s T_s}{L} \right] D^2$$
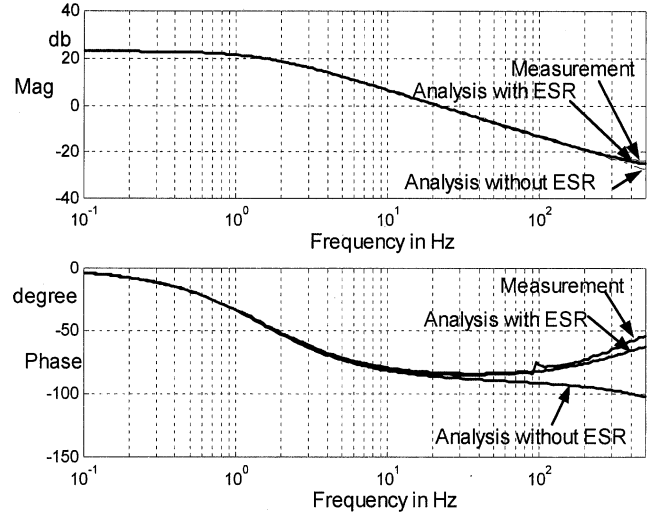

Fig. 9.   Bode plot of the control gain transfer function $G_v(s)$ of the PSM switched boost rectifier. Analysis results of the model with and without the ESR of the capacitor and the measurement results from the Schlumberger 1250 frequency response analyzer instrument are plotted in the same figure for easy comparison.
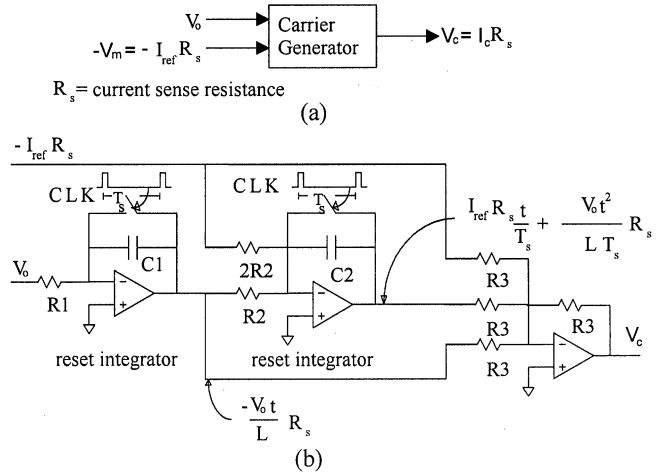

Fig. 10.   (a) Carrier generator block of the PSM. (b) Circuit realization of the PSM carrier waveform.

$$+ \left[-3V_m + \frac{V_g R_s T_s}{2L} \right] D + \left[V_m - \frac{V_g R_s}{R} \right] = 0. \qquad (49)$$

We perturb (48) and subsequently linearize the quantities to obtain the small-signal linear model of the PSM, as given by

$$\left[\frac{V_g T_s R_s}{2L} + V_m + 2DV_o \left(\frac{R_s T_s}{L} \right) - V_o \left(\frac{R_s T_s}{L} \right) \right] \hat{D}$$

$$= (1-D)\widehat{V_m} + D(1-D)\left(\frac{R_s T_s}{L} \right) \widehat{V_o} - \widehat{I_g} R_s. \qquad (50)$$

We define a constant N as follows:

$$N = \left[\frac{V_g T_s R_s}{V_o 2L} + \frac{V_m}{V_o} + 2D \left(\frac{R_s T_s}{L} \right) - \left(\frac{R_s T_s}{L} \right) \right]. \qquad (51)$$
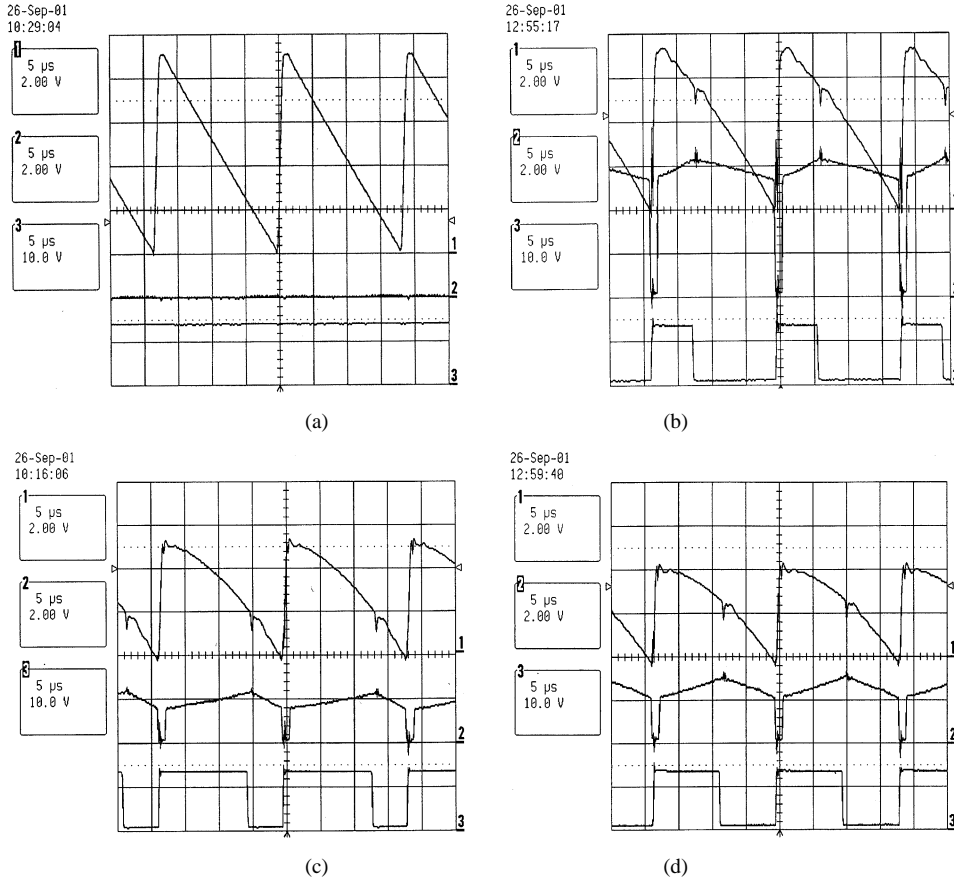
Fig. 11. Experimental modulator waveforms of the PSM switched boost rectifier. Ch1: Carrier waveform $V_c(t)$. Ch2: Sensed inductor current $i_g(t)$. Ch3: Switch duty ratio pulses. (a) At $V_o = 0$ V, $V_{in} = 0$. (b) At $V_0 = 400$ V, $V_{in} = 170$ V, $R = 500$ Ω. (c) At $V_0 = 400$ V, $V_{in} = 200$ V, $R = 500$ Ω. (d) At $V_0 = 400$ V, $V_{in} = 220$ V, $R = 500$ Ω. The current sensing resistance is $R_s = 1.98$ Ω and the sensed current signal is reset at the beginning of every switching cycle to avoid generation of noise-related turn-off pulses.

We can rewrite (47) as (52) after replacing $\hat{D}$ by the expression of (50) and using the definition of N

$$
\begin{bmatrix} \dfrac{d\widehat{I_g}}{dt} \\[2mm] \dfrac{d\widehat{V_o}}{dt} \end{bmatrix}
$$

$$
= \begin{bmatrix} -\dfrac{1}{L}\dfrac{R_s}{N} & \dfrac{-(1-D)}{L} + \dfrac{D(1-D)}{N}\dfrac{R_sT_s}{L} \\[3mm] \dfrac{(1-D)}{C} + \dfrac{I_g}{C}\dfrac{R_s}{V_oN} & \dfrac{-1}{RC} - \dfrac{I_g}{C}\dfrac{D(1-D)}{V_oN}\dfrac{R_sT_s}{L} \end{bmatrix}
$$

$$
\cdot \begin{bmatrix} \widehat{I_g} \\[2mm] \widehat{V_o} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L}\dfrac{(1-D)}{N} \\[3mm] \dfrac{-I_g}{C}\dfrac{(1-D)}{V_oN} \end{bmatrix} \begin{bmatrix} \widehat{V_m} \end{bmatrix}. \qquad (52)
$$

The control gain transfer function can be obtained as shown in (53) at the bottom of the page. The analytical model developed in this section is valid at any input–output and load condition as long as the boost converter operates in the continuous conduction mode. For validation of the developed low-frequency small-signal model the operating point of Fig. 8 is chosen. The component values of the experimental boost rectifier unit are also indicated in the same figure.

Fig. 9 shows the Bode plot of the control gain transfer function $G_v(s)$ that is obtained by analysis. The measurement results of the control transfer function are obtained from the boost rectifier experimental unit by using Schlumberger 1250 frequency-response analyzer (FRA) instrument. These results are placed on the same figure for easy comparison. The dc input voltage of the modulator is $V_m = 6.54$ V. It produces an output voltage of $V_o = 300$ V, that is the maximum voltage rating of the FRA channel, at $V_g = 110$ V and at load resistance of $R = 606$ Ω.

It can be seen that qualitatively the analysis and the measurement results match each other very closely if the ESR of the capacitor ($\tan\delta = 0.2$ at 120 Hz) is taken into consideration. This validates our choice of rms voltage as the nominal operating point in a cycle of the input voltage waveform. A closed loop

$$
G_v(s) = \frac{\widehat{V_o}(s)}{\widehat{V_m}(s)} = \frac{-\left[\dfrac{1}{N}\dfrac{s}{RC} - \dfrac{1}{N}\dfrac{(1-D)^2}{LC}\right]}{s^2 + s\left[\dfrac{1}{RC} + \dfrac{1}{N}\dfrac{D}{RC}\dfrac{R_sT_s}{L} + \dfrac{1}{N}\dfrac{R_s}{L}\right] + \left[\left(\dfrac{(1-D)^2}{LC}\right)\left\{1 - \dfrac{1}{N}\dfrac{DR_sT_s}{L}\right\} + \left\{\dfrac{2}{N}\dfrac{R_s}{R}\dfrac{1}{LC}\right\}\right]} \qquad (53)
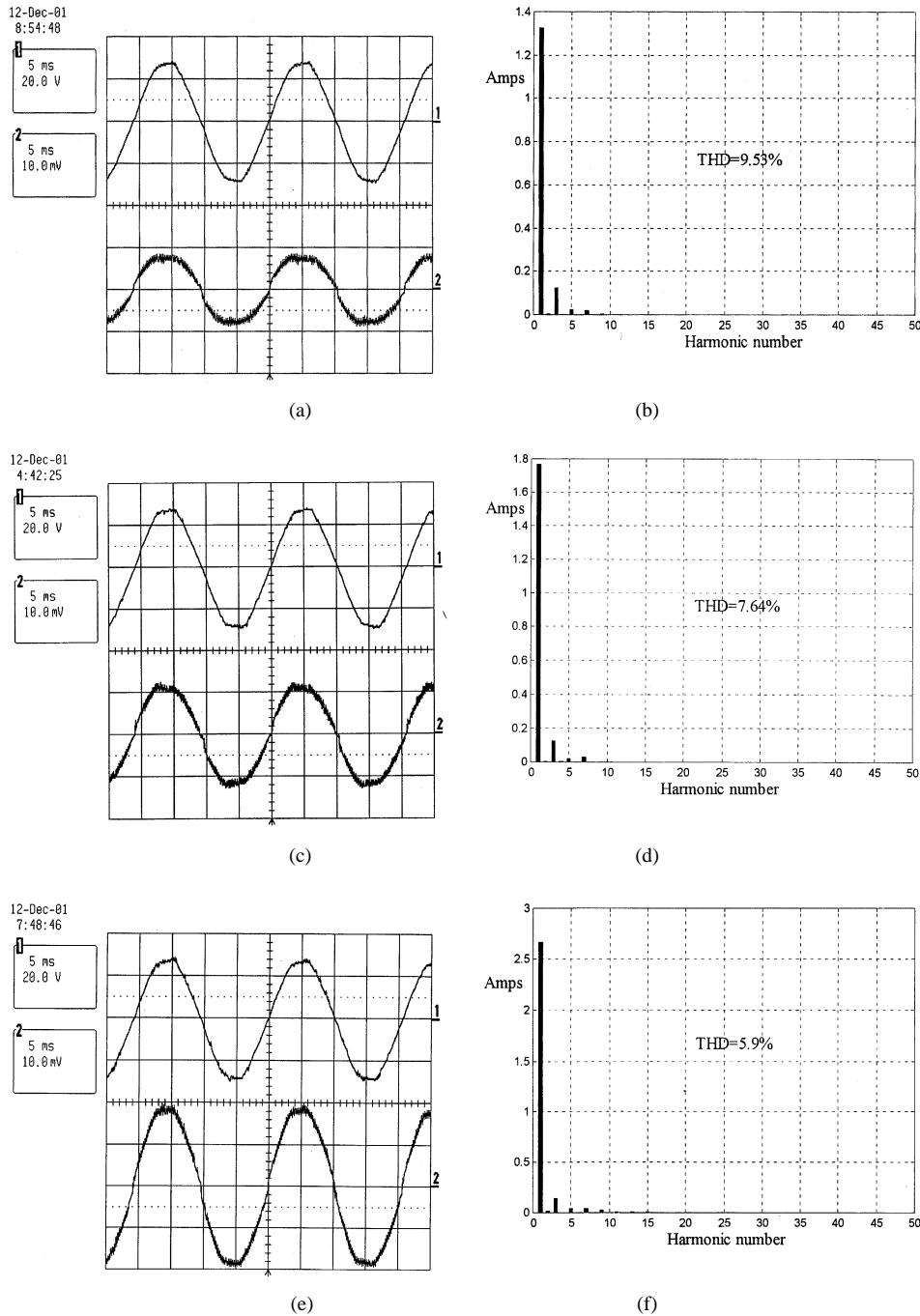$$

Fig. 12. Experimental results of the PSM switched boost rectifier. (a), (c), and (e) Ch1: V_{in} input voltage (230 V/div), Ch2: I_{in} input current (1.75 A/div). (b), (d), and (f) show harmonic spectrum of the corresponding input current at: (a), (b) $V_o = 400$ V, $V_{in} = 220$ V, $R = 875$ Ω, (c), (d) $V_0 = 400$ V, $V_{in} = 220$ V, $R = 600$ Ω, and (e), (f) $V_0 = 400$ V, $V_{in} = 220$ V, $R = 380$ Ω.

controller for the outer voltage loop can now be designed, based on the control transfer function given by (53), using the standard method available in linear control theory. The small-signal model of [2] is developed using power output = power input (POPI) concept [7]. The control gain transfer function of [2] is first order that can effectively be used to design the frequency response of the voltage error amplifier. Usually for power factor correction circuit the closed loop bandwidth is chosen around 5–10 Hz. Therefore the small-signal model developed here, even though accurate for higher frequency of operation compared to [2], has no added advantage so far as the design of the closed

loop controller is concerned. However, this model has been derived following the standard technique used by power supply designers in determining the small-signal model of a current mode controlled dc–dc converter. It is shown here that with proper choice of the nominal operating point in a line cycle a second order model of the boost rectifier can be obtained. This model equates the frequency response of the model in [2] in the low-frequency range. It may also be noted that the derivation of the small-signal model need not be performed manually because standard computer aided design tools are nowadays available for small-signal analysis of dc–dc converters.

VI. EXPERIMENTAL RESULTS

A 400 W boost rectifier is built to experimentally verify the PSM control method described in the previous sections of this paper. The output voltage of the rectifier is regulated at 400 V dc. Fig. 10 shows the circuit that generates the carrier waveform of the PSM. It can be seen that two reset integrators are enough for the generation of the carrier waveform. In comparison the NLC implementation of [2] needs an additional reset integrator for computation of the average current of the switch.

The following equations are used to select the circuit components

$$R_1 C_1 = \frac{L}{R_s} \tag{54}$$

$$2R_2 C_2 = T_s. \tag{55}$$

R_s is the equivalent current sensing resistance and L is the inductance of the boost rectifier. The modulator waveforms of the experimental single phase boost rectifier switched by the predictive switching modulator (PSM) are shown in Fig. 11(a)–(d). It can be seen that under regulated output voltage condition the shape of the carrier waveform changes with the variation of the operating input voltage. In this implementation the current sensing resistance is $R_s = 1.98\ \Omega$ and the sensed current signal is reset at the beginning of every switching cycle to avoid generation of noise related turn off pulses. The experimental waveforms of the input voltage and input current at different load conditions are shown in Fig. 12(a), (c), and (e). The harmonic spectrum of the corresponding input current is shown in Fig. 12(b), (d), and (f), respectively. The harmonic distortion of the input voltage waveform is 2.02%. It can be seen that the power factor of the boost rectifier is almost unity. The total harmonic distortion of the input current is less than 10% over a load range of 422 W to 180 W.

VII. CONCLUSION

In this paper, a PSM for high power factor operation of boost rectifier has been proposed. The modulator implements the switching function in such a way that the actual current lies on the top of a reference current profile that has the same shape as the input voltage waveform. This is achieved without sensing of the input voltage and without the use of a multiplier in the control circuit. The advantage of PSM is that it is able to extend the continuous conduction mode of operation over a wide range of variation of M_g, i.e., for $(0 < M_g < 0.86)$, compared to NLC. Circuit realization of the PSM is simple. It requires two reset integrators instead of three as would be required for NLC. It is shown that structurally the PSM can be configured as a current mode controller, with a dc reference and a linear and a nonlinear compensating ramp. The steady-state stability condition for the PSM switched boost rectifier is obtained by graphical analysis. Small-signal low-frequency model of the boost rectifier is derived by perturbing the converter states and inputs at the nominal operating point of input voltage rms. The small-signal model has been experimentally verified. The controller has been tested in hardware by building a 400 W boost rectifier prototype unit. Very low THD in the input current has been obtained over a wide range of loads.

REFERENCES

[1] J. P. Gegner and C. Q. Lee, "Linear peak current mode control: A simple active power factor correction control technique for continuous conduction mode," in *Proc. IEEE PESC'96 Conf.*, 1996, pp. 196–202.
[2] D. Maksimovic, Y. Jang, and R. Erickson, "Nonlinear-carrier control for high power factor boost rectifiers," in *Proc. IEEE APEC'95 Conf.*, 1995, pp. 635–641.
[3] S. Hsu, A. Brown, L. Rensink, and R. D. Middlebrook, "Modeling and analysis of switching dc-to-dc converters in constant-frequency current-programmed mode," in *Proc. PESC'79 Conf.*, 1979, pp. 284–301.
[4] R. Zane and D. Maksimovic', "Nonlinear-carrier control for high-power-factor rectifiers based on up–down switching converters," *IEEE Trans. Power Electron.*, vol. 13, pp. 213–221, Mar. 1998.
[5] R. D. Middlebrook and S. M. C'uk, "A general unified approach to modeling switching converter power stages," in *Proc. IEEE PESC'76 Conf.*, 1976, pp. 18–34.
[6] F. Dong Tan and R. D. Middlebrook, "A unified model for current-programmed converters," *IEEE Trans. Power Electron.*, vol. 10, pp. 397–408, July 1995.
[7] S. Singer and R. Erickson, "Canonical modeling of power processing circuits based on the POPI concept," *IEEE Trans. Power Electron.*, vol. 7, pp. 37–43, Jan. 1992.
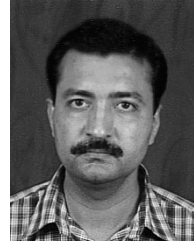
Souvik Chattopadhyay received the B.E. degree in electrical engineering from Bengal Engineering College, Howrah, India, in 1988, and the M.Sc. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 1990, where he is currently pursuing the Ph.D. degree in the Power Electronics Laboratory, Department of Electrical Engineering.

From 1991 to 1995, he was with M/S Crompton Greaves, Ltd., Bombay, India, as a Research and Development Engineer in the Power Electronics Group of R&D (Electricals). From 1996 to 1998, he was with M/S Cegelec India, Ltd., Delhi, India, as a Project Engineer dealing with industrial drives. His research interests include design, analysis, control, and modeling of power converters for PFC circuits and active filter systems.

V. Ramanarayanan received the B.E. degree from the University of Madras, Madras, India, in 1970, the M.E. degree from Indian Institute of Science, Bangalore, India, in 1975, and the Ph.D. degree from California Institute of Technology, Pasadena, in 1986.

He is a Professor and Chairman of the Department of Electrical Engineering, Indian Institute of Science, Bangalore, India. He had held positions in industry as a Senior Design Engineer and Chief of R&D with M/S Larsen and Toubro, Ltd. (1970–1979) and NGEF, Ltd. (1979–1982). His areas of interest include power electronics, industrial drives, switched-mode power conversion, and power quality issues. He is a Consultant to several industries in related areas.
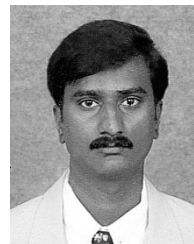
V. Jayashankar received the B.E. degree from the M.V. Institute of Technology, Bangalore, India, in 1997, and the M.E. degree from the U.V. College of Engineering, Bangalore, India, in 1999, both in electrical engineering with an emphasis on power electronics.

He was a Project Associate, Department of Electrical Engineering, Indian Institute of Science, Bangalore, from 1999 to 2001. In 2002, he joined the GE Medical Systems, Bangalore, India, as a Design Engineer. His research interests are primarily in power electronic converters and their control and power factor correction issues.