A PWM Plus Phase-Shift Control Bidirectional DC–DC Converter

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***Abstract*—A pulse-width modulation (PWM) plus phase-shift control bidirectional dc–dc converter is proposed. In this converter, PWM control and phase-shift control are combined to reduce current stress and conduction losses, and to expand ZVS range. The operation principle and analysis of the converter are explained, and ZVS condition is derived. A prototype of PWM plus phase-shift bidirectional dc–dc converter is built to verify the analysis.**

***Index Terms*—Bidirectional dc–dc converter, conduction loss, phase-shift, pulse-width modulation.**

I. Introduction

BIDIRECTIONAL dc–dc converters will be widely used in applications such as dc uninterrupted power supplies, aerospace power systems, electric vehicles and battery chargers. In order to minimize the size and weight of the converters, switching frequency must be increased. But the increase of switching frequency results in higher switching losses. There are many techniques to solve this problem. Some circuits use resonant, quasiresonant, and/or multi-resonant techniques [1]–[3]. However, voltage or current stresses in these converters are higher and require the devices of higher VA rating. Some circuits use passive snubbers or active clamp techniques [4]. However, these converters become more complicated. Phase-shift ZVS technique has been used in bidirectional dc–dc converters since it can realize ZVS for all switches without auxiliary switches [5], [6]. However, when the amplitude of input voltage is not matched with that of output voltage, the current stresses and RMS currents of the converters become higher. In addition the converters can not achieve ZVS in light-load condition.

Fig. 1 is a phase-shift (PS) bidirectional dc–dc converter [7]. There are two switches on both sides of the isolation transformer. Switch M_1 and M_2 are controlled complementarily. Switch M_3 and M_4 are also controlled complementarily. Duty cycles of the switches are kept in 0.5. The inductor L_1 is used as the main energy transfer element. Fig. 1 is simplified as Fig. 2(a). Fig. 3(a) shows the corresponding waveforms of the simplified circuit when the amplitude of equivalent input voltage (V_{ab}) is equal to that of equivalent output voltage

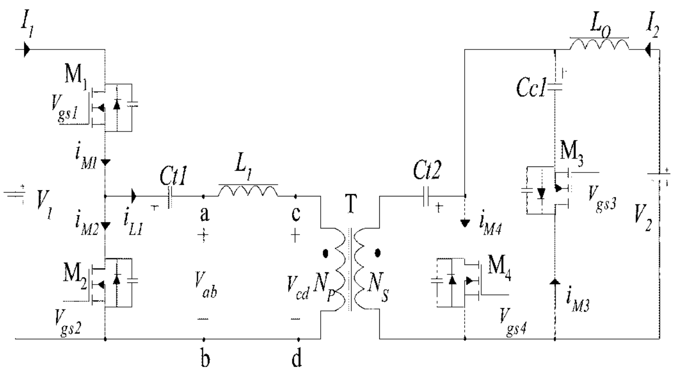
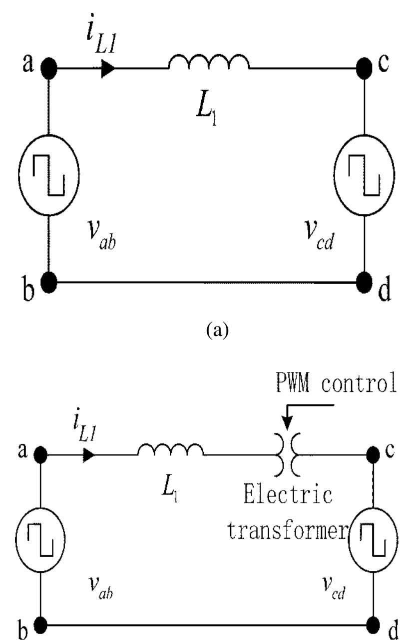


Fig. 1. Phase-shift bidirectional dc–dc converter.



(a)

(b)

Fig. 2. (a) Simplified circuit of PS control. (b) Simplified circuit of PPS control.

(V_{cd}), that is $V_1/2 = NV_2$, where $N = Np/Ns$ is the turn ratio of the isolation transformer. When the amplitude of equivalent input voltage (V_{ab}) is not equal to that of equivalent output voltage (V_{cd}), such as $V_1/2 < NV_2$, Fig. 3(b) shows the corresponding waveforms. The current stresses and RMS

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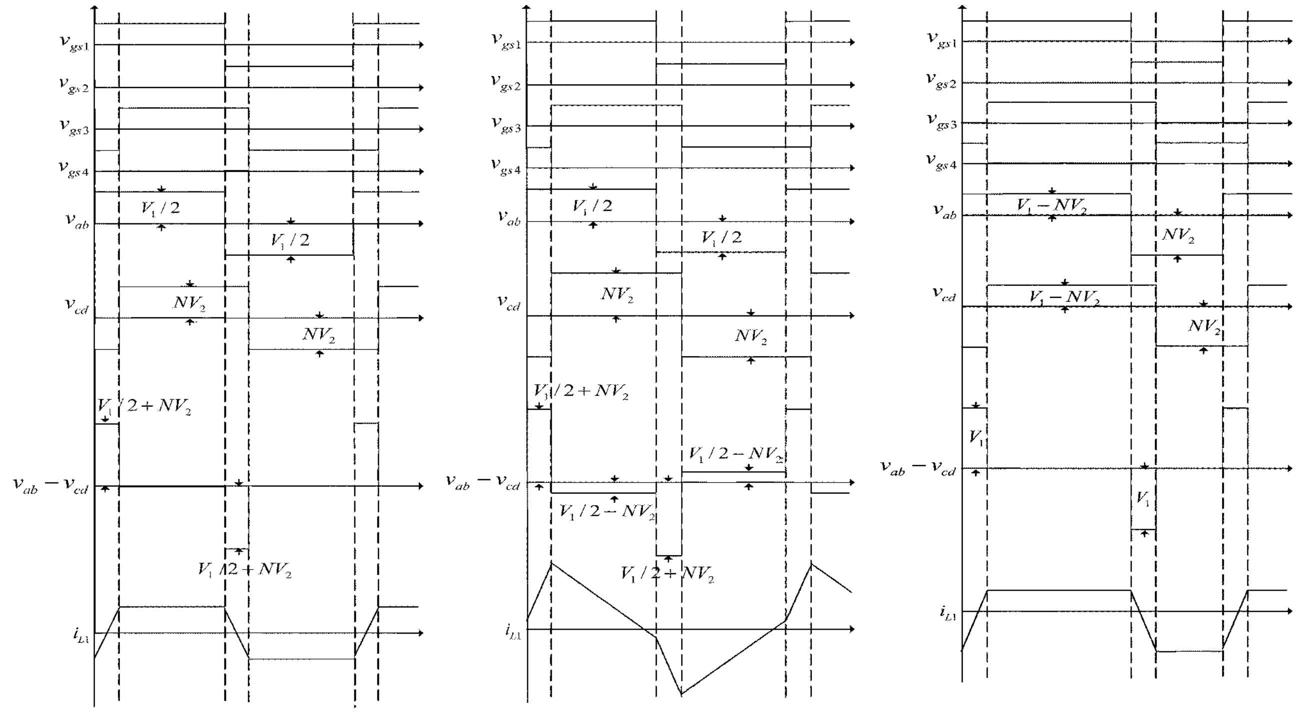


(a) (b) (c)

Fig. 3. (a) PS control when $V_1/2 = NV_2$. (b) PS control when $V_1/2 = NV_2$. (c) PPS control when $V_1/2 = NV_2$.

currents of the converter become much higher and the reactive power transferred also increases, which leads to higher current stresses of the switch devices and higher conduction losses. The converter can not achieve ZVS in light-load condition.

This paper proposes a PWM plus phase-shift (PPS) control bidirectional dc–dc converter. Fig. 2(b) shows concept of PPS control bidirectional dc–dc converter. The PWM control of duty cycles acts as an electric transformer between equivalent input voltage (V_{ab}) and equivalent output voltage (V_{cd}), so that both positive and negative amplitudes of equivalent input voltage (V_{ab}) are equal to those of equivalent output voltage (V_{cd}). Fig. 3(c) shows the corresponding waveforms of the simplified circuit of PPS control bidirectional dc–dc converter. Compared with PS control, PPS control can reduce the current stresses and RMS currents of the converter. The losses of the converter can also decrease. Later, it will be proved that the converter can achieve ZVS in larger load variation.

II. Operation Principle of PPS Control Converter

To simplify the analysis, the operation of PPS control converter is explained with the following assumptions.

1) The converter has reached steady state.
2) All switch devices are assumed as ideal switches with parallel body diodes and parasitic capacitors.
3) The inductance L_1 is composed of the leakage inductance of the transformer and additional series inductance.
4) The values of the capacitors $Ct1, Ct2$, and $Cc1$ are so large that the voltage ripples across them are small.
5) The resonant frequency of capacitor (composed of $Ct1, Ct2$, and $Cc1$) and L_1 is much lower than the switching frequency of the converter.

Duty cycles of M_1 and M_3 are D, and duty cycles of M_2 and M_4 are 1-D. In the forward mode, the gate drive signals of M_1 and M_2 is leading to those of M_3 and M_4 so that power flows from V_1 to V_2. The equivalent circuits and key waveforms in the forward mode are shown in Figs. 4 and 5, respectively. The switching cycle can be divided into eight stages which are explained as follows.

1) Stage 1 $(t_0 - t_1)$*:* Just before t_0, M_4 is turned off. M_1 is on. The current i_{L1} is in positive direction. The capacitor in parallel with M_4 is charged, while the capacitor in parallel with M_3 is discharged. The voltage across M_3 decreases to zero at t_0 and M_3's body diode starts to conduct. M_3 is turned on with ZVS and then works as a synchronous rectifier. The voltage across M_4 is clamped at V_{Cc1}. The current slopes of L_1 is

$$\frac{di_{L1}}{dt} = \frac{V_1 - V_{Ct1} + NV_{Ct2} - NV_{Cc1}}{L_1} \tag{1}$$

where $V_{Ct1}, V_{Ct2}, V_{Cc1}$ are average voltages of $Ct1, Ct2$, and $Cc1$, respectively.

2) Stage 2 $(t_1 - t_2)$*:* M_1 is turned off at t_1. The capacitor in parallel with M_1 is charged linearly by the current i_{L1} and the capacitor in parallel with M_2 is discharged. The stage terminates at t_2, while the voltage across M_2 is zero.

3) Stage 3 $(t_2 - t_3)$*:* M_2's body diode starts to conduct at t_2. Then M_2 is turned on in zero-voltage condition. The current

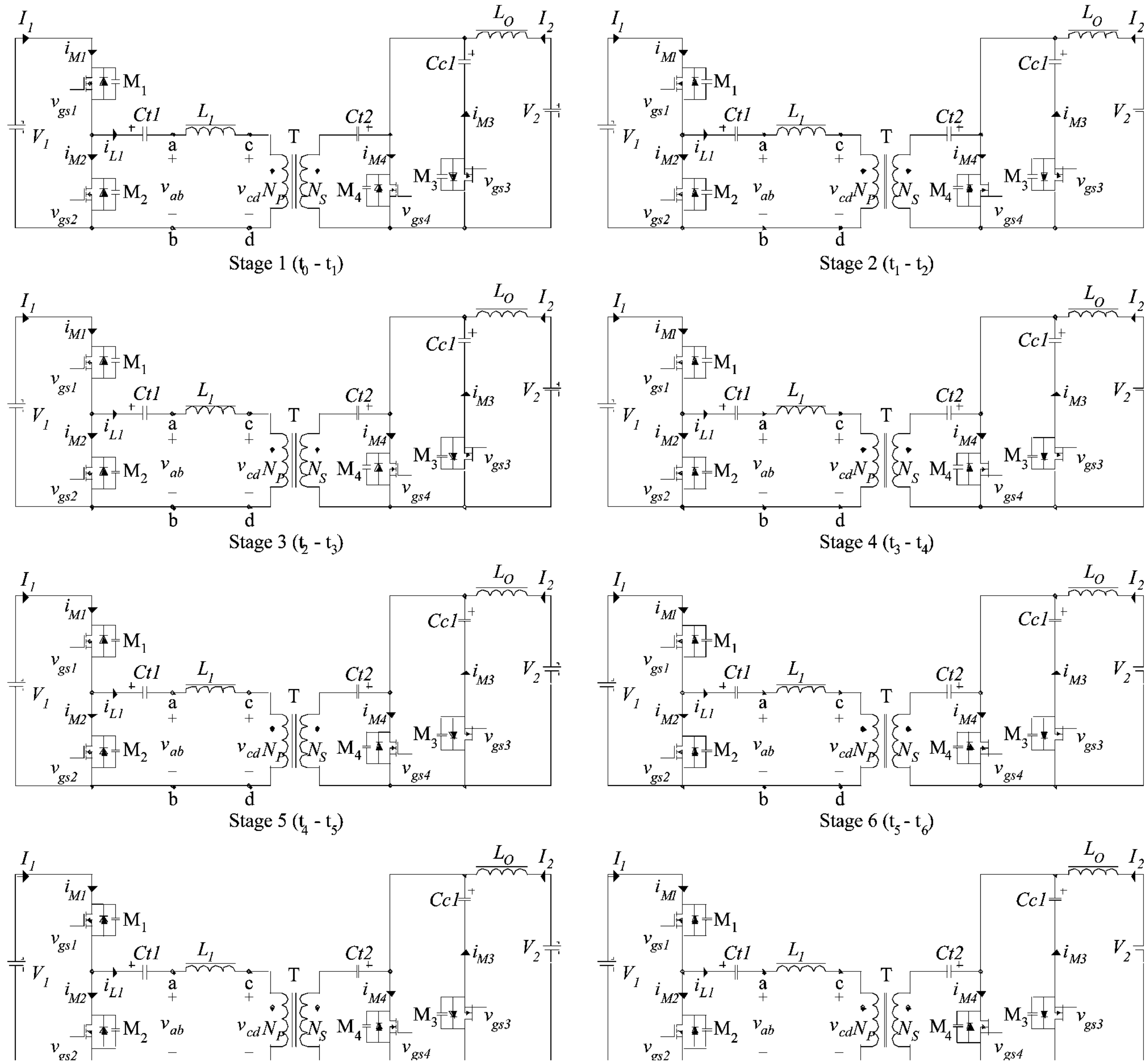


Fig. 4. Operation stages of the converter in the forward mode.

i_{L1} decreases linearly and its direction is changed from positive to negative. The slope of i_{L1} is

$$\frac{di_{L1}}{dt} = \frac{-V_{Ct1} + NV_{Ct2} - NV_{Cc1}}{L_1}. \tag{2}$$

4) Stage 4 $(t_3 - t_4)$*:* At t_3, M_3 is turned off. The capacitor in parallel with M_3 is charged and the capacitor in parallel with M_4 is discharged linearly. At the end of this stage, the voltage across M_4 decreases to zero.

5) Stage 5 $(t_4 - t_5)$*:* The body diode of M_4 is conducting at the beginning of this stage. Therefore M_4 is turned on in zero-voltage condition. The slope of i_{L1} is

$$\frac{di_{L1}}{dt} = \frac{-V_{Ct1} + NV_{Ct2}}{L_1}. \tag{3}$$

6) Stage 6 $(t_5 - t_6)$*:* At t_5, M_2 is turned off. The capacitor in parallel with M_2 is charged and the capacitor in parallel with M_1 is discharged linearly. At the end of this stage, the voltage across M_1 goes down to zero.

7) Stage 7 $(t_6 - t_7)$*:* At the beginning of this stage, the body diode of M_1 is conducting and M_1 is turned on in zero-voltage condition. The slope of i_{L1} is

$$\frac{di_{L1}}{dt} = \frac{V_1 - V_{Ct1} + NV_{Ct2}}{L_1}. \tag{4}$$

8) Stage 8 $(t_7 - t_8)$*:* At t_7, M_4 is turned off. The capacitor in parallel with M_4 is charged and the capacitor in parallel with M_3 is discharged linearly until the voltage across M_3 reaches zero. After t_8, the next switching cycle starts again.

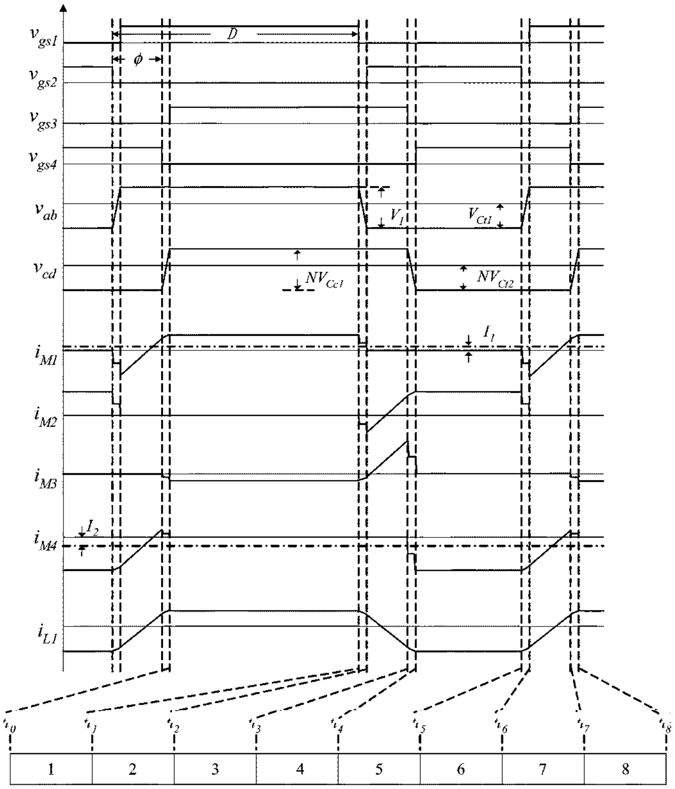


Fig. 5. Steady-state waveforms of the converter in the forward mode.

On the contrary, in the backward mode, the gate drive signals of M_3 and M_4 are leading to those of M_1 and M_2. The equivalent circuits and key waveforms in the backward mode are shown in Figs. 6 and 7, respectively. The switching cycle can also be divided into 8 stages. The principle of operation of the backward mode (power flows from V_2 to V_1) is similar to that of the forward mode, so it will not be explained in this paper.

III. Analysis of Converter

A. Low-Frequency Average Model

We use 2π to represent one switching cycle. ϕ is the phase shift between two cells, which are connected by the transformer. ϕ is defined to be positive when $V_{\rm gs1}$ is leading to $V_{\rm gs3}$ in phase. The duty cycles of M_1 and M_3 are D, and duty cycles of M_2 and M_4 are 1-D.

PWM control is used to regulate the positive amplitude of equivalent input voltage to be equal to that of equivalent output voltage and at the same time the negative amplitude of equivalent input voltage is regulated to be equal to that of equivalent output voltage. Hence the slope of the current i_{L1} is zero in stage 1 and stage 5. In other words, the duty cycles of M_1 and M_3 are

$$D = \frac{NV_2}{V_1}. \tag{5}$$

Referring to the Appendix A, the power flows from V_1 to V_2 under PPS control

$$P = \frac{\phi NT}{8\pi^2 L_1}\left(-|\phi| V_1^2 - 4\pi V_2^2 N^2 + 4\pi V_1 V_2 N\right) \tag{6}$$

where T is operation period.

Referring to the Appendix B, the current stress of inductor L_1 under PPS control

$$I_{L1\max} = \max\{|i_{L1}|, |i_{L3}|\} = \max\left\{\frac{V_1 - NV_2}{V_1^2 L_1}A, \frac{NV_2}{V_1^2 L_1}A\right\} \tag{7}$$

where $A = TV_1NV_2 - TN^2V_2^2 - \sqrt{T(TV_1^2N^2V_2^2 - 2TV_1N^3V_2^3 + TN^4V_2^4 - 2V_1^2PL_1)}$.

The power flows from V_1 to V_2 under PS control [7]

$$P = \frac{\phi NTV_1V_2}{4\pi^2 L1}(\pi - |\phi|). \tag{8}$$

The current stress of inductor L_1 under PS control [7]

$$I_{L1\max} = \max\left\{\frac{TV_1^2 - 2\sqrt{TV_1NV_2(TV_1NV_2 - 16PL_1)}}{8V_1L_1}\right. \\ \left.\frac{2TN^2V_2^2 - \sqrt{TV_1NV_2(TV_1NV_2 - 16PL_1)}}{8NV_2L_1}\right\}. \tag{9}$$

B. Current Stress Comparison

Fig. 8 shows current stress of inductor L_1 under PS control in the following conditions: $V_1 = 48$ Vdc, $V_2 = 20$ Vdc–30 Vdc, $Np{:}Ns = 1{:}1, P = 100$ W, switching frequency $f = 100$ kHz, inductance $L_1 = 1$ μH–6 μH. From Fig. 8 we can see that the smaller the value of inductance L_1 is, the lower current stress is when output voltage is 24 V. In other words, input voltage and output voltage match. On the contrary, when input voltage and output voltage do not match, such as output voltage is 30 V, the smaller the value of inductance L_1 is, the higher current stress is. It is difficult to design the value of inductance L_1 when two aspects above are considered.

Here a method to optimize the value of inductance L_1 is proposed. Current stress $I_{L1\max}$ is averaged within the range of output voltage. Average current stress $I_{\rm AV}$ is used to determine the value of inductance L_1

$$I_{\rm AV} = \frac{\int_{V_{2\min}}^{V_{2\max}} I_{L1\max} dV_2}{V_{2\max} - V_{2\min}}. \tag{10}$$

The variation of average current stress under PS control, $I_{\rm AV}$, as a function of value of inductance L_1 is plotted in Fig. 9(a) from which we can find that average current stress $I_{\rm AV}$ is minimum when the value of inductance is 4.4 μH. Fig. 9(b) shows average current stress under PPS control versus value of inductance L_1. But we are hardly to find the minimum average current stress since the smaller value of inductance is, the lower

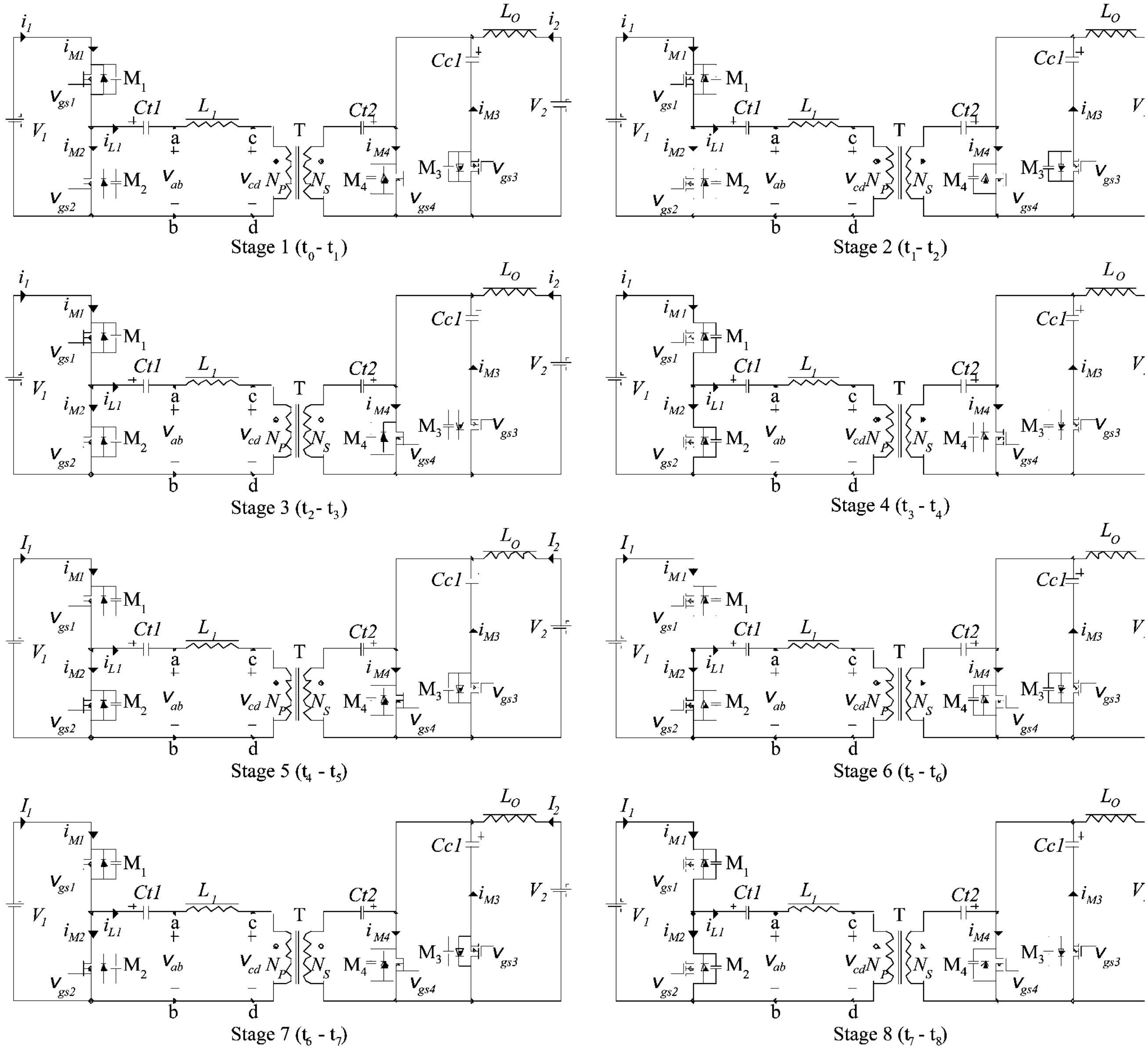


Fig. 6. Operation stages of the converter in the backward mode.

average current stress is. But the smaller value of inductance L_1 is, the smaller the phase-shift angle is, and the more difficult the converter is, is controlled. Here we assume the minimum phase-shift angle is 20°. Value of inductance L_1 under PPS control is given in previous conditions

$$L_1 = \frac{V_1^2 T}{81P} = \frac{48 \times 48 \times \frac{1}{100\,000}}{81 \times 100} = 2.844\ \mu\text{H}. \qquad (11)$$

Fig. 10(a) shows current stress of inductor L_1 under PS control and under PPS control in the following conditions: $V_1 = 48$ Vdc, $V_2 = 20$ Vdc–30 Vdc, $Np{:}Ns = 1{:}1$, $P = 100$ W, switching frequency $f = 100$ kHz, inductance $L_1 = 1\ \mu$H–6 μH. From it we can see that PPS control can reduce current stress except that the value of the inductance L_1 is large enough.

Pspice simulation results and calculation results derived from (7) under PPS control, Pspice simulation results and calculation results derived from (9) under PS control are compared in Fig. 10(b). From it we can see that the Pspice simulation traces and calculation results are in a good agreement, PPS control can reduce current stress.

C. ZVS Range Comparison

The ZVS range under PS control is [7]

$$|\phi| > \max\left(\frac{\pi}{2} - \frac{\pi V_1}{4NV_2}, \frac{\pi}{2}\sqrt{2 - 4\frac{NV_2}{V_1}}\right). \qquad (12)$$

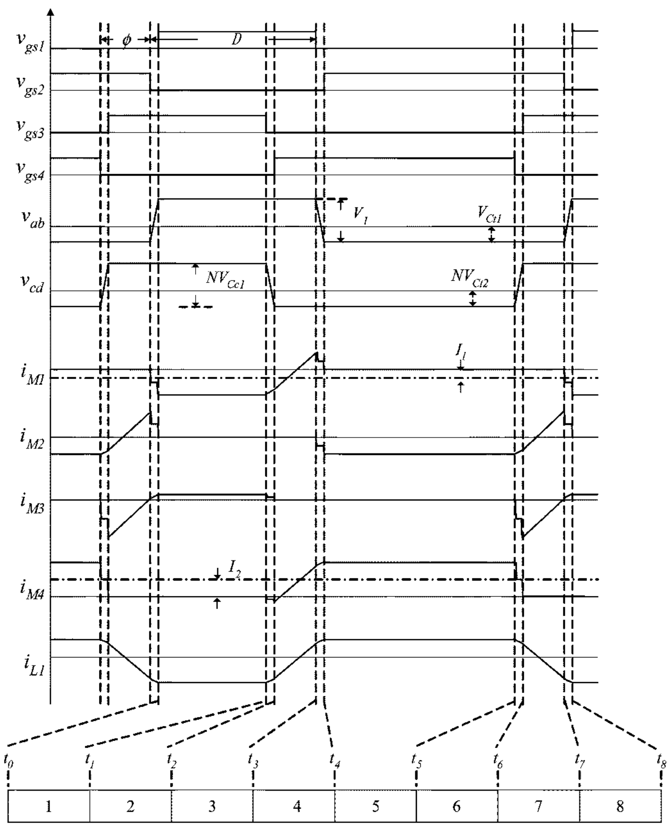


Fig. 7. Steady-state waveforms of the converter in the backward mode.

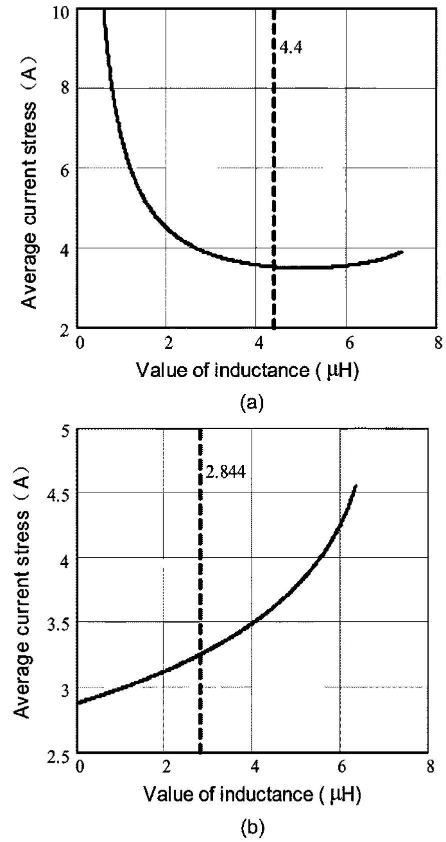


Fig. 9. Average current stress versus value of inductance L_1. (a) PS control. (b) PPS control.

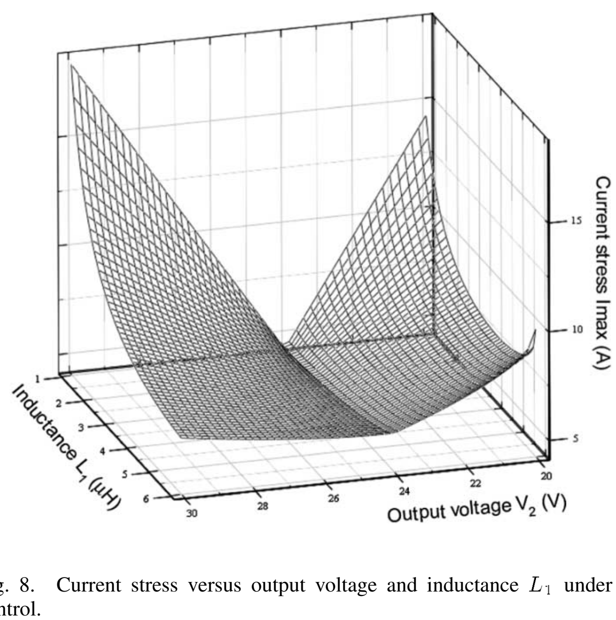


Fig. 8. Current stress versus output voltage and inductance L_1 under PS control.

Fig. 11 shows ZVS range under PS control.

Referring to the Appendix C, the ZVS range under PPS control is

$$|\phi| > 0. \tag{13}$$

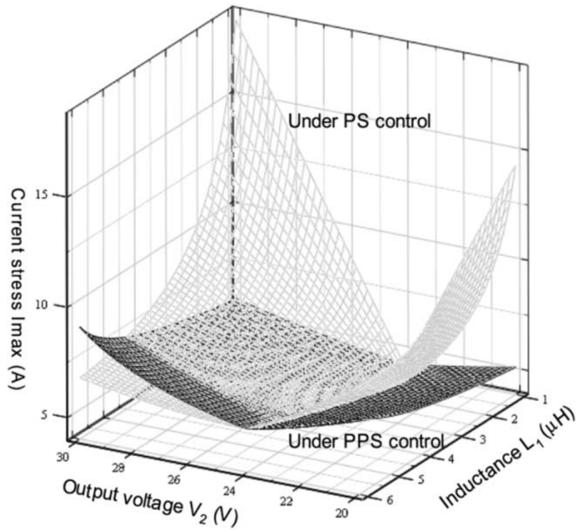
In other words, the converter under PPS control can maintain ZVS in larger load variation. Hence PPS control can expand ZVS range.

IV. Experimental Results

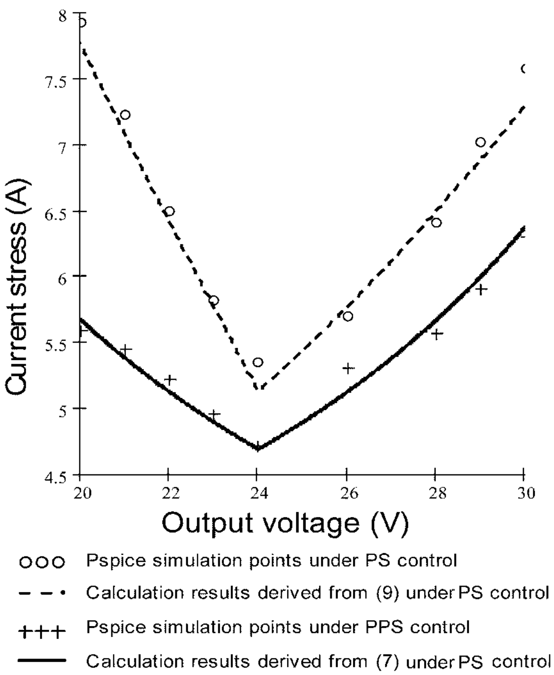
Fig. 12 shows the system block diagram of the proposed converter. UC3875 generates signal g1 and signal g2. Signal g1 has leading phase according to the error signal of command power (Po*) and actual power (Po) to signal g2. Signal g1 and signal g2 connect to UC3525 respectively. Signal g1 has the same phase as $vgs1$ and signal g2 has the same phase as $vgs3$. The signalNV_2/V_1 modulates the duty cycles of $vgs1$ and $vgs3$. By inverting $vgs1$ and $vgs3$, we can get other two gate signals.

A prototype of PPS control bidirectional dc–dc converter is built to verify the analysis. Experiments are performed in the following conditions: $V_1 = 48$ Vdc, $V_2 = 24$ Vdc–30 Vdc, $Np{:}Ns = 1{:}1, L_0 = 150$ μH, $Ct1 = Ct2 = 13$ μF, $Cc1 =$ 2.2 μF, $L_1 = 4.4$ μH (PS control), $L_1 = 2.8$ μH (PPS control), switching frequency f =100 kHz, M_1–M_4: *MOSFET IRF540 (IR)* (referring to Appendix D).

Fig. 13 shows experimental waveforms in $V_2 = 24$ Vdc with 100 W output power condition. Since input voltage V_1 and output voltage V_2 match in this case, current stress of inductance L_1 between PS control and PPS control is the same.



(a)



(b)

Fig. 10. (a) Current stress versus output voltage and inductance L_1 under PS control and under PPS control. (b) Current stress versus output voltage.

Fig. 14 shows experimental waveforms in $V_2 = 30$ Vdc with 100 W output power condition. In this case, input voltage V_1 and output voltage V_2 do not match. Therefore, current stress of inductor L_1 with PS control is higher than that of PPS control. Fig. 15 gives curves of current stress versus output voltage under PS and PPS control respectively. From the experimental waveforms and curves, we can easily see that PPS control can reduce current stress and reduce conduction losses.

Fig. 16 shows experimental waveforms in $V_2 = 30$ Vdc with 30 W output power condition. The converter under PS control can not achieve ZVS, while the converter under PPS control

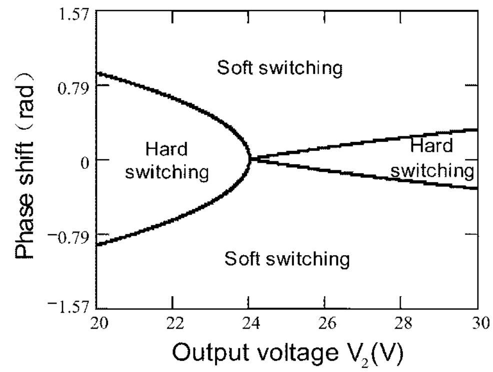


Fig. 11. ZVS range versus output voltage under PS control.

can still hold ZVS. Therefore, PPS control can reduce switching losses.

Fig. 17 shows the efficiency curves of the converter under PS and PPS control. It can be easily found that PPS control has higher efficiency than PS control, especially in light-load condition.

V. Conclusion

A PWM plus phase-shift control bidirectional dc–dc converter is proposed in this paper. From the theoretical analysis and the experiments, it can be found that PPS control has the following features.

1) PPS control reduces current stress, conduction losses and switching losses of devices.
2) The converter under PPS control can achieve ZVS in a larger load variation.

Appendix A

From Fig. 5, we can see that average voltage of inductance L_1 in one period is zero

$$DV_1 - V_{Ct1} + NV_{Ct2} - DNV_{Cc1} = 0. \tag{A1}$$

Average voltage of inductance L_M in one period is also zero

$$-V_{Ct2} + DV_{Cc1} = 0. \tag{A2}$$

Average voltage of output inductance L_o in one period is zero too

$$DV_{Cc1} - V_2 = 0. \tag{A3}$$

Average current of capacitance $Cc1$ in one period is zero

$$4\pi D\phi TN(V_{Ct1} - NV_{Ct2} + NV_{Cc1} - V_1) + 8\pi^2 L_1(DI_2 - NI_1) + \phi^2 TN(-NV_{Cc1} + V_1) = 0. \tag{A4}$$

According to the law of conservation of energy, the following equation is obtained:

$$V_1 I_1 + V_2 I_2 = 0. \tag{A5}$$

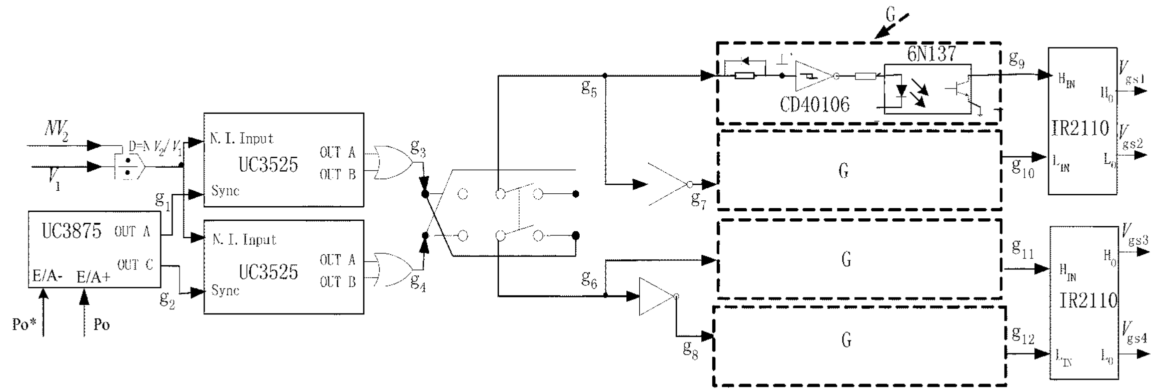


Fig. 12. System block diagram of the proposed converter.

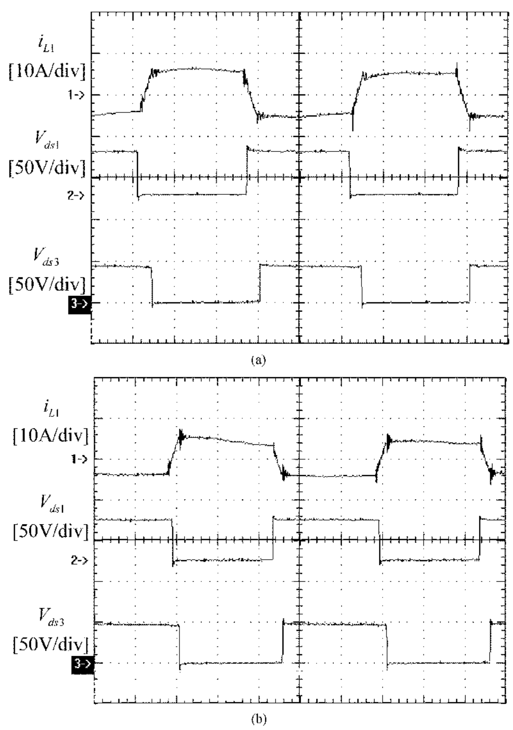


Fig. 13. Experimental waveforms in $V_2 = 24$ Vdc (100 W-output) condition (2 us/div). (a) PS control. (b) PPS control.

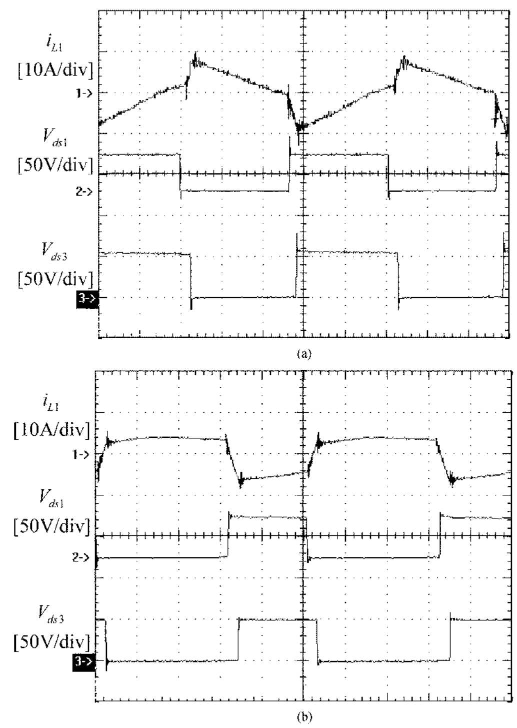


Fig. 14. Experimental waveforms in $V_2 = 30$ Vdc (100 W-output) condition (2 us/div). (a) PS control. (b) PPS control.

The output current of the converter in bidirectional operation can be obtained as following:

$$I_2 = \frac{\phi NT}{8\pi^2 L_1 V_2}\left(-|\phi|V_1^2 - 4\pi V_2^2 N^2 + 4\pi V_1 V_2 N\right). \quad \text{(A6)}$$

In bidirectional operation, the power transmitted through the converter can be expressed by

$$P = V_2 I_2 = \frac{\phi NT}{8\pi^2 L_1}\left(-|\phi|V_1^2 - 4\pi V_2^2 N^2 + 4\pi V_1 V_2 N\right). \quad \text{(A7)}$$

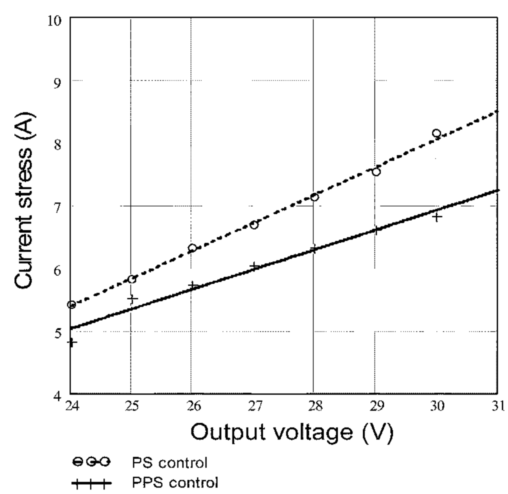


Fig. 15. Experimental result of current stress versus output voltage.

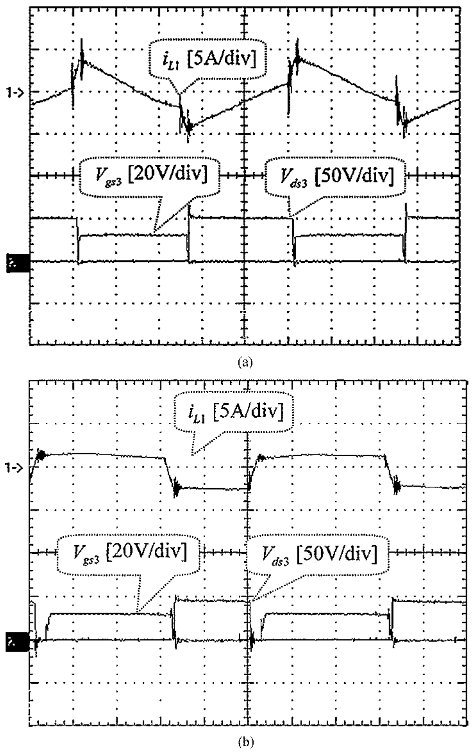


Fig. 16. Experimental waveforms in $V_2 = 30$ Vdc (30 W-output) condition (2 us/div). (a) PS control. (b) PPS control.

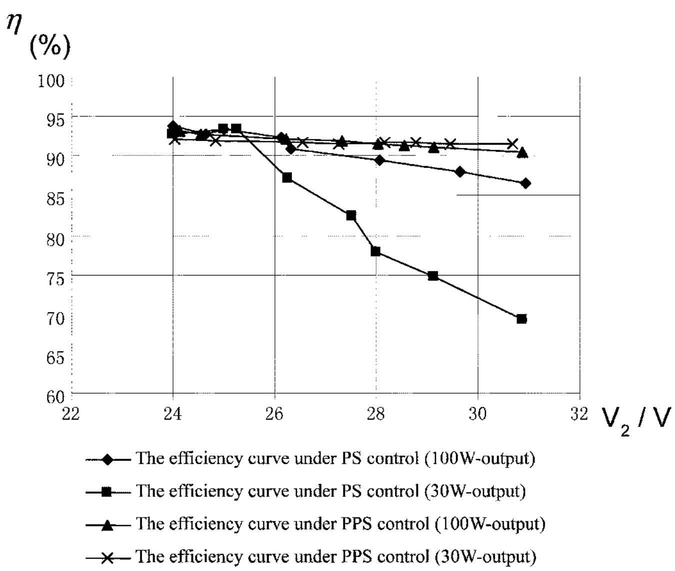


Fig. 17. Efficiency waveforms versus output voltage.

APPENDIX B

i_{L1}, i_{L3}, i_{L5}, and i_{L7} are the currents of inductance L_1 at t_1, t_3, t_5, and t_7.

We can derive the following equation from (1):

$$\frac{i_{L11} - i_{L17}}{(D - \phi/2\pi)T} = \frac{V_1 - V_{Ct1} + NV_{Ct2} - NV_{Cc1}}{L_1}. \tag{B1}$$

We can derive the following equation from (2):

$$\frac{i_{L13} - i_{L11}}{T\phi/2\pi} = \frac{-V_{Ct1} + NV_{Ct2} - NV_{Cc1}}{L_1}. \tag{B2}$$

We can derive the following equation from (3):

$$\frac{i_{L15} - i_{L13}}{(1 - D - \phi/2\pi)T} = \frac{-V_{Ct1} + NV_{Ct2}}{L_1}. \tag{B3}$$

Average current of inductance L_1 in one period is zero

$$\frac{i_{L11} + i_{L13}}{2}\frac{\phi}{2\pi} + \frac{i_{L13} + i_{L15}}{2}\left(1 - \frac{\phi}{2\pi} - D\right) + \frac{i_{L15} + i_{L17}}{2}\frac{\phi}{2\pi} + \frac{i_{L17} + i_{L11}}{2}\left(D - \frac{\phi}{2\pi}\right) = 0. \tag{B4}$$

i_{L1}, i_{L3}, i_{L5}, and i_{L7} can be obtained by combining (B1)–(B4)

$$i_{L1} = i_{L7} = \frac{V_1 - NV_2}{2\pi L_1}T\phi, i_{L3} = i_{L5} = -\frac{NV_2}{2\pi L_1}T\phi. \tag{B5}$$

Equation (7) can be obtained by combining (A7) and (B5).

APPENDIX C

In the forward mode, the converter can achieve ZVS on condition of

$$i_{L5} < 0 \quad (M_1 \text{ can be turned on with ZVS}) \tag{C1}$$

$$i_{L1} > 0 \quad (M_2 \text{ can be turned on with ZVS}) \tag{C2}$$

$$-Ni_{L13} + I_2 > 0 \quad (M_3 \text{ can be turned on with ZVS}) \tag{C3}$$

$$Ni_{L17} - I_2 > 0 \quad (M_4 \text{ can be turned on with ZVS}). \tag{C4}$$

The ZVS range under PPS control can be obtained by substituting (B5) into (C1)–(C4)

$$|\phi| > 0. \tag{C5}$$

APPENDIX D

The design of PPS control bidirectional dc–dc converter is illustrated on the prototype built for the following specifications: input voltage rating: 48 Vdc, output voltage rating: 24 Vdc, and it varies from 24 Vdc to 30 Vdc, maximum output power: 100-W, switching frequency: 100 kHz.

In order that duty cycles of M1 and M3 are 0.5 when input voltage and output voltage are equal to their rating value respectively, the turn ratio of the transformer can be derived from (5): 1:1.

In order to simplify the prototype, the same type of MOSFET is choosen. From (7) and (9), the current stress of M_1–M_4 can be calculated and it is 7.3 A. The voltage stress of M_1–M_4 is 60 Vdc when the converter is operated under PS control and the output voltage is 30 Vdc. Therefore, *IRF540* whose V_{DSS} is 100 Vdc and I_D is 28 A can satisfy this situation.

The value of the output inductance L_o can be calculated by $L_o = (TV_{2\max})/(4\Delta I_{\max})$ ($\Delta I_{\max}$ is the maximum ripple of the output current, here it is 0.5 A) and it is 150 μH.

The value of $Ct1, Ct2$, and $Cc1$ can be calculated by $C = (\int idt)/(\Delta U_{\max})$ ($\Delta U_{\max}$ is the maximum ripple of the voltage, here it is 1 V) and $Ct1 = Ct2 = 13\ \mu$F, $Cc1 = 2.2\ \mu$F.

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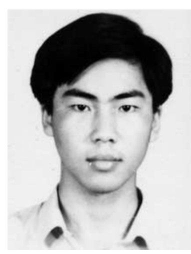

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