A Quadrature Switched Capacitor Power Amplifier

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Abstract—This paper presents an all-digital class-G quadrature switched-capacitor power amplifier (Q-SCPA) implemented in 65nm CMOS. It combines in-phase (I) and quadrature (Q) signals on a shared capacitor array. The *I/Q* signals are digitally weighted and combined in the charge domain. Quadrature summation results in a 3-dB signal loss; Hence the Q-SCPA utilizes a class-G dual-supply architecture to improve efficiency at backoff. Unlike polar/EER counterparts, the Q-SCPA requires no wideband phase modulator or delay matching circuitry. The Q-SCPA delivers a peak output power of 20.5 dBm with a peak PAE of 20%. It is measured with a 10-MHz, 64-QAM LTE signal and achieves an ACLR of <-30 dBc, with an EVM < 4%-rms.

Index Terms— Quadrature Transmitter, Switched-Capacitor PA, SCPA, Class-D PA, Digital PA, Class-G. RF-DAC

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I. Introduction

Consumer electronic devices for modern communication require transmitters with high power and high efficiency while simultaneously operating with high linearity and wide bandwidth. The low breakdown voltage of CMOS limits the practically achievable output power of power amplifiers operating in either switching or linear regimes. Linear amplifiers further operate with a finite quiescent current that limits their efficiency. Hence, non-linear switching amplifiers, such as class-D, -E and -F PAs, are widely used to implement RF power amplifiers. Switching amplifiers are shown to be more efficient than their linear amplifier counterparts and take advantage of CMOS scaling, which has made the device a lower loss, faster switch. However, switching amplifiers require linearization circuitry for normal operation on modern wideband linear communication signals (e.g., LTE, Wi-Fi, etc).

Several techniques have been investigated to linearize the RF power amplifiers (PA) implemented with switching PAs, including envelope elimination and restoration (EER) [1]–[5], polar modulation [6]–[8], digital PAs [9]–[16], Digital-Doherty [17], outphasing [18], and pulse-wave modulation [19], [20]. The techniques above require a conversion from the Cartesian to the polar coordinate system. In the digitally intensive versions, the Cartesian-to-polar conversion requires a complex coordinate rotation digital computer (CORDIC) and the resulting bandwidth expansion limits wideband operation required by current wireless standards [21], [22]. The Cartesian-to-polar transformation can be expressed as follows:

$$A(t) = \sqrt{I^2(t) + Q^2(t)}, \quad (1)$$

$$\phi(t) = tan^{-1}(Q(t)/I(t)). \quad (2)$$

Owing to the strong non-linearity associated with these conversions, the bandwidth required for the polar components $A(t)$ and $\phi(t)$, especially the phase component $\phi(t)$, are substantially larger than the bandwidth of the Cartesian components $I(t)$ and $Q(t)$ [21].

An alternative to techniques that require a polar conversion is to digitally modulate and sum the *I* and *Q* signals in the Cartesian domain, as shown in Fig. 1. In the past, summation in the quadrature domain has been performed with transformers [23], [24]. Due to interactions between the *I* and *Q* currents in the windings and due to memory effects, this technique requires precise duty-cycle control and/or digital predistortion. Several efforts have been made to perform the combination in the charge domain, on a capacitor array [25]–[27]. These techniques are more amenable to CMOS technology, as they do not require custom transformers, and are more linear due to low-loss switching and precision capacitor matching [14]. Further, duty-cycle control is not necessary, as long as the voltage on the capacitor array due to one input settles before the next input is entered (e.g., $I(t)$ must settle before $Q(t)$) [26]. In the capacitively combined versions, a capacitor array is divided into *I* and *Q* sub-arrays, each with a quantized number of unary/binary capacitor cells. The *I*/*Q* vectors can be represented simply by clocking the *Q* cells with a quadrature clock delayed by 90 degrees from the *I* clock; *I*/*Q* vectors can be weighted by controlling the number of cells that are switched in each sub-array. Four quadrant operation in the complex plane is achievable by appropriately inverting the *I* and *Q* clock signals. The output amplitude and phase are achieved by appropriate weighting of the *I*/*Q* signals; hence, this eliminates the need for a CORDIC, and a wideband supply modulator and phase modulator required for other realizations of Polar/EER PAs. Another direct benefit is that the *I*/*Q* vectors propagate at similar frequency with similar group delay. This obviates the need for delay synchronization circuitry necessary in many Polar/EER transmitters; careful, symmetric layout ensures proper timing alignment.

Because summation of quadrature signals results in a 3-dB loss when compared to summation of in-phase signals (e.g., polar modulation), amplifier efficiency is critical. Switching amplifiers are ideal for this operation, as their ideal efficiency is higher than that of linear amplifiers. A class-G technique can be adopted to enhance the efficiency at output power backoff [13]. It is noted that the quadrature architecture

consumes less overhead power than polar architectures owing to the lack of a wideband phase modulator and synchronization circuitry. As with other SCPAs, it is worth noting that the Q-SCPA achieves high linearity owing to the ability to precisely define capacitance ratios in CMOS. Similarly, the Q-SCPA eliminates the need for auxiliary, high-bandwidth analog/mixed-signal circuitry (e.g., supply modulators and phase modulators) and can be scaled to higher resolutions as required by the communication standard.

In this paper we present a class-G Q-SCPA for non-constant envelope amplification. This paper is organized as follows. In section II, theoretical operation of the Q-SCPA is discussed. Design details of the presented Q-SCPA are provided in section III, followed by measurement results in Section IV. Finally, conclusions are presented in Section V.

II. Theory of Operation

A. Operation of Conventional SCPA

Switched-capacitor circuits are ubiquitous in CMOS owing to their fast low-loss switches and precisely-controlled capacitance ratios. The SCPA is a class-D PA with a precisely controlled capacitive divider at its output. The divider precisely controls the voltage level at the output of the SCPA using charge division on an array of capacitors; hence, it provides a direct linear summation of RF signals. Moreover, the load impedance of SCPA is code-independent, i.e., it is constant as the input digital code causes the output amplitude to vary.

As shown in Fig. 2, an SCPA consists of an array of capacitors whose top plates are shared and whose bottom plates are connected to an inverter that can be switched between the supply voltage (V_{DD}) and ground (V_{GND}). Though shown as a single inductor, in practice, L is the excess reactive impedance of the impedance matching network and R_{opt} represents the optimum termination resistance [14]. A decoder can selectively enable or disable any of the inverters. When enabled, switching is allowed to occur, while when disabled the bottom plate of the capacitor is held at ground. The output amplitude can thus be

modulated by controlling the number of the capacitors that are switched each cycle. When all capacitors are switched, a peak voltage is output, while switching fewer capacitors proportionally reduces the output voltage. An inductor is connected in series with the top plate to filter the square switching waveforms at the SCPAs input. This inductor forms a series resonant circuit with the output resistor; hence it acts as a bandpass filter for the fundamental operation frequency. The inductor and output resistor may be formed by passive components, or they can comprise a bandpass matching network that transforms the impedance of an antenna to an equivalent small resistance in series with a positive reactance. The output amplitude, V_{out}, is given by the following expression:

$$V_{out} = \frac{2}{\pi}\left(\frac{n}{N}\right)V_{DD} \tag{3}$$

where N is the total number of unit capacitors in the array and n is the number of capacitors that are being switched. The output power, P_{out}, and input power, P_{SC}, are given by the following expressions:

$$P_{out} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2 \frac{V_{DD}^2}{R_{opt}} \tag{4}$$

$$P_{SC} = C_{IN}V_{DD}^2 f \tag{5}$$

where f is the carrier frequency and C_{IN} is the input capacitance that varies with the selected code and the value of a unit capacitor C, *as follows*:

$$C_{IN} = \frac{n(N-n)}{N^2}C \tag{6}$$

The efficiency of the SCPA can be found as the ratio of the output power to the total power:

$$\eta_{SCPA} = \frac{P_{out}}{P_{out} + P_{SC}} = \frac{4n^2}{4n^2 + \frac{\pi n(N-n)}{Q_{nw}}} \tag{7}$$

where Q_{nw} is the network quality factor for the series resonant circuit:

$$Q_{nw} = \frac{2\pi fL}{R_{opt}} = \frac{1}{2\pi fCR_{opt}} \tag{8}$$

The design of an SCPA commences by choosing a desired P_{out}, and an acceptable value of Q_{nw}. Q_{nw} is limited by the quality factor of the available passive components and is typically dominated by the inductor in CMOS processes. Practical values of the quality factor of on-chip inductors are < 20. Matching network efficiency for a two element, lowpass downward transformation can be approximated by:

$$\eta_{Match} = \frac{1}{1+\frac{Q_{nw}}{Q_{Inductor}}} \quad (9)$$

Thus to maintain a network efficiency of greater than 75%, Q_{nw} values must be less than 5 [28]. Further details of the SCPA design and its theory of operation can be found in Yoo, et. al. [13], [14].

B. Operation of the Q-SCPA

An example schematic of a Q-SCPA is shown in Fig. 3. Design of a Q-SCPA commences from the same point as the polar SCPA to find the value of the total array capacitance. The array is subdivided such that half of the array capacitance is placed in the individual I/Q paths. The sub-arrays are further divided into unit capacitors with individual driver chains that can be either switched between V_{DD} and V_{GND}, or held at V_{GND}. A quadrature clock is generated that switches the sub-arrays such that the *I*-array rising edge leads the *Q*-array rising edge by 90°. In previous quadrature transmitter designs the clock was operated with a 25% duty-cycle to limit interactions between the individual *I*/*Q* components [23], [25]. Here it is noted that as long as the *I*-array code settles before the switching of the *Q*-array clock, there is no interaction between the *I*/*Q* components; this does set practical upper limits on the operation frequency of the Q-SCPA with 50% duty-cycle. Operation will now be described in detail.

As was previously mentioned, the input pulse waves for the *I* and *Q* capacitor sub-arrays are 90° out of phase. The output signal *s(t)* is the direct summation of *I(t)* and *Q(t)* waveforms:

$$s(t) = I(t)p(t) + Q(t)p(t+\frac{T}{4}) \quad (10)$$

where T is the carrier period; *p(t)* and *p(t+T/4)* represent the input 50% duty-cycle square waveforms as shown in Fig. 3(b). The *I(t)* and *Q(t)* signals are given by the following:

$$I(t) = A(t) \cdot cos\,\phi(t) \tag{11}$$

$$Q(t) = A(t) \cdot sin\,\phi(t). \tag{12}$$

where *A(t)* and $\phi(t)$ are the amplitude and phase of the modulated signal, respectively.

By substituting (11) and (12) into (10), performing the Fourier expansion and keeping only the terms at the desired carrier frequency, the following expression results:

$$s(t) = \mathrm{A(t)}\cos\phi(t)\frac{4}{\pi}\cos(\omega t) + A(t)\sin\phi(t)\frac{4}{\pi}\sin(-\omega t) = A'(t)\cos(\omega t + \phi(t)) \tag{13}$$

where A′(t)=4/π×A(t). The factor of 4/π is due to the fundamental component of the Fourier expansion of a square pulse train.

It can be seen that the amplitudes of *I(t)* and *Q(t)* are proportional to the number of capacitors switching in *I* (cos) and *Q* (sin) modes, respectively. Hence, weighting the *I*/*Q* sub-arrays properly, the output amplitude and phase can be controlled precisely. An example of the operation of the proposed Q-SCPA is shown in Fig. 4. In this figure both *I* and *Q* operate with 3b of total capacitance (e.g., 8 unit capacitors). In Fig. 4(a) an output in quadrant II of the complex plane is achieved with an inverted *I* clock signal and a non-inverted *Q* clock signal; precise phase and amplitude are controlled by selecting the number of capacitors that are on (e.g., switched), relative to the number held at ground. Examples for operation in quadrants I, III and IV are shown in Fig. 4(b), (c) and (d), respectively.

C. Q-SCPA Efficiency

The output power of the individual I or Q array in Q-SCPA can be found by increasing the total number of capacitors, *N*, in (4) by a factor of 2, assuming the *I* sub-array is off when the Q sub-array is switching (and vice-versa) and summing the power contribution from the I and Q sub-arrays [26]:

$$P_{out,QSCPA} = \frac{2}{\pi^2}\left(\frac{n}{\sqrt{2}N}\right)^2 \frac{V_{DD}^2}{R_{opt}} \tag{14}$$

The input power for the individual I and Q array can be found by assuming that the capacitors being switched (nC/N) are in series with the parallel combination of the capacitors not being switched (C(N-n)/N) and the capacitance from the other array (C). This gives the following input capacitance:

$$C_{IN} = \frac{n(2N-n)}{2N^2} C \tag{15}$$

Making a similar substitution of (15) into (5):

$$P_{SC,QSCPA} = \frac{n(2N-n)}{2N^2} C V_{DD}^2 f \tag{16}$$

The ideal drain efficiency of the Q-SCPA can be found as the ratio of the Q-SCPA output power to the total power:

$$\eta_{QSCPA} = \frac{P_{out,QSCPA}}{P_{out,QSCPA} + 2P_{SC,QSCPA}} = \frac{4n^2}{4n^2 + \frac{\pi n(2N-n)}{Q_{nw}}} \tag{17}$$

The total drain efficiency of the PA is the product of (9) and (16):

$$\eta_{Total} = \eta_{SCPA} \cdot \eta_{Match} \tag{18}$$

This is the total drain efficiency and does not account for input power due to the overhead (e.g., clock distribution, decoder logic, pad drivers, etc.) or losses due to finite switch resistance. This accounts for the discrepancy between the measured *power added efficiency* and the total drain efficiency calculation. It should be noted that the power associated with the It should be noted that the efficiency profile of (17) is identical to that of (9); however, the Q-SCPA peak efficiency will always be lower since its peak output power is 3-dB lower than the original SCPA. A plot comparing the ideal PAE of the conventional SCPA to the Q-SCPA for several different values of Q_{nw} is plotted in Fig. 5. It is noted that η_{QSCPA} is proportional to Q_{nw}, while η_{Match} is inversely proportional to Q_{nw}; this implies that an optimal Q_{nw} exists. η_{Total} is plotted versus Q_{nw} in Fig. 6, for several different values of code word, n in a 7 bit Q-SCPA (i.e., $N = 128$). This plot assumes that the quality factor of the capacitor is significantly larger than the inductor, and that $Q_{Inductor} = 10$. It can be seen that the optimal Q_{nw} is between 2 (n=128, peak output power) and 4 (n=32, 6dB backoff).

Additional losses in clocking and driving can be accounted for with estimates of the total gate capacitance being driven [14]. As has been noted, though there is a penalty for combining the signals after the PA, there is no requirement for precision synchronization or wideband phase-/amplitude-modulator circuitry, all of which require significant power from the supply.

III. Circuit Details

A. Top Level of the 7-bit Q-SCPA

A single-ended block diagram of the proposed Q-SCPA is shown in Fig. 7 [26]. Note that the fabricated circuit is differential. A Cartesian representation of a non-constant envelope signal is separated into its constituent in-phase, *I*, and quadrature, *Q*, vectors. The digitized *I*/*Q* vectors, $B_{I,Q}$, are represented as signed digital code words; These vectors are input to a digital pattern generator that separates the bit pattern and outputs the bits to their proper digital inputs. The on-chip decoder is a binary-to-thermometer decoder for the MSBs, while the LSBs are simply buffered to match the decoder delay. An RF frequency equal to twice the desired output frequency is received on chip via an LVDS clock receiver and is then converted to a quadrature clock by a quadrature ÷2 circuit. The MSB from the decoder is the sign bit and is input to an XOR along with the output of the ÷2 circuit. Hence, a quadrature output that can be inverted depending on the value of the sign bit is realized.

The remaining LSBs represent the amplitude weighting of the constituent *I* and *Q* signals. Each capacitor sub-array comprises a total of 6 bits, chosen primarily to reduce the amount of quantization noise at the output of the Q-SCPA, while meeting signal fidelity requirements (e.g., EVM, ACLR, etc.). This resolution also allows for additional bits should digital predistortion (DPD) be required. The capacitor sub-arrays are sub-divided into a partial unary and binary array as a compromise between size/complexity and linearity. The four MSBs are unary-weighted (C_U=200fF) and controlled by a binary-to-thermometer decoder whereas the two LSBs are binary-weighted (C_1=100fF and C_0=50fF) for fine output resolution. An extra bit is achieved by operating as a class-G circuit, with two binary weighted power supply voltages; hence, in the fabricated circuit, 7 total bits of amplitude resolution are realized. The capacitor sizes were limited by the smallest dimensions achievable for MiM capacitors in the chosen technology.

The capacitor array is designed using MiM capacitors with a common top-plate, while the bottom plates are connected to class-G switches (more detail on the class-G switch will be provided in the

following section). The top plates are connected in series with a low-pass matching network that transforms the antenna impedance of 50 Ω to the optimum termination impedance. The matching circuit is comprised of a series inductor, L_{ser}, and a shunt capacitor, C_{sh}, forming a bandpass series-resonant circuit at the design frequency. Because the total capacitance remains unchanged from the perspective of the matching network, it can be sized to be series resonant with the total capacitance in the array. The matching network also acts to filter the undesired harmonic content associated with switching waveforms at the input of the circuit.

The inductor, L_{ser} = 1.0 nH, is realized as custom wound, fully differential transformer, as seen in Fig. 8(a). The routing of the inductor allows both sides of the differential Q-SCPA to be matched to the antenna impedance while providing ease of routing. The simulated inductance and resistance of the custom cell are plotted in Fig 8(b). The capacitor, C_{sh} = 4.8pF is a MiM capacitor, similar to those used in the Q-SCPA capacitor arrays. The impedance transformation circuit uses a loaded quality factor, $Q_{nw} \approx 3$, leading to a circuit with approximately 600 MHz 3-dB bandwidth centered at 2 GHz. Higher quality factors can be used if off-chip impedance transformation is used owing to the higher quality factors possible with use of off-chip components.

B. Unit Class-G SCPA

The schematic of the dual supply class-G driver [29], [13] is shown in Fig. 9. Low voltage is a primary reason for poor efficiency in CMOS power amplifiers; this is because the output resistance is proportional to the square of the supply voltage; hence a reduction in supply voltage by a factor of two reduces the optimum termination impedance by a factor of four. This leads to larger impedance transformations from the antenna, corresponding to higher losses in the matching network, as well as a voltage division at the output of the switching transistor. The nominal supply voltage for CMOS devices is V_{DD} = 1.2 V in the chosen 65nm process technology. In order to increase the output power and to reduce the losses from

impedance transformation, it is desirable to operate with higher voltage supplies. This is implemented by cascoding the transistors in a standard CMOS inverter that acts as the switch between the high supply voltage and ground in the Q-SCPA. Using this topology, the supply voltage of the cascoded driver is increased to twice V_{DD}, which is labeled as V_{DD2} in Fig. 9. It has been shown that efficiency in power backoff can be improved by reducing the supply voltage for envelope signals that are small enough [13], [30], [31]. In a switched capacitor circuit, switching supplies results in no glitch, as the transition can be controlled to only occur when the switch is already open (e.g., disconnected from the load) [13], [32]. Therefore, a second switching path is added with a supply voltage of V_{DD}. It is critical to match the resistances of both the pull-up and the pull-down paths. This will mitigate code dependent non-linearity [14]. The class-G topology increases the peak output power, improves the efficiency at power backoff, and adds an extra binary bit of resolution since $V_{DD2} = 2V_{DD}$.

C. Logic and Switch Drivers

The schematic for the enabling logic and drivers that precede the switch is shown in Fig. 10. The enabling logic for each switch path is located adjacent to the switch and takes its input from the decoder. Colocation of the logic and driving chains allows the parasitic routing capacitance to be minimized and for easier timing synchronization of the switching signals. Four separate controls (A, B, C and D) are required to control the class-G switch. The PMOS transistors operate between supply rails V_{DD} and V_{DD2}; hence, a level shifter is used to change the logic levels [33]. Inverters after the level shifters are placed in isolation wells to allow operation from these different supply rails. Care is taken to minimize the delay mismatch from output to input in all four paths, as this minimizes the potential for crowbar current to flow between the supply rails if the PMOS and NMOS paths were on simultaneously. Non-overlapping clocks can be used to further minimize crowbar current, at the expense of slightly lower output power and reduced

linearity. Effects of relative delay mismatch between different cells is mitigated using an input latch; all data bits are designed to arrive at the latch within its setup time.

IV. Experimental Results

An experimental prototype of the capacitively combined, class-G Q-SCPA is fabricated in a 65 nm RF LP CMOS process with 9 layers of metallization, including an ultra-thick top metal for high quality passive elements. The prototype occupies an area of 1.8mm×1.0mm including all bonding and probe pads; the chip area is heavily pad dominated due to required I/O. A chip microphotograph of the Q-SCPA is shown in Fig. 11. The circuit is comprised of a differential, quadrature 6-bit array of precision MIM capacitors, switches, drivers, selection logic, decoders and a fully integrated output matching network. The bottom plates of I+ and Q+ arrays are connected while I- and Q- arrays share the same bottom plates. All circuits operate from 1.2 V, with the exception of the cascoded switches that operate from 2.4 V.

A. Static Measurements

The PA operates at a center frequency of 2 GHz with a peak output power and efficiency of 20 dBm and 21%, respectively, as shown in Fig. 12. The -3 dB bandwidth of the PA is ≈400 MHz as determined by the loaded quality factor of the band-pass matching network. Note that the performance below 2 GHz is dominated by the rolloff of the balun in the measurement setup.

Shown in Fig. 13(a) is the P_{out} vs. the quadrature code input for the vector I=Q. This corresponds to a transition from the maximum in quadrant III to the maximum in quadrant I of the complex plane. The output amplitude reduces linearly as the code is changed, with minor distortion due to bonding inductance. A sign bit allows the quadrature oscillator signals to be inverted so that all quadrants of the complex plane are accessible. Asymmetry in the response owes to supply and ground bounce due to excess bondwire inductance in the PCB layout, owing to spacing requirements for the chip-on-board packaging utilized. This distortion can be reduced with better decoupling of the supply circuits on chip, or with low-

inductance packaging (e.g., Flip-chip) [13]. The efficiency is plotted as a function of output power for the *I=Q* vector in Fig. 13. Again, the asymmetry is due to supply and ground inductance and can be reduced similarly.

B. Dynamic Measurements

2D-DPD was performed to improve the linearity of the QSCPA [23], [24]. A 2D-DPD lookup table is constructed based on static measurements consisting of a 255×255 points of measurement in the *I* and *Q* dimensions, respectively. The input data is applied to the lookup table where the inverse of the distortion characteristic is applied to the codes that are input to the PA. This accounts for all of the aforementioned asymmetry in the output response. To verify the quadrature SCPAs ability to amplify complex, wideband modulated signals, a 10 MHz, 64 QAM LTE signal is applied to the power amplifier. The ACLR performance is plotted in Fig. 14 and shows less than -30 dBc when outputting 14.5 dBm at 12.2% average efficiency. This result is obtained after a 2D digital pre-distortion procedure that is only necessary due to the aforementioned excessive supply and ground bondwire inductance, as was verified with simulations of the Q-SCPA with and without bondwire inductance. The Q-SCPA, like all class-D PAs is more susceptible to bondwire inductance, as it is critical to minimize the ground *and supply* inductance. This can be mitigated if using a flip-chip package [13], and by using a single external supply with on-chip DC-DC converters to create additional supply voltage levels. The signal constellation is plotted in Fig. 15, showing the measured EVM at this output power is 3.6%-rms.

Digital PAs such as the SCPA and Q-SCPA are quantized systems and hence their out-of-band (OOB) noise is dominated by quantization. The OOB noise for the 7-bit QSCPA when transmitting a 10 MHz, 64 QAM LTE signal is plotted in Fig. 16. The OOB noise at +80, +85, +95, +190 MHz and the ISM band is -115.4, -115.3, -115.8, -108.8 and -112.4 dBm/Hz, respectively. Though these exceed the desired specification of -125 dBm/Hz, with two extra bits of resolution the specification would be met. It is noted

that the primary reason that additional resolution was not accommodated in this design was a limitation on I/O pads in the available area. In an SOC implementation, external pad drivers are unnecessary, also a serialized input can be used in future stand-alone applications. Calculations for the chosen process show that the maximum resolution that can be achieved in this process at this frequency is 16b (jitter) and 18b (mismatch). As the presented design was pad limited, increasing resolution in a fully integrated transmitter would not be problematic. It should also be noted that the poor performance at 190 MHz was dictated by the sampling rate of the pattern generation instrument and could be increased to move the spurs further OOB. The functionality of the QSCPA is validated through both the static and vector measurements. The advantages of the QSCPA are evident in that no phase modulator or timing synchronization circuitry was necessary.

V. Conclusions

A quadrature SCPA that can output any phase and amplitude on the complex plane based on digitally coded quadrature inputs is demonstrated in 65nm CMOS. As with all SCPAs, this PA leverages CMOS strengths of low-loss switches and precision capacitor ratios to simultaneously achieve good efficiency and linearity. The Q-SCPA, however, leverages the advantages of digital PAs while not requiring the wideband modulator of typical DPAs. Furthermore, no complex synchronization circuits are required, unlike what is required in Digital polar PAs. A prototype fabricated in a 65 nm CMOS process achieves a peak P_{out} and PAE of 20.5 dBm and 20 %, respectively. The performance of the Q-SCPA in a transmitter is validated using a 10MHz, 64-QAM LTE signal. After a 2D DPD, the ACLR is below the required -30 dBc limit and the measured EVM is < 4%-rms, while achieving an average P_{out} and PAE of 14.5 dBm and 12.2%, respectively. A comparison to similar completely integrated digital transmitter front-ends is in Table I. Though the peak efficiency and output power are lower than the polar/EER counterparts, no wideband phase-modulator or supply modulator is required, nor are synchronization of the phase and

amplitude circuits. Furthermore, with higher quality external passives, sharing of the I/Q paths [25], and with complete integration (e.g., no pad drivers) the total system efficiency can be similar to polar variants.

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LIST OF FIGURE AND TABLE CAPTIONS

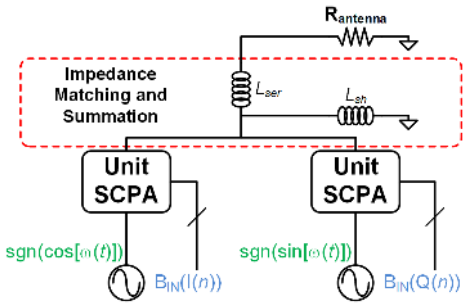


Fig. 1. Block Diagram of an SCPA based quadrature power amplifier.

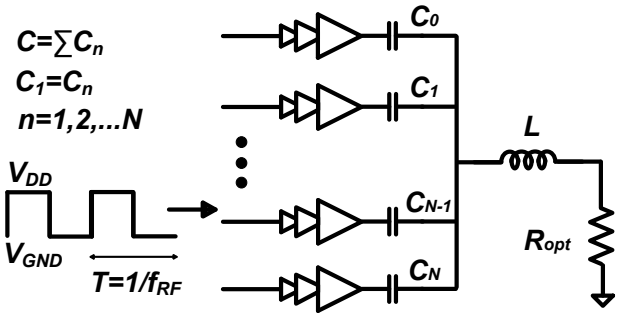


Fig. 2. Schematic of an SCPA.

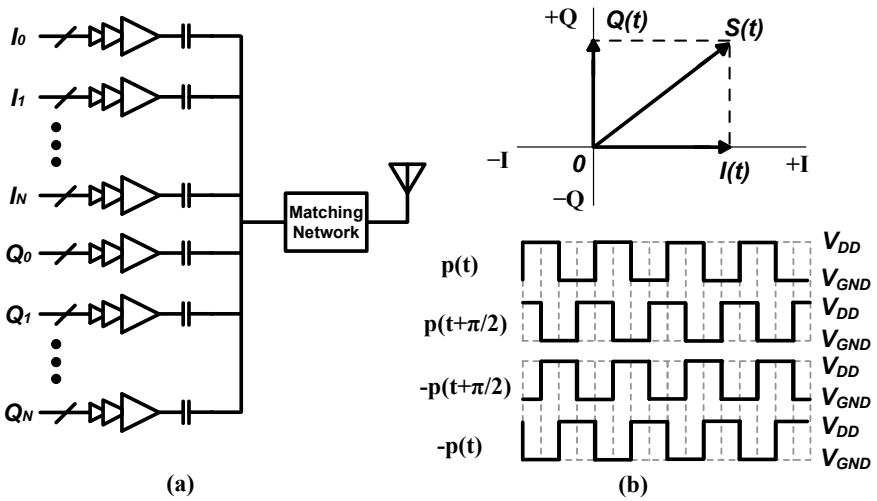


Fig. 3. (a) Schematic diagram of a Q-SCPA; (b) waveforms of I/Q vectors.

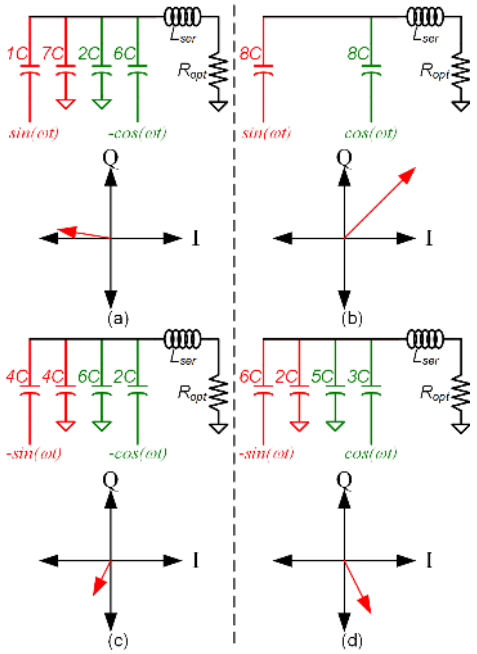


Fig. 4. Schematics of capacitively combined quadrature SCPAs outputting (a) -6+j1, (b) 8+j8, (c) -2-j4, and (d) 3-j6.

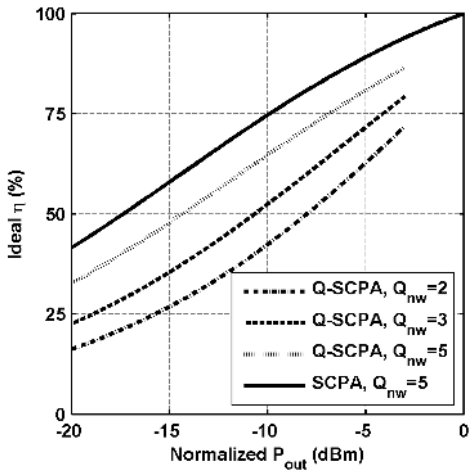


Fig. 5. Comparison of ideal drain efficiency, η, versus P_{out} for a conventional SCPA and several Q-SCPAs.

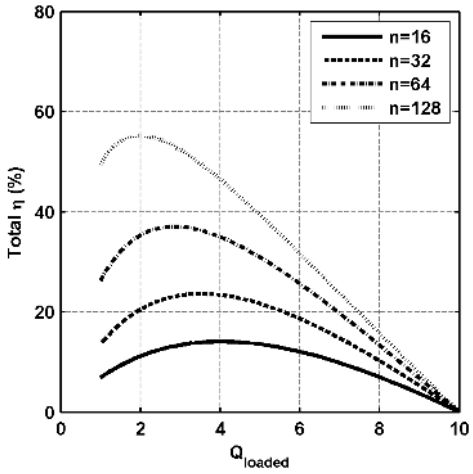


Fig. 6. Comparison of the total drain efficiency versus Q_{nw} for several code words in a Q-SCPA.

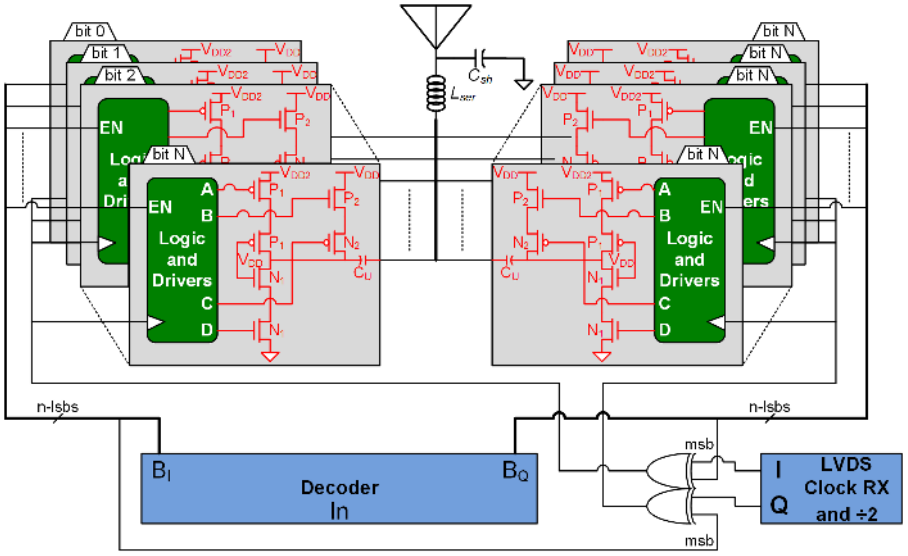
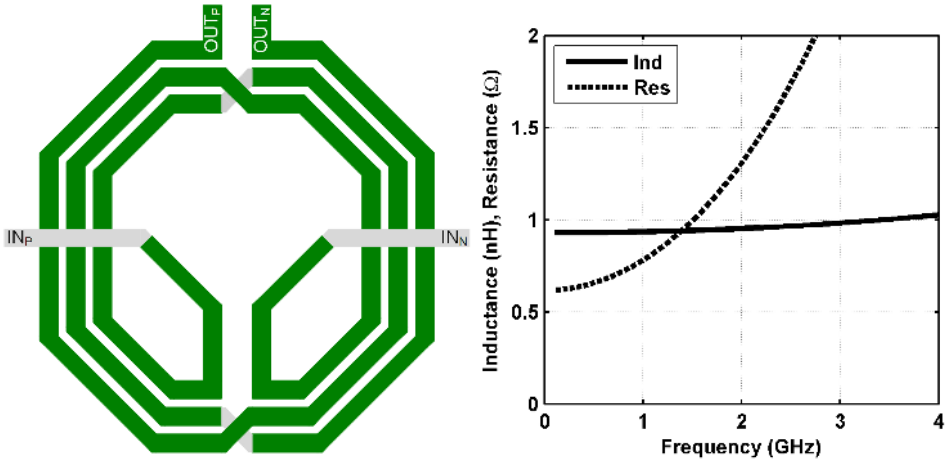


Fig. 7. Block diagram of the proposed quadrature SCPA. Note that the actual implementation is differential and that the switches are cascoded class-G switches (See Fig. 9). The Unit capacitance size is 200fF.



(a) (b)

Fig. 8. (a) Custom differential inductor L_{ser}; (b) simulated Inductance and resistance vs. frequency.

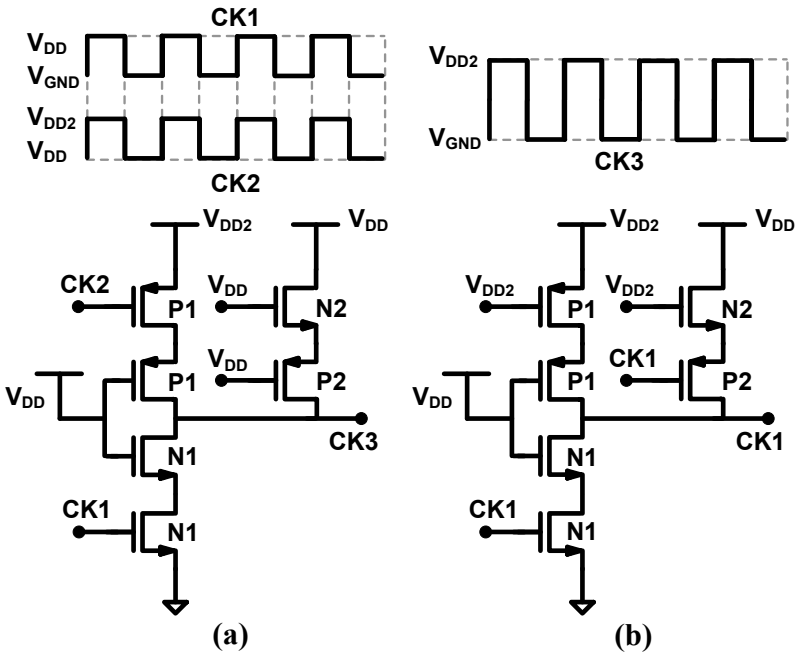


Fig. 9. Schematic of unit class-G driver with active supply of (a) V_{DD2} (b) V_{DD}. All transistors are minimum length (e.g., 65 nm), with the following widths (in μm): P_1=P_2= 87.84, N_1=28.8, N_2=38.88.

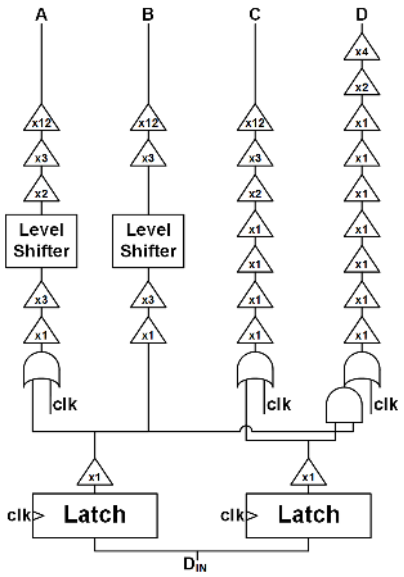


Fig. 10. Q-SCPA Class-G Logic Decoder. Note that the unit size for an NMOS transistor is 550nm×60nm, while a PMOS is 1320nm×60nm

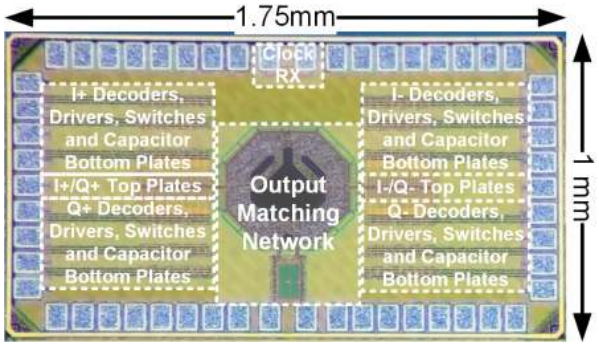


Fig. 11. Chip microphotograph of the 65 nm experimental prototype transformer combined SCPA.

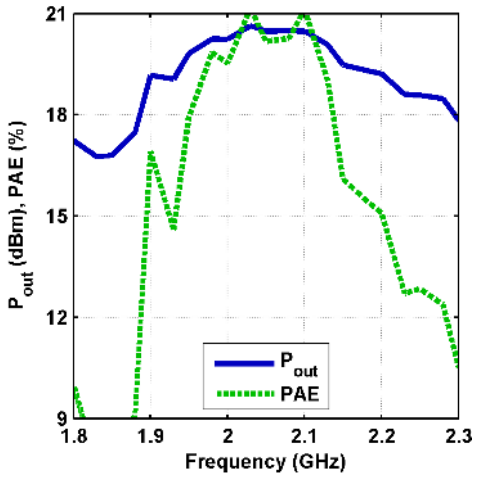
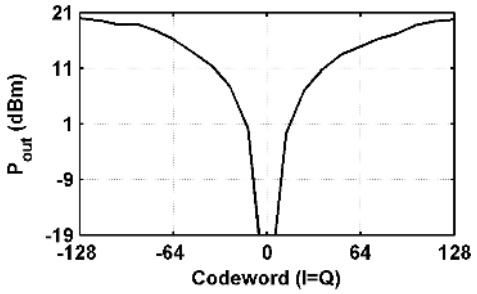
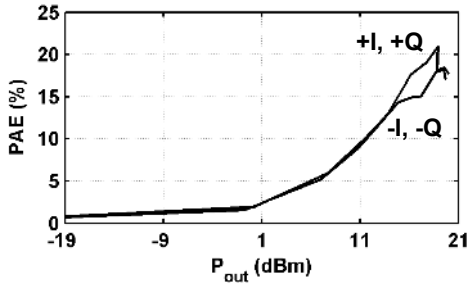


Fig. 12. Measured output power and PAE vs. frequency.



(a)



(b)

Fig. 13. (a) Measured output power vs codeword (b) Measured PAE vs. output power.

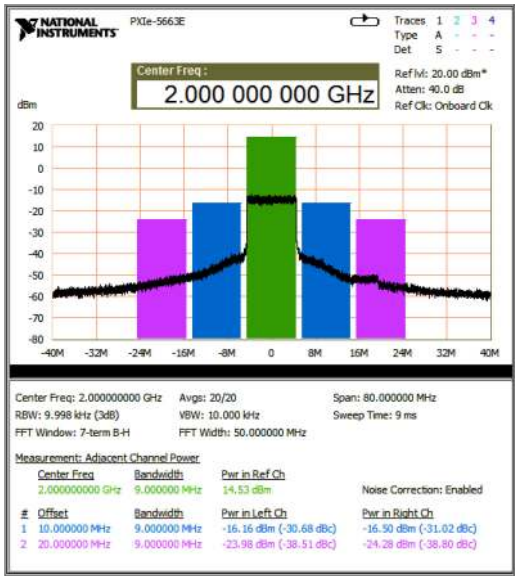


Fig. 14. Measured ACLR for a 10 MHz, 64 QAM LTE signal.

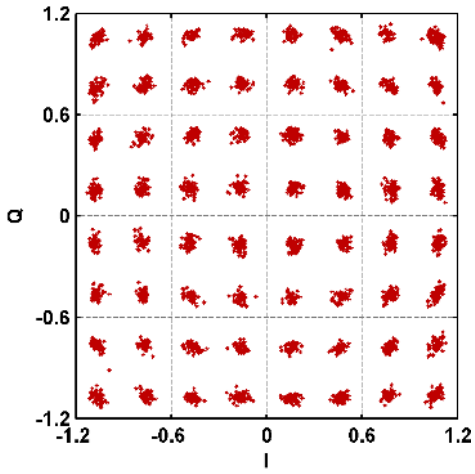


Fig. 15. Measured Signal Constellation for a 10 MHz, 64 QAM LTE signal.

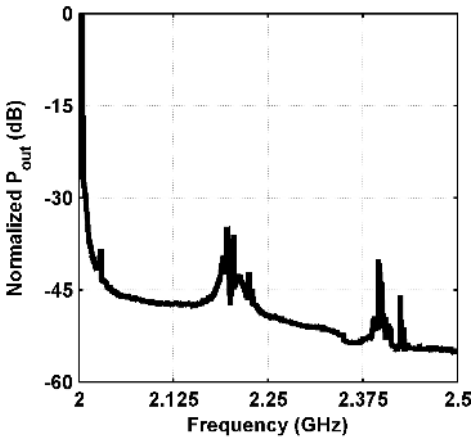


Fig. 16. Measured OOB Spectrum for a 10 MHz, 64 QAM LTE signal.

Table I. Comparison to Prior Art

	This Work	[25]	[23]	[27]	[16]
Process technology	65 nm	28 nm	65 nm	65 nm	65 nm
Supply voltage (V)	1.2/2.4	1.1	1.3	1.25	1.2
Resolution (bit)	7-IQ	6-IQ	13-IQ	7-IQ	9-Polar
Carrier Frequency	2.0 GHz	800 MHz	2.4 GHz	800 MHz	2.2 GHz
Peak P_{out} (dBm)	20.5	13.9	22.8	7.87	23.3
PAE at peak P_{out}	20%	40.4%	42%	10.8%	38%
Modulation signal	LTE 10 MHz, 64-QAM	LTE 10 MHz, 16-QAM	Single carrier 22 MHz, 64-QAM	LTE 5 MHz	802.11g 20 MHz, 64-QAM
Average P_{out} (dBm)	14.5	6.97	15	0.26	16.8
Average PAE	12.2%	29.1%	NA	6.7%	21.8%
EVM	3.6%-rms	NA	3.98%-rms	NA	3.98%-rms
ACLR (dBc)	-30.7/-31.0	-32.4/-32.7	<-43	-31.8/-31.5	NA
Matching Network	LC Matching	No	Transformer	No	Transformer
w/ DPD	Yes	NA	Yes	NA	Yes