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A QUASI-STATIC TECHNIQUE FOR MOS *C–V* AND SURFACE STATE MEASUREMENTS

M. KUHN

Bell Telephone Laboratories, Inc.
Murray Hill, New Jersey, U.S.A.

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Abstract—A quasi-static technique is discussed for obtaining the 'low frequency' thermal equilibrium MOS capacitance–voltage characteristics. The method is based on a measurement of the MOS charging current in response to a linear voltage ramp, so that the charging current is directly proportional to the incremental MOS capacitance. With this technique, surface potential and the surface state density can be obtained relatively simply and over a large part of the energy gap on a single sample, while also providing a direct test for the presence of gross nonuniformities in MOS structures. This method has been used to determine the surface state distribution at the interface of a bias grown steam oxide and 10 Ω-cm *n*-type silicon, and the results are compared with composite measurements using the conductance technique for a similar interface. The sensitivity for surface state density measurements is estimated to be of the order of 10^{10} states per cm^2 eV near mid-gap for 10 Ω-cm silicon and improves with decreasing doping density. Some applications and limitations are also briefly discussed.

Résumé—On examine une technique quasi-statique pour obtenir l'équilibre thermique à basse fréquence des caractéristiques capacité-tension des MOS. La méthode est basée sur les mesures du courant de charge MOS en réponse à une rampe linéaire de tension de sortie de sorte à ce que le courant de charge est directement proportionnel à la capacité d'accroissement MOS. Avec cette technique, le potentiel de surface et la densité d'état de surface peuvent être facilement obtenus sur un même échantillon pour une grande partie de l'intervalle d'énergie tout en fournissant un test direct pour les présences d'irrégularités dans les structures MOS. Cette méthode a été employée pour déterminer la distribution de l'état de surface à l'interface d'un oxyde de vapeur développé pour la polarisation et du silicium de type n à 10Ω-cm et les résultats sont comparés aux mesures composées employant la mesure de conductance pour un interface similaire. La sensibilité des mesures de densités d'états est estimée être de l'ordre de 10^{10} états par cm^2 eV près de l'intervalle central pour le silicium 10Ω-cm et s'améliore en diminuant la densité de dope. On discute aussi les applications et les limites.

Zusammenfassung—Eine quasi-statische Technik zur Bestimmung der Kapazitäts-Spannungscharakteristik von MOS-Strukturen im thermischen Gleichgewicht bei niedrigen Frequenzen wird diskutiert. Die Methode beruht auf der Messung des Ladestromes bei linearem Spannungsanstieg, so dass dieser Strom direkt der Kapazitätszunahme proportional ist. Hiermit gewinnt man das Oberflächenpotential und die Oberflächentermdichte auf relativ einfache Weise für einen grossen Teil der Bandlücke. Das Verfahren dient der Auswertung sowohl einzelner Proben als auch zum Testen der Gleichmässigkeit der MOS-Strukturen. Die Verteilung der Oberflächenzustände an der Grenzfläche von *n*-Typ-Silizium mit einem spez. Widerstand von 10 Ω cm und im Wasserdampf gewachsenen Oxidschichten wurde bestimmt. Die Ergebnisse wurden verglichen mit anderen Messungen an ähnlichen Grenzflächen, die die Leitfähigkeit ausnützen. Die Empfindlichkeit der Methode für die Bestimmung der Oberflächenzustandsdichte nahe der Bandmitte wird zu etwa $10^{10}/cm^2$ eV abgeschätzt für Silizium mit einem spez. Widerstand von 10 Ω cm; sie nimmt zu mit abnehmender Dotierung. Einige Anwendungen und Grenzen der Methode werden kurz diskutiert.

INTRODUCTION

A LARGE part of the information on metal–insulator–semiconductor structures was obtained from detailed studies of the electrical properties of the MOS capacitor and the field effect transistor, and several techniques have been developed for the extraction of surface state properties from such measurements. In this paper we shall discuss a

quasi-static technique[1-3] for the measurement of the low frequency incremental MOS capacitance–voltage characteristics under thermal equilibrium conditions and show that this technique can be used to obtain the semiconductor surface potential and the energy distribution of surface states over a large fraction of the band gap with a single measurement on a single sample, including a test for the presence of gross nonuniformities.

The high frequency capacitance technique developed by TERMAN[4] yields surface state charge by comparison of a high frequency C–V curve (0.1–1.0 MHz) with an ideal C–V curve. The limitations of this technique have been discussed in detail by ZAININGER and WARFIELD.[5] The most serious of these is that a graphical differentiation of the analyzed data is required to determine surface state distribution, in the energy gap, and that both the surface state density and the surface potential must be obtained with the help of an ideal C–V curve. Furthermore, the region of the band gap accessible with this technique is limited by the condition that the surface state charging time is much longer than the period of the test frequency.

The a.c. conductance technique[6] yields the most detailed and accurate information about surface states, as surface state density and capture cross section are obtained from measurements of the MOS admittance as a function of bias and frequency. However, a large number of measurements are required to achieve such detailed results, and only that portion of the energy gap between mid-gap and the Fermi level can be conveniently probed with this technique.

On the other hand, surface state density near the majority carrier band edge may be estimated with the GRAY–BROWN technique,[7,8] in which the change in flat band voltage of an MOS capacitor is measured as a function of temperature. Again, the range of band gap accessible is very small, being determined by the variation of the Fermi level within the temperature limits dictated by oxide instability at high temperature and impurity deionization at low temperatures.

From this brief discussion it becomes clear that a simple method of determining surface state density over an extended range of the energy gap would be desirable, as this would provide a common bridge between the various methods outlined above, and it could expedite surface state measurements considerably. Very low frequency MOS capacitance measurements in which thermal equilibrium is maintained, as first suggested by BERGLUND,[9] can yield surface state density over such an extended energy range. From a theoretical treatment of the low frequency response of MOS devices, HOFSTEIN[10] showed that inversion layer response times of the order of one second are expected, and BERGLUND[9] has observed low frequency C–V dispersion down to 5 Hz using a lock-in technique. However, conventional sinusoidal phase sensitive measurement techniques become difficult to perform below this frequency range[11] and therefore this method has not been widely used. Such 'very low' frequency C–V measurements are most directly and easily obtained from the quasi-static response of an MOS capacitor to a linear voltage ramp.[1-3] This method and some of its applications will be discussed below.

The details of the measurement technique are described in the following section, and some typical low frequency C–V curves on both n- and p-type silicon are given. In the next section the details of the ideal quasi-static response are discussed and their analysis to determine surface potential and surface state distribution is described. The limitation on the sweep rate and its relation to the expected deviation from thermal equilibrium are discussed in the final section, and the sensitivity of the method for surface state analysis is estimated.

Measurement technique

The quasi-static technique requires the measurement of the MOS displacement current in response to a linear voltage ramp. The elements of a circuit for performing such measurements are shown in Fig. 1. This circuit is essentially an analog differentiator incorporating the MOS device as the capacitive element. The amplifier A is a high gain, high impedance operational amplifier which maintains point N of the circuit at ground potential. When a voltage $V(t)$ is now applied to the circuit, the output voltage $V_0(t)$ is given by

$$V_0(t) = -RC(t)\frac{\mathrm{d}V(t)}{\mathrm{d}t}. \qquad (1)$$

Therefore, when $V(t)$ is a linear ramp of the form $V(t) = V_1 \pm \alpha t$, the output voltage $V_0(t)$ is

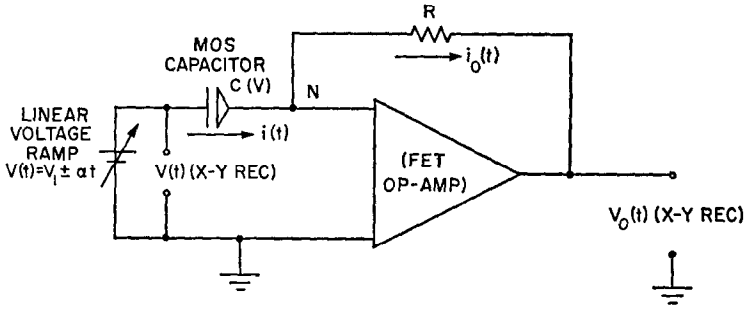

FIG. 1. Basic circuit required for quasi-static MOS C–V measurements.

directly proportional to the differential capacitance,

$$V_0(t) = \mp \alpha RC(t). \tag{2}$$

Therefore, a simultaneous display of $V_0(t)$ and $V(t)$ on an X–Y recorder will yield a directly scaled $C(V)$ vs. V curve with time as an independent parameter.

Such a circuit may be conveniently realized using an electrometer such as the Keithley model 602 in the 'fast' mode, as an operational amplifier and a simple operational amplifier integrator to obtain a linear ramp voltage with linearity better than 0.5 per cent. Typical voltage sweep rates are in the range from 5 to 500 mV per second depending on

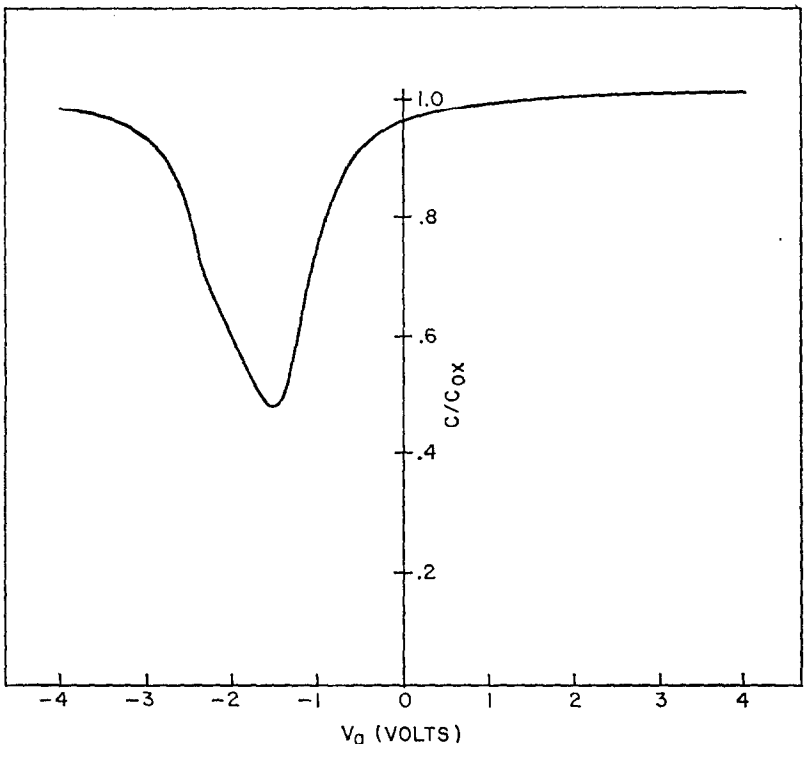

FIG. 2. MOS C–V curve obtained with the quasi-static technique for an n-type silicon MOS capacitor with the following characteristics: $Nd = 4.19 \times 10^{-14}$ cm^{-3}, field plate area $= 2.32 \times 10^{-2}$ cm^2, oxide: 800 Å thick, bias grown, steam oxide.

oxide capacitance and minority carrier lifetime; the resultant displacement current density is usually less than 10^{-8} A/cm^2. Such sweep rates usually yield C–V curves which are essentially independent of both the sweep direction and the sweep rate. The limitations on the sweep rate imposed by restriction to negligible deviation from thermal equilibrium will be discussed in a later section. Some typical examples of low frequency C–V curves obtained from quasi-static measurements are shown in Figs. 2 and 3, for 10 Ω-cm n-type, and 0.1 Ω-cm p-type silicon with bias grown steam oxides.

potential ψ_s, and the surface state density N_{ss} are defined in the usual fashion. In the light of the considerable earlier work on this structure, it is convenient to discuss the response of the MOS capacitor to a time varying voltage in terms of a simplified equivalent circuit first derived by LEHOVEC and SLOBODSKOY[12] and shown in Fig. 4b. Here C_{ox} represents the oxide capacitance, and the remaining network represents the semiconductor–insulator interface and the semiconductor surface. C_d, C_a, and C_i are the depletion, accumulation, and inversion layer capacitances respectively, and C_{ss}

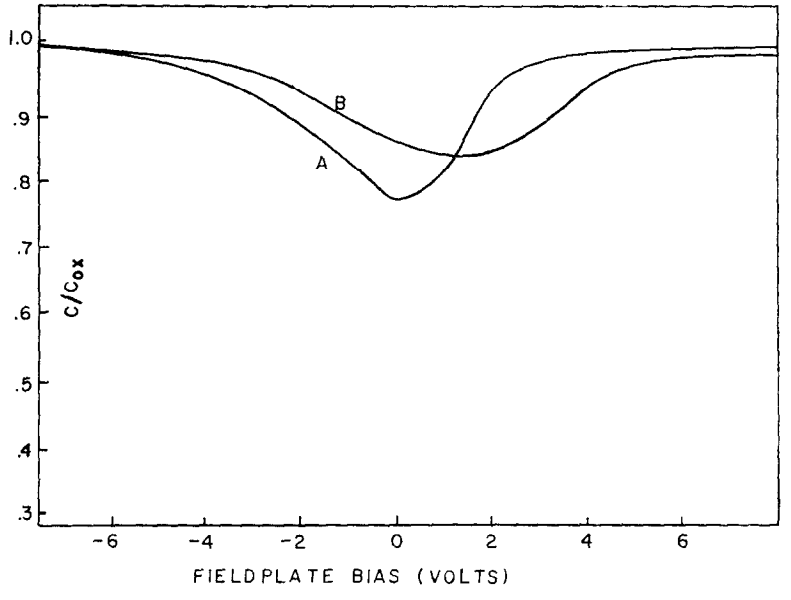

FIG. 3(a). Quasi-static C–V curves for Au–SiO_2–Si capacitor: Au dot: 10 mil dia. SiO_2: 600 Å. Si: 0.1 Ω-cm p-type epitaxial. (b). Quasi-static C–V curve for same capacitor but after avalanche charging of the SiO_2 to increase the surface-state density.

ANALYSIS

The surface potential and surface state distribution at the oxide-semiconductor interface may be determined from an analysis of the quasi-static C–V data. In this section we will discuss the necessary analysis to determine surface potential and surface state density using an n-type silicon MOS capacitor, as shown in Fig. 4, as an example.

The potential energy diagram for the MOS structure is shown in Fig. 4a, where the applied voltage V_a, the oxide voltage drop V_{ox}, the surface

is the surface state equivalent capacitance. R_c and R_v represent the capture and emission processes with which the surface states interact with electrons and holes at the semiconductor surface, and R_g represents the depletion layer generation–recombination mechanisms responsible for formation of the inversion layer. All of the elements of this equivalent circuit describing the semiconductor surface are nonlinear functions of the surface potential, and hence all are voltage dependent, thereby complicating an exact analysis. However,

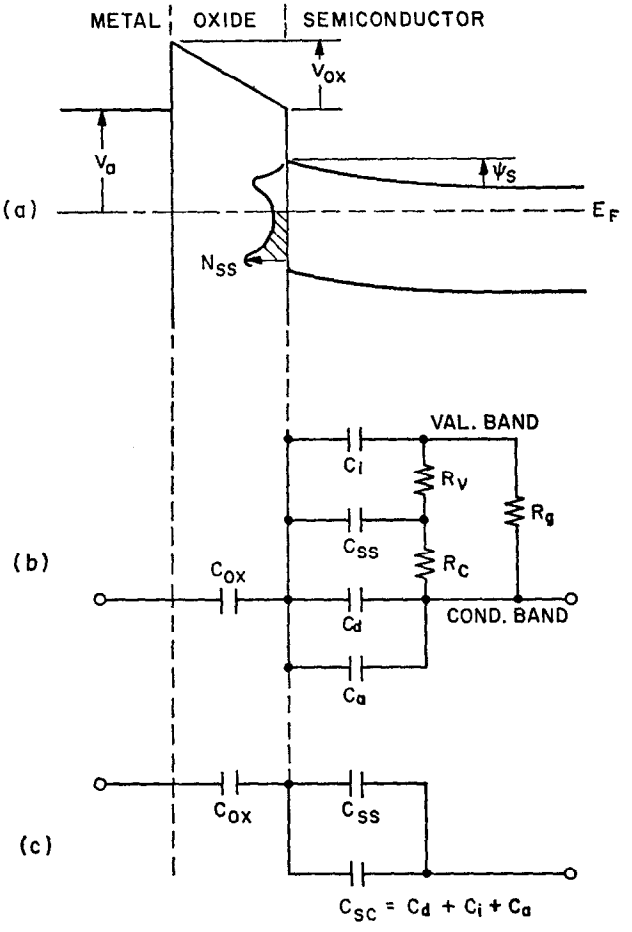

FIG. 4(a). Energy band diagram for the n-type MOS capacitor. (b). Equivalent circuit for the MOS capacitor. All of the components describing the semiconductor response are strongly dependent on the surface potential ψ_s. (c). Reduced equivalent circuit for the MOS capacitor under quasi-static conditions when thermal equilibrium is maintained.

this equivalent circuit may be used qualitatively to assess the relationship between surface state time constant and inversion layer formation time constant and to discuss the effects of maintaining thermal equilibrium with the quasi-static technique.

In the accumulation and depletion regimes, the minority carrier concentration at the surface is very low and, therefore, the surface states interact with the semiconductor surface primarily by capture and emission of electrons in the conduction band. In terms of the circuit model, this means that $R_v \gg R_c$, and the surface state time constant is given by $\tau_{ssc} \simeq C_{ss}R_c$. In inversion, however, the MOS response is more complex because it depends on two different rates: the inversion layer formation rate and the hole-capture rate from the valence band. The latter depends on the hole concentration at the surface, while the former determines the hole concentration at the surface. Minority carrier generation in the depletion region provides the holes for the inversion layer formation which proceeds with a time constant $\tau_i \simeq C_iR_g$ of the

order of one second in device quality silicon. If the quasi-static voltage sweep is sufficiently slow to maintain the inversion layer in thermal equilibrium, the thermal generation term effectively shorts the valence band to the conduction band. Then the surface state relaxation time constant is given by $\tau_{ssv} = C_{ss}R_v$. Both τ_{ssv} and τ_{ssc} have been experimentally measured on p- and n-type samples, respectively, using the conductance technique.[6] These measurements show that both τ_{ssc} and τ_{ssv} are exponentially dependent on surface potential, such that in depletion $\tau_{ssc} \ll \tau_{ssv}$, and in inversion $\tau_{ssv} \ll \tau_{ssc}$, and that near mid-gap both are of the order of 10^{-2} sec. Therefore, in the quasi-static method the longest surface state time constant will be of the order of 10^{-2} sec at room temperature; this is very much shorter than the time constant for inversion layer formation. Therefore, the sweep rate limiting factor in the quasi static method is the thermal generation rate, and if the sweep rate is low enough to maintain the inversion layer in thermal equilibrium, the surface states must then also be in thermal equilibrium. In effect, the thermal generation term allows both the minority carriers and those surface states near the minority carrier band edge to respond to the applied signal, and thus contribute to the incremental capacitance, thereby increasing the energy range over which surface states may be studied. If the thermal generation rate is large compared to the applied sweep rate, R_v, R_c, and R_g may be replaced by short circuits, and the equivalent circuit in Fig. 4b reduces to the much simpler capacitance network of Fig. 4c, where C_{sc} is the ideal incremental low frequency semiconductor surface capacitance including the inversion layer response.

Now, from Fig. 4c, the measured MOS capacitance $C(V_a)$ is

$$\frac{1}{C(V_a)} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}+C_{ss}}. \tag{3}$$

Equation (3) yields the following expression for the surface state density:

$$N_{ss}(\psi_s) = \frac{C_{ss}(\psi_s)}{q} = \frac{1}{q}\left[\frac{C(V_a)}{1-\dfrac{C(V_a)}{C_{ox}}} - C_{sc}(\psi_s)\right], \tag{4}$$

which is equivalent to BERGLUND's[9] expression but is written here in terms of the measured and ideal capacitances per unit area, rather than in terms of voltage differentials.

In order to use this equation for surface state density determination, it is first necessary to obtain the relationship between the surface potential ψ_s and the applied voltage V_a. BERGLUND[9] has shown that surface potential may be determined within an additive constant directly from the measured thermal equilibrium C–V curve. By integrating the measured $C(V)$ curve from a voltage, $V_{acc.}$, corresponding to strong accumulation toward inversion, the surface potential at any applied voltage V_a is given by [6]

$$\psi_s(V_a) = \int_{V_{acc.}}^{V_a}\left[1-\frac{C(V_a)}{C_{ox}}\right]dV_a + \Delta. \tag{5}$$

The additive constant Δ may be calculated or determined by comparison with ideal curves as will be discussed below.

In addition to providing a reliable measure of surface potential, Berglund has also shown that this method provides a test for the presence of gross nonuniformities in either the oxide or the semiconductor beneath the MOS field plate. The presence of such gross nonuniformities, if unknown would destroy the validity of any results from a surface state analysis based on one-dimensional assumptions. In essence, if the magnitude of the definite integral in (5) evaluated from strong accumulation to strong inversion is larger than the expected surface potential variation for the particular doping density of the semiconductor, gross nonuniformities are present. Therefore, a sample may be tested for the presence of gross nonuniformities before commencing a surface state analysis with the same data that is used in the surface state analysis itself.

Finally, ideal C–V characteristics are needed to carry out the surface state analysis. They are needed primarily to evaluate $C_{sc}(\psi_s)$ in (4), but they are also used in the test for gross nonuniformities and in the determination of the additive constant Δ in (5). A convenient computer program produced by IRVIN[13] was used in these experiments to calculate the ideal MOS curves required. When these curves are obtained, N_{ss} can be

determined directly from (4) above. Convenient steps in performing the surface state analysis are presented and discussed below:

(1) Ideal C–V curves are generated from the measured field plate area, oxide capacitance and doping density.

(2) The measured C–V curve is integrated according to (4) from strong accumulation to strong inversion, to give surface potential as a function of applied voltage to within an additive constant. This measured surface potential change should be compared with the change expected from the ideal C–V curve to assure the absence of gross nonuniformities, as shown in Fig. 5.

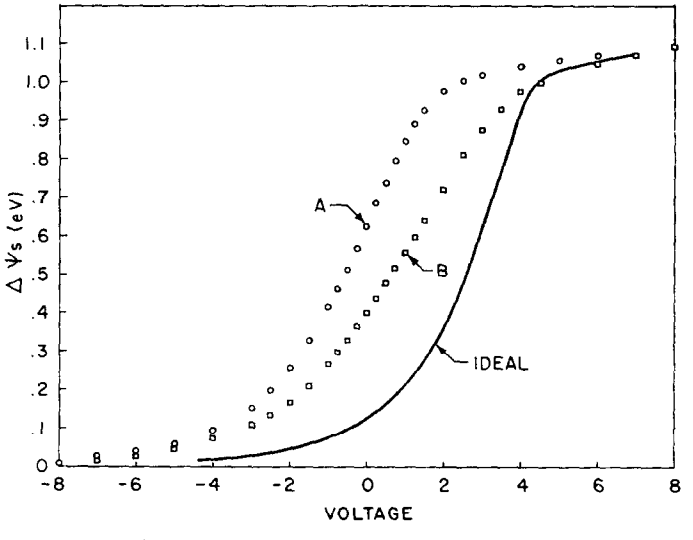

FIG. 5. Surface potential as a function of applied bias. Curves A and B were obtained from the corresponding C–V curves (A and B) of Fig. 3, and are compared with the ideal, calculated $\Delta\psi$ vs. V curve.

(3) A plot of the measured capacitance ratio C/C_{ox} as a function of the experimentally determined surface potential can then be constructed and compared with a similar plot for the ideal MOS structure, to check the internal self-consistency between the actual and ideal MOS structures, and to determine the additive constant Δ. Because the quasi-static technique yields a thermal equilibrium C–V curve, this curve should coincide with the ideal C–V curve both near strong accumulation and also near strong inversion, where the accumulation or inversion capacitances are much larger than the surface state capacitances. The quality of the fit between the curves is a sensitive measure of the internal self-consistency of the structures, while the displacement of the surface potential axes required to establish coincidence of the curves is equal to the additive constant Δ. This additional precision with which quasi-static C–V curves can be compared to ideal C–V curves is highly desirable, since the ideal curve is used to determine N_{ss} according to (8). Figure 6 shows the measured and ideal capacitance vs. surface potential for the 10 Ω-cm n-type MOS capacitor of Fig. 2, and shows the degree of self-consistency obtainable.

(4) Surface state density can now be determined by manipulation of the data according to (4). This is equivalent to taking the difference between the measured semiconductor surface capacitance and the ideal semiconductor surface capacitance at each value of surface potential to yield surface state density. A plot of these two quantities for the n-type sample being analyzed is shown in Fig. 7. The surface state distribution resulting from this analysis is shown in Fig. 8.

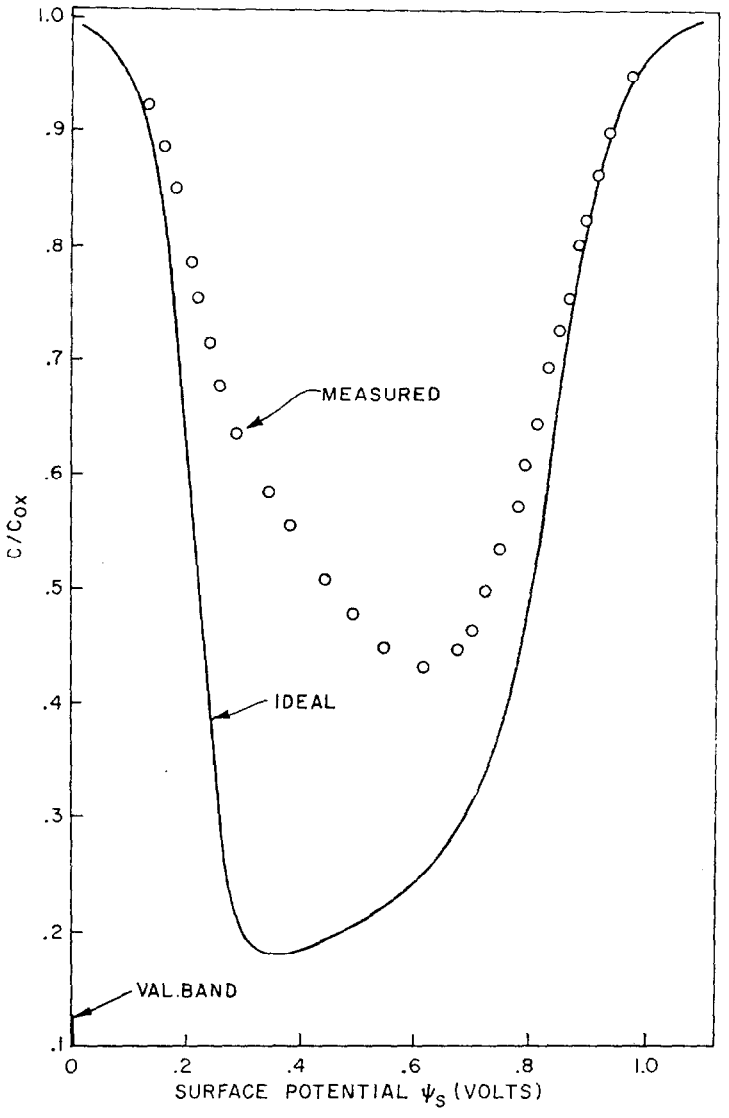

FIG. 6. Measured and calculated curves of C/C_{ox} as a function of surface potential ψ_s, showing the expected agreement in accumulation and strong inversion.

The surface state density shown in Fig. 7 was obtained with the above method on a 10 Ω-cm n-type MOS capacitor with a bias grown steam oxide. For comparison, a composite surface state density curve obtained for a similar bias grown steam oxide by NICOLLIAN and GOETZBERGER[6] using the conductance technique is also shown in Fig. 8. Considering the sensitivity of surface state distribution to fabrication procedure, the agreement between these two curves is reasonably good. To obtain this composite curve by the conductance technique, however, it was necessary to use two separate MOS capacitors, a p-type structure for the points below mid-gap, and an n-type structure for

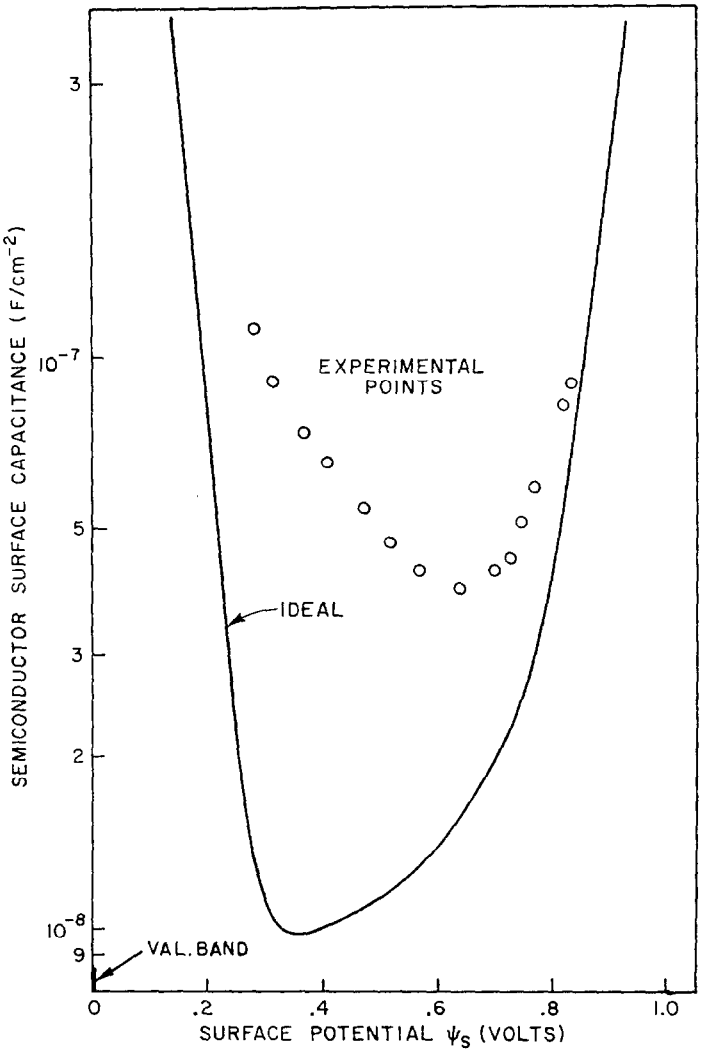

FIG. 7. Measured and calculated curves of semiconductor surface capacitance as a function of surface potential ψ_s. Surface state density at any surface potential is given by $1/q$ times the difference between these two curves.

those points above mid-gap. This immediately points out one of the advantages of the quasi-static technique: The surface state density can be obtained relatively simply over a large part of the energy gap on a single sample.

Furthermore, quasi-static measurements may be combined with high frequency C–V measurements to obtain surface state density directly, but over a restricted energy range without the use of ideal C–V curves, as discussed by CASTAGNE.[1] In the energy range from accumulation to the onset of inversion, the dispersion between the quasi-static capacitance C_{LF} and the high frequency capacitance C_{HF} is directly related to the surface state

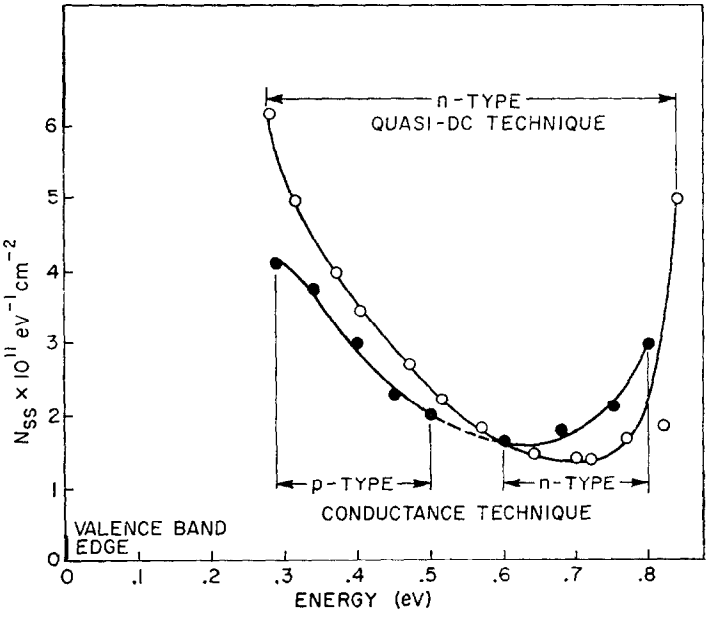

FIG. 8. Surface state distribution obtained from the quasi-static technique for the sample shown in Fig. 2. Surface state distribution on a similar interface obtained with the conductance technique is also shown for comparison.

density as follows

$$N_{ss} = \frac{C_{ss}}{q} = \frac{C_{LF}C_{ox}}{C_{ox}-C_{LF}} - \frac{C_{HF}C_{ox}}{C_{ox}-C_{HF}}. \quad (6)$$

In combination with a quasi-static measurement of surface potential, the surface state energy distribution is obtained. A typical example and results of this procedure are shown in Fig. 9. This approach recommends itself most strongly when the surface state information in the energy range corresponding to inversion is not required.

DISCUSSION

The limiting sensitivity for determination of surface state density from the thermal equilibrium C–V curves is largely determined by the doping density of the semiconductor. This is evident from (4) which shows that the surface state density at any given surface potential is given by the difference between a measured surface capacitance and the ideal semiconductor surface capacitance, C_{sc}. The ideal surface capacitance represents a reference for surface state measurements, and in depletion C_{sc} is proportional to the square root of the doping density. For example, C_{sc} for a 10 Ω-cm silicon sample has a minimum value of about 10^{-8} $F\,cm^{-2}$ near mid-gap; an equivalent surface state capacitance would yield a surface state density of about 1.5×10^{11} states per cm^2 eV. If we assume a 10 per cent uncertainty in C_{sc} due largely to a possible error in the doping density, this would lead to an ultimate sensitivity of about 10^{10} states per cm^2 eV near mid-gap. This example clearly illustrates that both a low doping density and an accurate knowledge of the doping density are needed in order to maximize the sensitivity of this technique.

In the previous section it was shown that, in the absence of hysteresis effects, the inversion layer response is the slowest process in the MOS structure at room temperature. Therefore, one may estimate the magnitude of the sweep rate required to maintain distortion of the C–V curve due to deviation from thermal equilibrium within acceptable limits, by considering the inversion layer response in more detail.

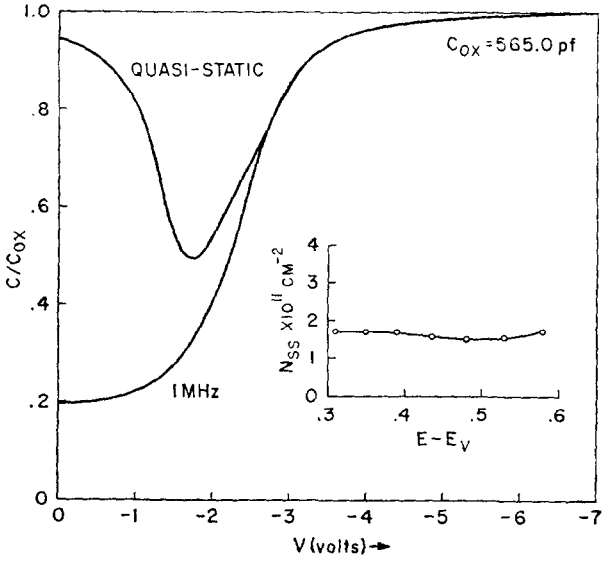

FIG. 9. Combined high frequency (1 MHz) and quasi-static C–V curves for Au–Cr–SiO_2–Si capacitor (10 Ωcm p-type Si, 500 Å SiO_2) and the resulting surface state distribution as calculated from (6). In the energy range of 0.3–0.4 eV the measured surface state density is expected to be in error (smaller than the actual surface-state density), because of surface-state dispersion effects in the 1 MHz curve.

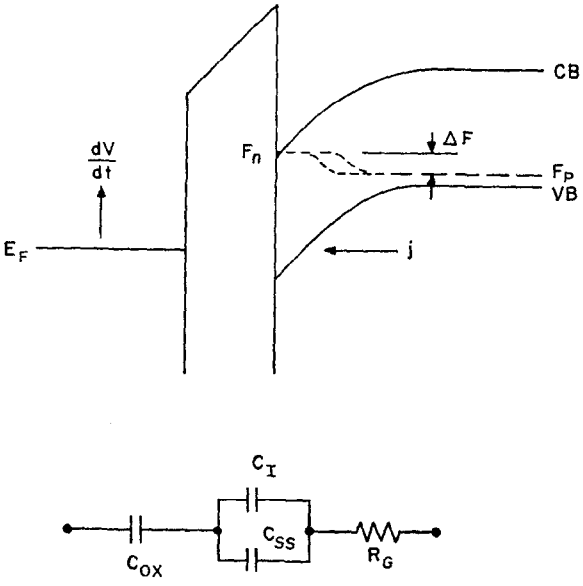

FIG. 10. Band diagram showing deviation from thermal equilibrium ΔF in strong inversion resulting from a finite sweep rate dV/dt, and the corresponding equivalent circuit.

For example, we consider a p-type MOS capacitor swept from strong inversion toward accumulation, as shown in Fig. 10. The charge stored in the inversion layer decreases by recombination either in the depletion region below the inverted surface or through surface states, requiring a net difference ΔF between the quasi Fermi levels at the surface, F_n, and in the bulk, F_p. In strong inversion, recombination through surface states will be small due to lack of majority carriers at the surface; therefore, the displacement current density for small deviation from thermal equilibrium can be related to ΔF, using Shockley–Read recombination statistics, by defining a generation recombination resistance[14] as follows:

$$j_d = \frac{\Delta F}{R_g}, \tag{7}$$

where R_g is the generation–recombination resistance given by $R_g = \tau_0 V_D / q n_i W$ which is valid when $\Delta F \ll kT$, V_D is the effective diffusion potential ($V_D \simeq E_g - \phi_B$) for a strongly inverted surface, τ_0 is the bulk minority carrier life time, and W is the depletion layer width,

$$W = \left(\frac{2\epsilon_s V_D}{q N_a}\right)^{1/2}. \tag{8}$$

The displacement current in strong inversion is essentially determined by the oxide capacitance

$$j_d = C(V)\frac{dV}{dt} \simeq C_{ox}\frac{dV}{dt}. \tag{9}$$

Combining these to eliminate j_d and W, we obtain the relation between the applied sweep rate and ΔF,

$$\Delta F \simeq \left(\frac{N_a V_D}{2q\epsilon_s}\right)^{1/2}\frac{\tau_0}{n_i}C_{ox}\frac{dV}{dt}, \tag{10}$$

which provides an estimate of the deviation from thermal equilibrium under a given sweep rate. For an MOS capacitor on 10 Ω-cm p-type silicon with $\tau_0 = 1\ \mu$sec and 1000 Å of SiO_2 swept at 10^{-2} V/sec in inversion equation (10) yields $\Delta F \simeq 4$meV at a displacement current density of 3.4×10^{-10} A/cm^2 and is in good agreement with our observations. Therefore, in quasi-static measurements the limitation on the sweep rate is primarily determined by the zero bias conductance of the field induced p–n junction below the field plate in inversion.

CONCLUSIONS

Quasi-static C–V measurements on MOS capacitors provide a simple, direct, and accurate method for obtaining the low frequency thermal equilibrium C–V characteristic. Such quasi-static measurements allow full implementation of Berglund's low frequency method for surface potential determination and surface state analysis and provide a test for the presence of gross nonuniformities. Surface potential may be accurately and directly measured, and the surface state energy distribution may be determined over a large part of the energy gap without a graphical differentiation.

Alternatively, quasi-static C–V measurements in combination with high frequency C–V measurements directly yield the surface state energy distribution near mid-gap without the need for ideal C–V characteristics.

The measurement technique is also readily extended with the help of simple analog integrating circuitry to yield automatic plots of surface potential vs. applied voltage and capacitance versus surface potential. This allows a more direct comparison with ideal characteristics and facilitates surface state analysis.

Alternatively, the quasi-static data can be readily digitized, and all manipulation of the data can be carried out in a computer.

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