A RADIATION-HARD SILICON GATE BULK CMOS CELL FAMILY

Charles F. Gibbon
Sandia National Laboratories
Division 2142
Albuquerque, New Mexico 87185
(505) 844-9173

Donald H. Habing
Sandia National Laboratories
Division 2116
Albuquerque, New Mexico 87185
(505) 844-7364

Richard S. Flores
Sandia National Laboratories
Division 2116
Albuquerque, New Mexico 87185
(505) 844-2486

MASTER

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

DISCLAIMER

This book was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

CONF-800703--2

A RADIATION-HARD SILICON GATE BULK CMOS CELL FAMILY

Charles F. Gibbon
Sandia National Laboratories
Division 2142
Albuquerque, New Mexico 87185
(505) 844-9173

Donald H. Habing
Sandia National Laboratories
Division 2116
Albuquerque, New Mexico 87185
(505) 844-7364

Richard S. Flores
Sandia National Laboratories
Division 2116
Albuquerque, New Mexico 87185
(505) 844-2486

Introduction

This paper describes the successful development of a radiation-hardened bulk CMOS technology and a new two-port standard cell family which utilizes all the advantages afforded by a radiation-hard self-aligned four micron poly-silicon gate structure. Characteristic data obtained on the process, and results obtained from random logic circuits designed and laid out using the standard cells are presented to demonstrate the electrical and radiation performance of this technology. Designated the Expanded Linear Array (ELA), the principal objectives of this technology are higher packing density, increased speed of operation, topological design flexibility, compatibility with automated layout and routing techniques, and radiation hardness.

ELA Cell Family

The specific design goals of the ELA cell family include minimum performance characteristics of five to ten nanosecond gate delays and counter frequencies of 20 MHZ at ten volt operation. A total dose hardness of 10^6 Rad (Si) and a transient upset level of $5x10^8$ Rad (Si)/sec. with no latch up at any level have been demonstrated in this technology. The structure and cell layout technique were tailored to allow new cells to be designed easily and quickly and also to provide the capability for expansion and modification of existing cells with a minimum effort as design rules improve.

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

Fundamental assumptions used to derive the complete set of design rules and the prominent resulting feature sizes are summarized below.

1.	Alignment Tolerance	4μ
2.	Substrate Doping and Operating Voltage	10^{15}, 10v
3.	Metal Patterning	15μ pitch; 8μ lines x 7μ spaces
4.	Poly Patterning	20μ pitch; 14μ lines x 6μ spaces (interconnects), 4μ gates
5.	Contact Windows	6μ x 6μ or 5μ x 7μ

Figure 1 shows the ELA structure for a typical two-input gate. n and p transistors are arranged in a linear array; vertical, four micron polysilicon gates are on a fixed 20 micron horizontal pitch, and metal is used to interconnect the appropriate regions. The standard cell height for this cell family is 150μm. An advantage of this layout approach is that feedthroughs are available, and each cell input and output is accessible from both sides. These characteristics are significant in attaining minimum area standard cell chip layouts with automated placement and routing techniques.[1,2]

A continuous p+ guardband surrounds the p-well containing the n-channel devices to assure radiation hardness. The required lateral isolation of devices results from the use of field shields. In this layout approach the guardband area penalty is about five percent.

ELA Process

The process used to fabricate the ELA structure involves nine masks. A p-well is implanted into a 3-6 Ω-cm (100) substrate and driven in to 6μ M. Just after the p+ guardband diffusion, a nonselective phosphorous implant is used to increase the p-channel field threshold. An 8000 Å field oxide is formed; then a 550Å gate is grown in dry oxygen. After depositing, doping, and plasma etching the polysilicon, an aluminum mask is deposited and patterned, and the n+ sources and drains are implanted. The p+ regions are implanted using a photoresist mask. The intermediate dielectric is then deposited; this activates the implants. Contact windows are cut next and an aluminum-silicon interconnect metalization applied.

In order to assure radiation hardness, the ELA fabrication sequence has several features incorporated from earlier work on radiation-hard MOS processing.[3] Two aspects in particular should be noted. First, the gate dielectric is kept as thin as possible (550Å) to reduce radiation-induced threshold shifts. And secondly, thermal treatments after gate oxidation are kept to a minimum.

Test Vehicles

To thoroughly evaluate and characterize both the electrical and radiation performance of the ELA technology, a test chip containing a range of physics devices, test transistors on both gate and field oxides, standard cells, and circuits formed with these cells was designed. The 8-bit Arithmetic Logic Unit (ALU) used as the test circuit in the technology and design evaluation study of the Air Force Fault Tolerant Computer Program was also implemented in this technology. A photomicrograph of the ALU is shown in Figure 2.

Results

A representative sample of experimentally derived electrical parameters for the cell family are shown below.

Gate Propagation Delays		
	5v	10v
Inverter	7-11 ns	3-5 ns
2-input NOR	13-19 ns	6-8 ns
2-input NAND	14-20 ns	6-8 ns

Output Drives (ma) 2 Volts Off Rail	5v		10v	
	n	p	n	p
Output Buffer	7	5	14	9
Standard Cells	1	0.8	1.7	1.0

The cell family can be generally characterized as having 5-10 ns gate delays at 10 volts and 10-20 ns gate delays at 5 volts. Counter operation of 20 MHZ is possible at 10 volts.

Radiation results on both discrete test transistors and on ALU's fabricated with the ELA process show very consistent results. Figure 3 shows the n- and p-channel characteristic threshold shifts as a function of total dose for the two bias conditions of interest. The worst case threshold shift (ΔV_{th}) under gamma radiation is observed for the off (unbiased) p-channel transistor. The n-channels shift slightly toward depletion at moderate doses and then toward accumulation at about 3 to 5 x 10^5 Rads.

Typical gate delays as a function of gamma dose are shown in Figure 4 for 5 and 10-volt operation. At the 10-volt design voltage, delay times typically increase by 10 percent at 10^5 rads, about 50 percent at 3×10^5 rads and a factor of 3 at 10^6 rads. Of particular interest in the evaluation of ALU performance is one critical delay path containing 14 series gates. Figure 5 shows the increased delay in this path; results agree well with that quoted for individual cells. Test circuits have also demonstrated transient upset levels of 5×10^8 Rads (Si)/sec. with no latch up at any level.

Summary

A radiation-hardened bulk silicon gate CMOS technology and a topologically simple, high-performance dual-port cell family utilizing this process have been demonstrated. Additional circuits, including a random logic circuit containing 4800 transistors on a 236 x 236 mil die, are presently being designed and processed. Finally, a joint design-process effort is underway to redesign the cell family in reduced design rules; this results in a factor of 2.5 cell size reduction and a factor of 3 decrease in chip interconnect area. Cell performance is correspondingly improved.

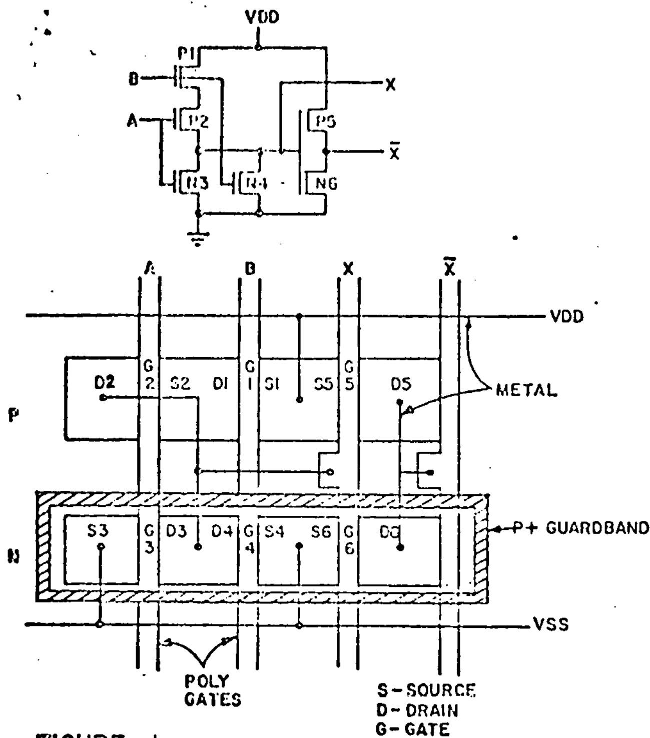

FIGURE- 1
2 INPUT OR/NOR GATE

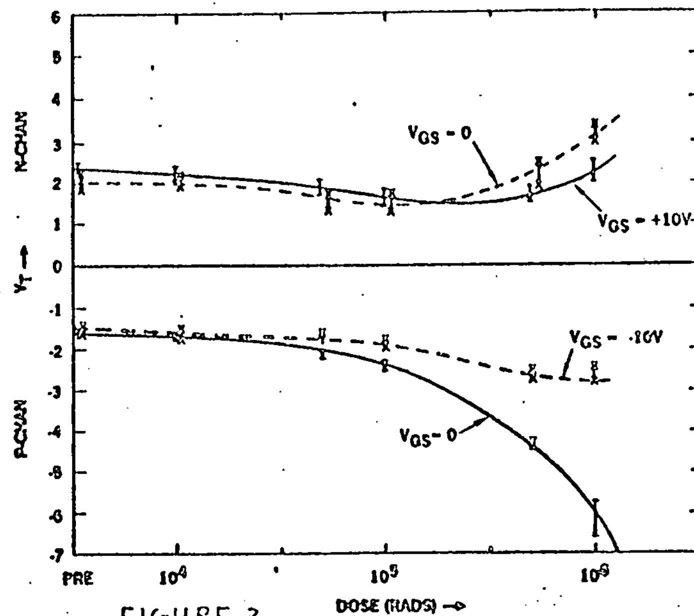

FIGURE 3

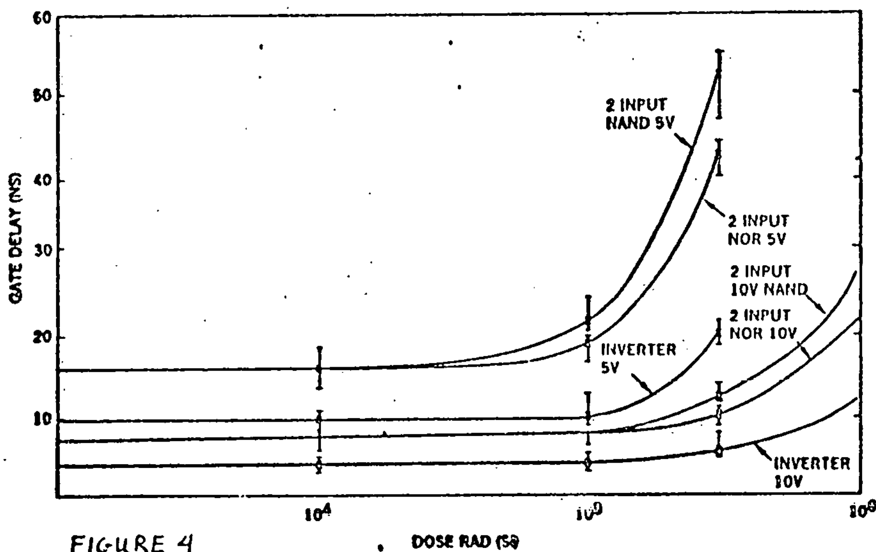

FIGURE 4

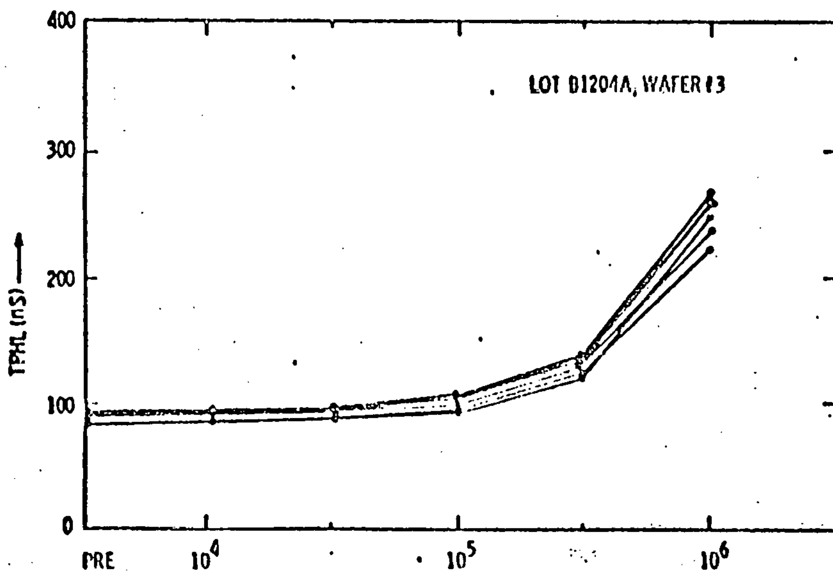

FIGURE 5

References

1. B. T. Preas and C. W. Gwyn, "Methods for Hierarchical Automatic Layout of Custom LSI Circuit Masks." Proc 15th Design Automation Conference, pp. 206-212, June 1978.

2. B. T. Preas, "Placement and Routing Algorithms for Hierarchical Integrated Circuit Layout," Dissertation, Stanford University, August 1979.

3. G. P. Derbenwick and R. L. Gregory, "Process Optimization of Radiation-Hardened CMOS Integrated Circuits," IEEE Trans. Nucl. Sci., Vol. NS-22, p. 2151 (1975).

Acknowledgments

The authors wish to thank B. D. Shafer, J. R. Adams, and W. C. Slemmer for their contributions to the development of this cell family.

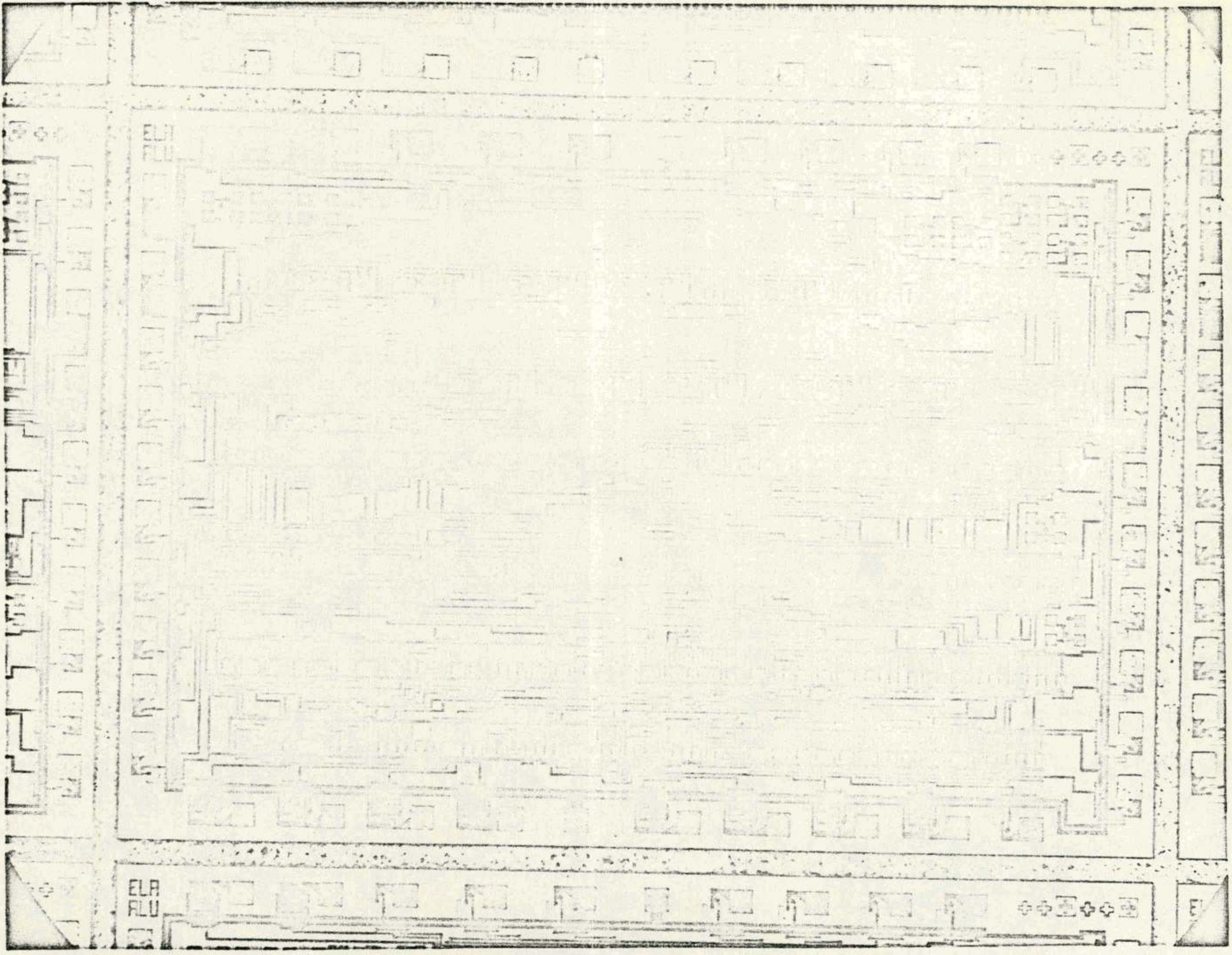

FIGURE 2