A Radiation Imaging Detector Made by Postprocessing a Standard CMOS Chip

Victor Manuel Blanco Carballo, Maximilien Chefdeville, Martin Fransen, Harry van der Graaf, Joost Melai, Cora Salm, *Member, IEEE*, Jurriaan Schmitz, *Senior Member, IEEE*, and Jan Timmermans

***Abstract*—An unpackaged microchip is used as the sensing element in a miniaturized gaseous proportional chamber. This letter reports on the fabrication and performance of a complete radiation imaging detector based on this principle. Our fabrication schemes are based on wafer-scale and chip-scale postprocessing. Compared to hybrid-assembled gaseous detectors, our microsystem shows superior alignment precision and energy resolution, and offers the capability to unambiguously reconstruct 3-D radiation tracks on the spot.**

***Index Terms*—Microsensors, nuclear imaging, radiation detectors, SU-8, wafer postprocessing, wafer-scale integration.**

I. Introduction

FOR RADIATION imaging applications in high-energy and nuclear physics, gas gain grids [1], [2] are commonly used. These grids are punctured metal membranes suspended some micrometers over an anode plane inside a gas volume filled with a gas mixture, such as helium/isobutane. When ionizing radiation (e.g., a cosmic ray particle or an X-ray) crosses the gas volume above the grid, electrons are liberated and driven toward the anode by a moderate electric field (∼1 kV/cm). By applying a high electric field (∼100 kV/cm) between the grid and the anode, each free electron will create an ionization avalanche in this region, yielding an exponential increase in the number of free electrons. The avalanche electrons are collected at the anode. Typically, a charge-sensitive amplifier is used to record arrival time, position, and pulse height. This type of radiation detector is relatively cheap and of low mass, and consumes little power. It finds application in nuclear, high-energy, and astrophysics, as well as biology, medicine, and industrial radiology [3].

When a microchip is used as the anode [4], [5], the signal is directly picked up at the origin, reaching very high sensitivity [schematic in Fig. 1(a)]. The microchip typically has an array of bond pads (for picking up the charge) each connected to a preamplifier and buffer. With a manually mounted grid, misalignment between the holes in the grid and the sensing array on the chip leads to Moiré effects. To overcome these, we pursue the integration of the grid on a chip through wafer postprocessing [6], which is inspired by other microsystems reported in the literature [7]–[11]. After early trials by Key *et al.* [12], we showed the first functional grid made in postprocessing planar technology [13] on bare silicon wafers. In this letter, we present the first results of fully integrated detectors made by microfabrication of a grid on top of CMOS microchips: Medipix2 [14] and Timepix [15], [16] chips were employed. Both wafer postprocessing and chip postprocessing were pursued. Integration of detecting device and readout electronics leads to superior performance at lower projected cost.

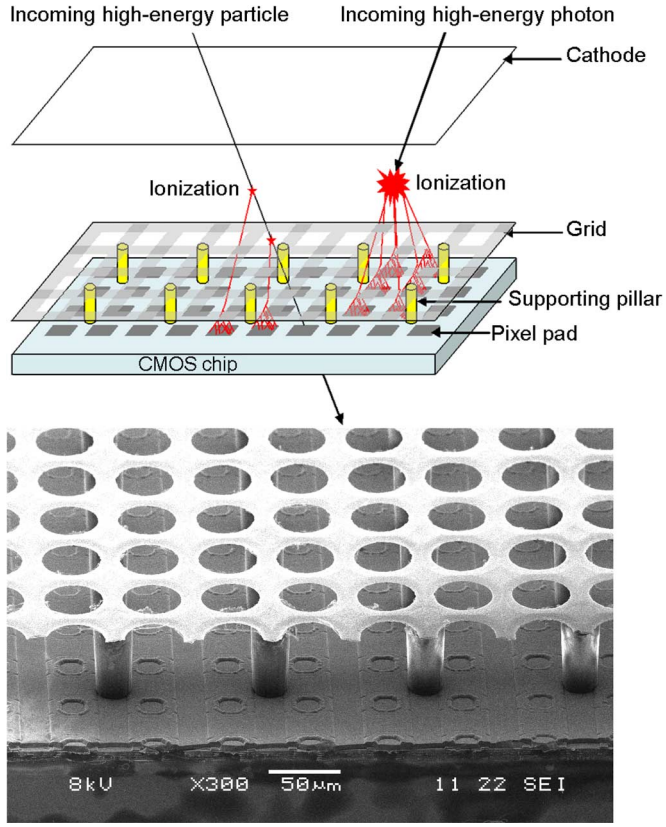

Fig. 1. (Top) Schematic view of the detector. An ionizing particle creates several free electrons that drift toward the CMOS chip and create an avalanche between the grid and the chip. (Bottom) SEM picture of an integrated device.

II. Material and Fabrication Process

The system is built by suspending a conductive mesh over a pixel readout chip supported by 50-μm-high insulating pillars.

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V. M. Blanco Carballo, J. Melai, C. Salm, and J. Schmitz are with the MESA+ Institute for Nanotechnology, University of Twente, 7500 AE Enschede, The Netherlands (e-mail: j.schmitz@utwente.nl).

M. Chefdeville, M. Fransen, H. van der Graaf, and J. Timmermans are with the National Institute for Nuclear Physics and High Energy Physics, NIKHEF, 1098 SJ Amsterdam, The Netherlands.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

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We chose SU-8 negative-tone resist [17] as pillar material. This well-documented resist can be used as both a sacrificial layer and a structural support [18], it can be spin coated in a thickness ranging from a few micrometers to a millimeter [19], and it is patterned with standard lithography. Its low temperature budget (below 95 °C) makes it CMOS postprocessing compatible, and it is radiation hard [20].

Sputtered aluminum was used as metal for the conductive grid. It exhibits low residual stress, can easily be etched and bonded, and shows good adhesion with SU-8 [21]. However, metal deposition over unexposed SU-8 may lead to cross-linking, through generation of ultraviolet light, or heat transfer. The literature reports the use of thermal evaporation [18], [22], and the use of a "light absorption layer" [23] or a metal mask [24] to circumvent this problem. We have chosen to deposit a layer of standard positive resist (Fujifilm OiR 907) over the SU-8 and expose both at the same time. The positive resist protects the SU-8 during sputter deposition, avoiding the cross-linking of the SU-8. It is selectively removed by wet etch in a later stage.

Fig. 1(b) shows a scanning electron microscopy (SEM) image of the final integrated device, where a punctured aluminum grid is suspended over a Medipix2 chip by SU-8 pillars placed in the middle of four pixels. More details about the fabrication process can be found in [25].

The fabricated prototypes are screened by optical inspection and electrical test (isolation between grid and chip, and capacitance–voltage measurement to verify the rigidity of the suspended membrane). Wafer-level fabrication in our (university) laboratory presently reaches a yield of above 80%, which is similar in chip-level fabrication. Our process allows for chip reprocessing in case of grid imperfections.

III. Result

The postprocessed chips were wire bonded on a printed circuit board (PCB) and placed inside a sealed chamber (note that no package is required for this microsystem). The chamber is flushed with a helium/iC$_4$H$_{10}$ (80/20) gas mixture, which leads to a low risk of sparks. The resistance of the microsystem against sparking was significantly improved with a spark protection layer (amorphous silicon directly deposited on the chip) [26], also allowing operation in other gas mixtures, such as argon/iC$_4$H$_{10}$ (95/5). The PCB was connected to a computer to read out the chip. The Medipix2 chip stores the number of electron avalanches that have reached every pixel; the Timepix chip, in addition, provides the time or charge information of the avalanche (this avalanche must contain more electrons than the threshold of the pixel, calibrated about 1000 electrons, to be detectable). The performance of the digital-to-analog converters and the number of dead pixels in the chips did not change after the postprocessing.

The devices were irradiated with 6-keV photons produced by an ^{55}Fe radioactive source. The integral image of the hits per pixel is shown in [Fig. 2 (inset)]. To (quickly) illustrate imaging capability, a circular metal nut was placed on top of the chamber, locally absorbing the ^{55}Fe photons. We obtained a homogeneous response as the Moiré effect is eliminated through the alignment between the holes in the grid and the pixels in the chip. During ^{55}Fe irradiation, tracks of alpha particles also crossed the detector area, as shown in [Fig. 2 (inset b)].

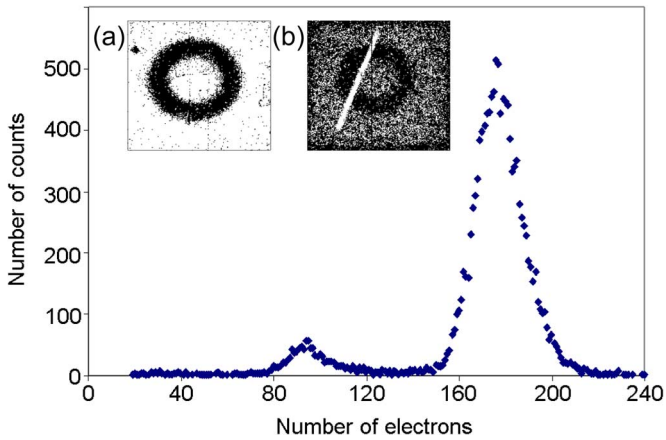

Fig. 2. Detector performance illustrated from X-ray radiation response, operating at 335 V on the grid in Ar/iC$_4$H$_{10}$ (95/5). The histogram shows a count spectrum of ^{55}Fe radioactive decays reconstructed from summing up single-electron avalanches. The insets show the imaging capability of the detector: (a) shadow image of a circular nut being irradiated with ^{55}Fe and (b) a similar image disturbed by an alpha particle crossing the detector area during data collection. The chip's sensitive area is 14 × 14 mm^2.

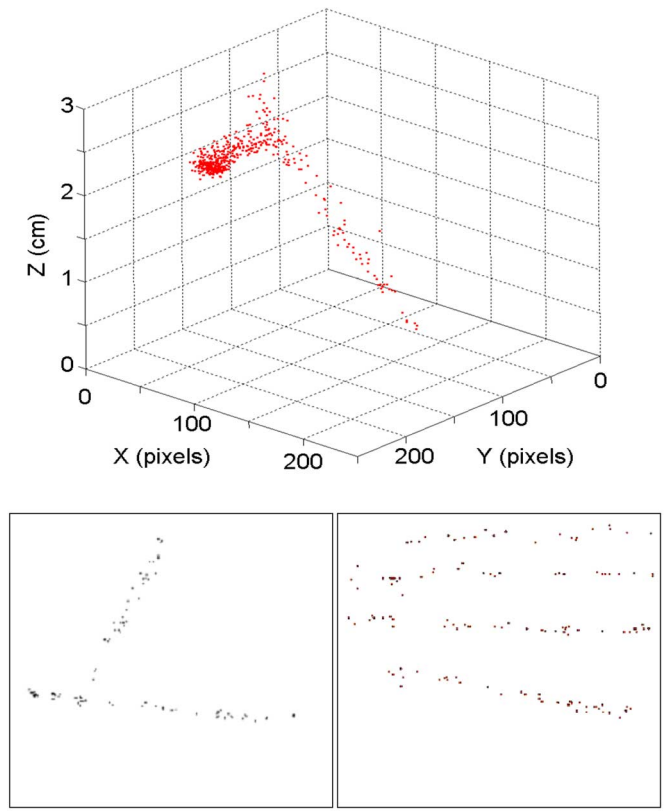

Fig. 3. Tracks of high-energy ionizing particles crossing the detector. (Top) An electron originating from ^{90}Sr radioactive decay, diagonally crossing, and emitting a horizontal delta-ray on its way. The X and Y coordinates are known from the pixel array; the Z coordinate is reconstructed from the signal arrival time. (Bottom) 2-D cosmic rays tracks (left: 2 tracks, right: 4 tracks). The figures illustrate the detector's imaging capability for high-energy ionizing particles, such as cosmic rays.

Using a distance of 10 cm between the cathode and the grid, and a gas mixture with high transverse diffusion (Ar/iC_4H_{10} 95/5), the primary charge of a ^{55}Fe photon conversion can be spread across the chip surface. The number of activated pixels is then a direct measure of the number of primary electrons. The ^{55}Fe spectrum reconstructed in this manner is shown in Fig. 2. A single-electron efficiency of 80% is deduced from this spectrum at 335 V on the grid.

With such a single-electron efficiency, cosmic rays passing the detector area can be visualized, and their trajectory can be reconstructed. Typical tracks of ionizing particles, both from a ^{90}Sr radioactive source and from cosmic rays, are displayed in Fig. 3. Using the Timepix microchip, the arrival time of electrons is also recorded, allowing the reconstruction of 3-D tracks [Fig. 3 (top)].

Several prototype detectors were continuously operated for several months in He/iC_4H_{10} and Ar/iC_4H_{10} while recording cosmic ray events and other types of radiation. We found stable and unchanged operation. Various reliability tests on the microsystem, such as temperature and moisture cycling, and tests of mechanical integrity, are ongoing.

IV. Conclusion

We have designed, realized, and tested an integrated gaseous pixel detector on several different pixel chips from 0.25-μm foundry CMOS. It consists of a punctured metal mesh supported by insulating pillars placed over the unpackaged chip. This integrated radiation imaging detector exhibits state-of-the-art tracking capabilities for ionizing radiation, good single-electron efficiency, and stable long-term operation. The straightforward CMOS postprocessing scheme allows mass production of this new detector at low cost.

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