A ratio metric analog-to-digital converter for eddy current displacement sensors

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To my parents

Declaration of Authorship

I, Ali Fekri, declare that this thesis titled, 'A ratio metric analog-to-digital converter for eddy current displacement sensors' and the work presented in it are my own. I confirm that:

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- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
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Abstract

Faculty of Electrical Engineering, Mathematics and Computer Science
Electronic and Instrumentation

Master of Science

by Ali Fekri

Displacement sensors are widely employed in industry for measuring position and movement of objects as well as for measuring other physical quantities like pressure, acceleration, etc., which can first be converted into movement. This thesis describes the implementation of a ratio metric analog-to-digital converter (ADC) for an eddy current displacement sensor interface. The interface which has been implemented by Dr. Nabavi as a PhD project, consists of a low-power front-end oscillator and a synchronous demodulator. An excitation frequency of 20 MHz enables the accurate sensing of targets with only a few tens of µm thick conductive surfaces. The ADC sampling frequency is 1.25 MHz, which provides an over-sampling ratio (OSR) of 312. The sampling frequency is obtained from the excitation frequency, which synchronizes the ADC and the interface. A ratio-metric measurement approach is applied to suppress the oscillator's noise contribution. The ratio-metric ADC has been realized in a 0.35µm BiCMOS technology and consumes 1.8mW. Measurement results demonstrate a total harmonic distortion of about -85dB, and a resolution of 16 bits within 1 kHz signal bandwidth.

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Chapter 1.

Introduction and background

Introduction

Displacement sensors are some of the most versatile sensors in industry for measuring the position of an object. By converting quantities such as acceleration, pressure, etc., into movement, displacement sensors can also be used to measure these quantities. The variety of quantities that can be measured make displacement sensors one of the most extensively employed sensors in industry. [1]

There are different types of non-contact displacement sensors used in industry, of which Eddy Current Sensors (ECS) are one type. The objective of this master project was to design a dedicated analog-to-digital converter for an ECS, operating with the analog read-out circuit implemented in [Nabavi]. Embedding an analog-to-digital conversion in the ECS interface enables local signal processing, provides sensor network capability, and enhances the creation of smart features in the ECS interface. In this chapter, first the operation principle of ECSs will be presented together with the operation principle of the ECS read-out circuit. Finally, the specification of the desired ADC and the design challenges will be explained. [1]

1.1 Eddy Current Sensor (ECS) operation principle

There are different types of non-contact displacement sensors which are popular in industry. Optical/laser, capacitive and eddy current sensors are the most commonly used. The best accuracy/measurement-range combination can be achieved by incremental optical lasers such as interferometers and encoders. However, the drawbacks of these types of sensors are first their price, which is quite high, and second their bulky size, which is due to their complex structure. On the other hand, two other types of non-contact sensors: capacitive and eddy current sensors, are good candidates when the absolute value of the position is the main target of the measurement, and the dynamic range is limited. They have many advantages such as being compact, robust, stable, accurate and relatively low cost. [1]

Studying the operation of capacitive and eddy current sensors in more detail shows that there is a similarity in their principle. For example, in both cases, sensors represent reactance

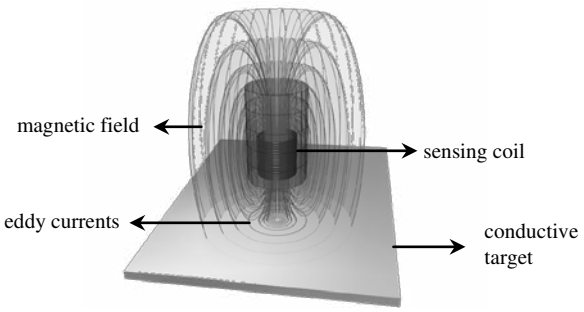


Fig. 1.1. Conceptual illustration of the eddy current sensing principle [1].

in electrical circuits. This means that they do not consume electrical energy and hence they are noiseless in ideal cases. In addition, both sensors have the same structure. What is used in an ECS with a flat sensing coil is similar to the sensing electrode of a capacitive sensor. Therefore, they can use the same material. Hence, the reason for the differences in the performance of these two sensors can be found in their sensitivity to working environment variations, the properties of their targets, and the performance of the utilized electronic interfaces [1].

The operating principle of an ECS is based on magnetic induction. The magnetic field created by the sensor induces eddy currents in the target (see Fig. 1.1). The target displacement causes the magnetic field, as well as the equivalent inductance of the coil, to change. The inductance measured by the electronic interface carries information about the target displacement. Since magnetic fields are not sensitive to the presence of contaminants such as oil, dirt, dust, etc., ECSs operate well even in polluted environments [1]. Moreover, unlike capacitive sensors, ECSs do not require electrical contact with the target since the sensing coil and the target communicate via magnetic coupling. This is an advantage in many applications where non-contact displacement measurement is needed.

Of course, ECSs also have some imperfections which need to be studied well and compensat for in order to achieve the above-mentioned advantages of ECSs and to create a high-performance displacement sensor based on the eddy-current principle.

The first imperfection is related to the eddy current penetration depth δ. When δ is comparable to the measured displacement range, any change in δ introduces a measurement error. This error is caused by changes in the intensity of the total magnetic field and hence changes in the value of the equivalent inductance. The intensity of the eddy currents weakens as they penetrate deeper in the target. This phenomenon is called “skin effect”. Therefore, a smaller depth will help the eddy current to reach a stronger intensity. Moreover, when the displacement of a thin target (e.g. a membrane) has to be measured, a low penetration depth is essential in order to maintain high measurement sensitivity and to reduce the impact of the

eventual presence of conductive objects behind the target on the measurement result. The penetration (skin) depth δ of eddy currents is defined as [1]:

$$\delta = \sqrt{\frac{2}{\omega_{exc}\mu\sigma}} \quad , \tag{1.1}$$

where μ and σ are the target permeability and conductivity, respectively. Since the penetration depth is inversely proportional to $\sqrt{f_{exc}}$, an n-times reduction of δ requires a frequency increase of n^2 times. Therefore, the electronic interface has to operate at a significantly higher f_{exc} in order to suppress the effect of this imperfection [1].

Another imperfection is the mechanical instability of the coil. Basically, a coil with many stacked turns and a complicated structure is less mechanically stable. Moreover, in some applications, the bulky coils are not suitable and cannot be employed.

Employing a higher excitation frequency f_{exc} will help to decrease δ and hence to reduce the skin effect. Also, reducing δ will make the displacement measurement result less sensitive to changes in the electrical properties of the target, due to, for example, temperature variations.

To solve the mechanical instability, simple flat coils with a few turns and a limited volume can be utilized. However, such simple coils have limited inductance. As a result, to make the coil impedance variation measurable, again, a higher excitation frequency f_{exc} is required. Measuring such small inductances with a high resolution (in the pH range) and a high enough excitation frequency (x10 MHz) has been so far feasible only with standard massive LCR meters. However, employing such bulky tools in today's industrial machines is not possible [1].

In the end, another reason to aim for a higher f_{exc} is the higher quality factor that can be achieved for the sensor, which can significantly help to reduce sensitivity to stray magnetic fields. However, as mentioned above, applying a high excitation frequency makes the challenges to the interface electronics much greater when high resolution, wide signal bandwidth, high stability, and low power consumption are needed. In the next section the implemented analog front-end will be briefly discussed [1].

1.2 Implemented analog front-end

As mentioned in the previous section, to overcome the imperfections of the eddy current sensors, we need to increase the excitation frequency, which results in more challenges in design of the electronic interface. Operating with a higher excitation frequency and achieving the needed resolution, stability, etc., results in an increase of the power consumption. In its turn, higher power consumption will increase the heat generation, causing an increase in the sensor temperature, and hence thermal drift of the output signal. Furthermore, introducing a local heat source is not an option in tightly controlled working environments. Due to the fundamental trade-offs in the integrated circuit technology between power consumption, operating frequency, stability and resolution, achieving a high performance at a higher f_{exc} becomes challenging.[1]

1.2.1 Oscillator

Figure 1.2 shows the implemented resonating front-end circuit which will detect the variation of two inductances caused by movement of the target. This resonator is realized by the two sensing coils and the capacitor $C_{o.}$ This configuration provides one resonance even when the coils have different inductances. This can be explained by deriving the expression for the impedance, which is seen by the –Gm stage. If the effect of the coil ohmic losses is neglected, the equivalent impedance at the input of the –Gm stage for Fig. 1.2 is:

$$Z_2(\mathrm{s}) = \frac{(L_1+L_2)\cdot \mathrm{s}}{(L_1+L_2)\cdot C_0 \mathrm{s}^2 + 1} \quad . \tag{1-2}$$

In expression (1-2), the root of the denominator defines the oscillation frequencies of the corresponding circuits. As explained above, because this expression has only one root, there is also only a single oscillation frequency, therefore if the coils have different inductances there is still only one resonant frequency.

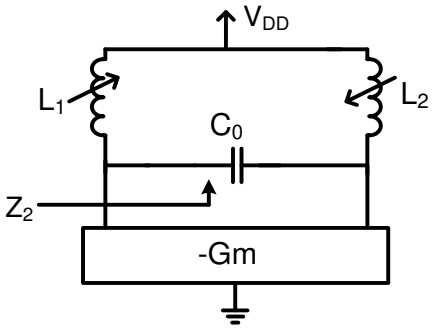


Fig. 1.2. The implemented front-end [1].

In this oscillator the negative transconductance can be realized with cross-coupled transistors in order to compensate for the coil series resistances, as depicted in Fig. 1.2. In this case, if the target between the two coils starts moving, the impedance of the coils and hence the voltage over them will also change in the opposite direction.

Drifts associated with the oscillator can deteriorate the stability of the oscillator output amplitudes. If the biasing current I_b or the switching efficiency drifts due to temperature variations and/or *1/f* noise, then the output amplitudes also drift, although the sensor inductance may not change. Such drifts can be suppressed by using ratio-metric measurement. We consider the following read out function D_{out} :

$$D_{out} = \frac{|V_{O1}| - |V_{O2}|}{|V_{O1}| + |V_{O2}|} \cong \frac{L_1 - L_2}{L_1 + L_2} = \frac{\Delta L}{L_0} \text{ [1]}. \quad (1\text{-}3)$$

As a result, by using the ratio-metric measurement, the non-idealities due to the drift of the oscillator and any noise which comes through the biasing transistor of the –Gm will ideally be removed. In the next three sections are discussed the effect of the ratio-metric measurement on the interface noise performance, as well as important factors limiting the ratio-metric effectiveness in improving the measurement resolution/stability [1].

1.2.2 Voltage-to-current converter (Gm) stages

To achieve high-resolution and stability, an efficient synchronous demodulator must provide a linear mixing operation. This is because the effectiveness of the ratio-metric function in suppressing multiplicative noise/drifts depends on this linearity. A linear mixing operation requires a linear voltage-to-current conversion. This demand will not be fulfilled by just using a single transistor to convert the input voltage into an output current due to the non-linear V-I transfer characteristic of the transistor, resulting in harmonics of the output current. To overcome this issue a linear voltage-to-current converter (i.e. the so-called transconductance stage) substitutes the single transistor solution.

The simplified architecture of the demodulator proposed in [1] (including two channels) is depicted in Fig. 1.3. The output voltages of the front-end oscillator are converted into fully-differential output currents by two transconductors G_{mt}. The G_{mt} stages are capacitively coupled to the oscillator to eliminate the DC component at the oscillator outputs. The output currents of the G_{mt} stages are also capacitively coupled to passive mixers (or choppers) to

[1] $L_1 = L_0 \pm \Delta L$ and $L_2 = L_0 \mp \Delta L$, where L_0 is the inductance value when both coils have the same amount of inductance (in a differential assembly as in Fig. 2.7, when the target is positioned in the middle between the coils).

demodulate the displacement information. This capacitive coupling prevents any DC output currents from being up-converted by the mixers, which helps to reduce the high-frequency ripple at the output of the demodulator. To facilitate a down-conversion to the baseband, a synchronized clock signal is needed to control the switches. This signal is provided by using a comparator that detects the polarity of the oscillator differential output voltage. The comparator controls the switches of the mixers. Another source of the common-mode multiplicative error is the offset of this comparator, which will again be suppressed by utilizing the ratio-metric measurement.[1]

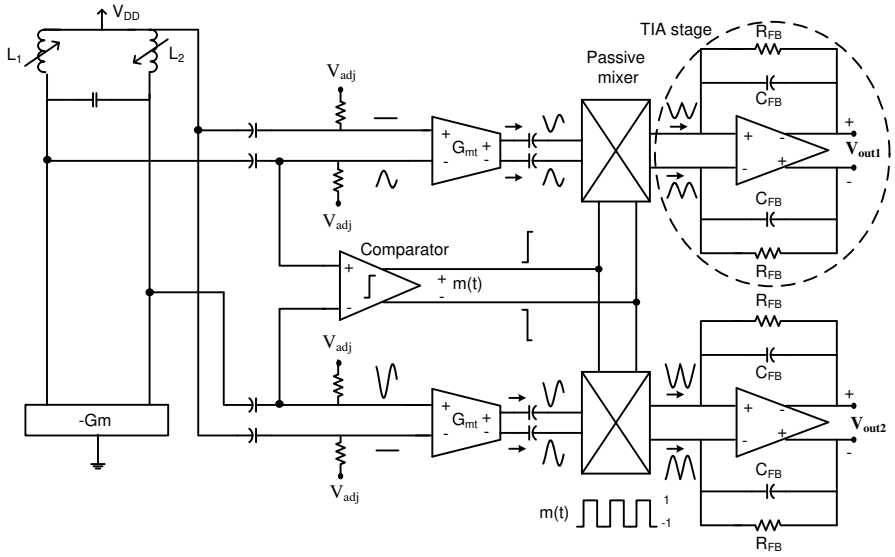


Fig. 1.3. Implemented ECS interface architecture using the synchronous detection principle [1].

Finally, the two demodulated currents, with some high frequency ripples, are pre-filtered and converted into voltage by two transimpedance amplifier (TIA) stages. The outputs of the TIA stages are applied to off-chip RC filters that further limit the bandwidth to a few kHz, which is in line with the signal bandwidth of interest. Finally, the outputs are digitized by an external analog-to-digital converter, after which the ratio-metric calculation is performed in the digital domain. [1]

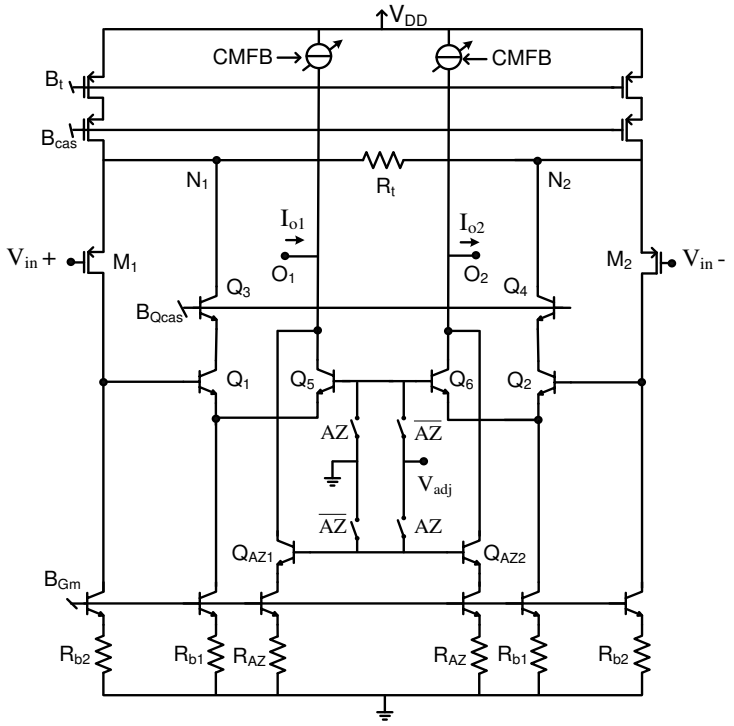


Fig. 1.4. Circuit diagram of the implemented G_{mt} stage ($G_{mt} = 1 / R_t$)[1].

Figure 1.4 shows the implemented circuit of the G_{mt} stage. The current consumption of the G_{mt} stage can be defined based on the targeted THD along with stability/noise requirements of the interface. In order to effectively suppress the multiplicative errors, the demodulator should be sufficiently linear, as mentioned above. This linearity should be on a level that introduces a total harmonic distortion no greater than that of the oscillator. This enables effective correlated-noise suppression when performing the ratio-metric measurement, and prevents the transconductance stages from deteriorating the overall linearity of the interface.

Common-mode feedback and DC servo loops

In order to control the common-mode output voltage of each transconductance stage, a common-mode feedback (CMFB) loop is employed. However, in addition to this block, another block is needed to fix the DC value of each branch separately, since the outputs of the G_{mt} circuit are capacitively coupled to the virtual grounds of the TIA stage,. This is because any small DC differential input or mismatch can cause the high-impedance output nodes to saturate. To avoid saturation, DC servo loops are employed to control the DC differential output voltage.

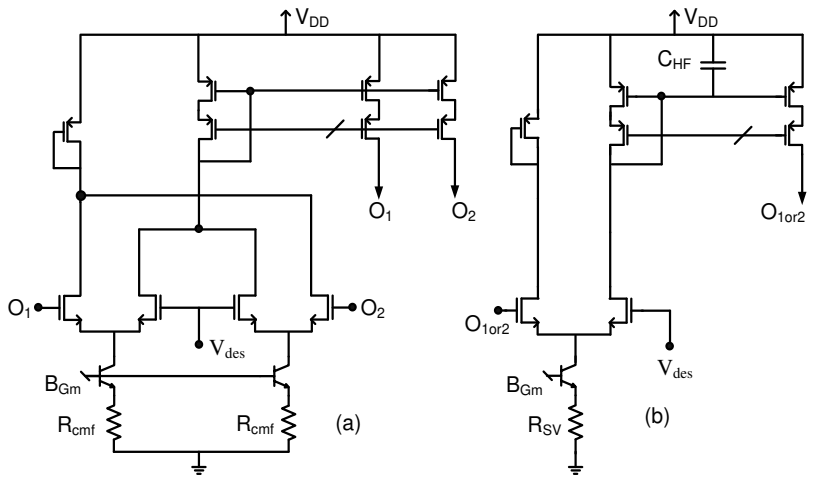


Fig. 1.5. (a) Circuit diagram of the common-mode feedback of the G_{mt} stages; (b) circuit diagram of the DC servo loops [1].

Fig. 1.5 depicts both feedback loops. The CMFB stage compares the average of the output

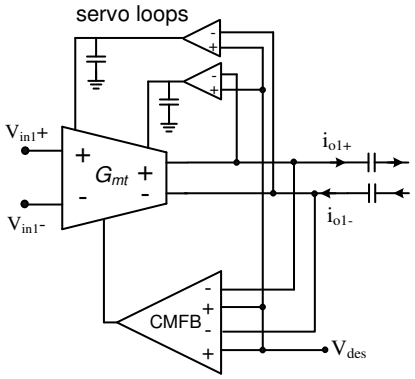


Fig. 1.6. Output voltage control loops of the transconductance stage [1].

voltages with a desired level V_{des} , while the servo loops compare the individual output voltages with V_{des} .

Figure 1.6 shows both the CMFB and the servo loops at the top level. It should be mentioned that servo loops are disabled at high frequencies by C_{HF} [1].

1.2.3 Comparator and mixers

Fig. shows the circuit diagram of the comparator. Three different functions are realized in the employed continuous-time comparator: pre-amplification, positive feedback, and post-amplification.

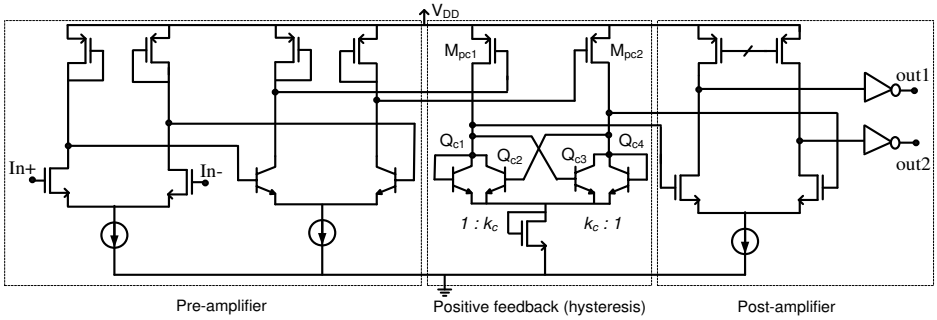


Fig. 1.7. Circuit diagram of the comparator[1].

The positive feedback stage is the core of the comparator since the decision point is mainly defined by this stage. Assume the currents of M_{pc1} and M_{pc2} are equal, and k_c=1: as soon as the current of M_{pc1} increases, the positive feedback provided by the BJTs will make the decision, eventually leading to the drain voltage of M_{pc1} increasing and that of M_{pc2} decreasing. The speed of the positive feedback network is related to the transconductance of the BJTs along with the parasitic capacitances existing at the input of this network [1].

1.2.4 TIA Stages

The TIA stages are realized by the two-stage cascode-compensated operational amplifier shown in Fig. . The amplifier can be designed so that its gain is larger than the desired dynamic range at the targeted bandwidth.

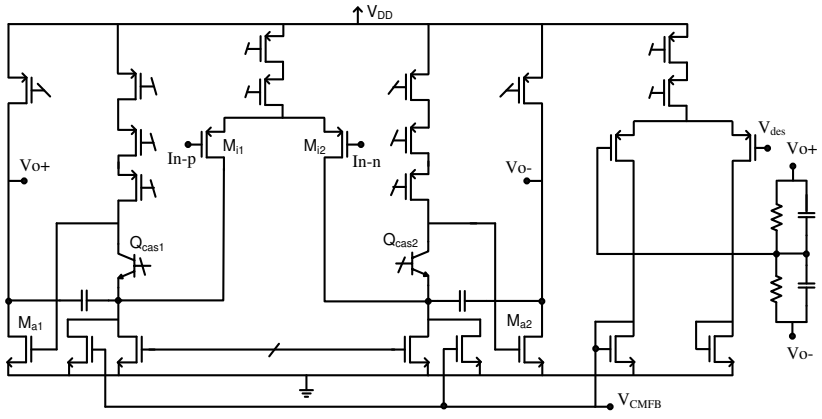


Fig. 1.8. Circuit diagram of the amplifier employed in the TIA stages.[1]

Using a two-stage architecture offers large enough gain which makes the amplifier gain error negligible. Moreover, the amplifier CMFB can be readily implemented using passive resistors[2] while still satisfying the desired gain requirement. As seen in Fig. , the common-

[2] Using passive resistors in the CMFB loop for averaging is beneficial since the amplifier swing is not limited by the CMFB circuit.

mode level is determined by a single loop which compares the average of the output voltages with the desired level. The generated control voltage is then fed back to the tail current sources of the first stage. Based on simulation results, the unity gain frequency of the OTA is about 55 MHz with a phase margin of more than 55° at a load of 10 pF. The amplifier gain is about 90 dB at 1 kHz (and is above 120 dB around DC), and its power consumption is approximately 1.8 mW. [1]

1.3 Analog-to-digital conversion challenges

As discussed in the previous sections, a dedicated analog-to-digital converter is needed for the implemented read-out circuit of Eddy Current Displacement sensors. This ADC needs a resolution above 16 bits with a 1 KHz signal bandwidth. The power consumption budget should not exceed 2 mw. Above all, due to the importance of the ratio-metric aspect, which was studied in the previous sections, it is highly recommended to have a ratio-metric conversion in the proposed ADC. Another task of this ADC is to filter out two main important ripples, one at 2×20 MHz and one at the chopping frequency (156KHz), which appear in the input voltage signals due to the existence of the mixers in the demodulator and also the chopping of the TIA stages . Furthermore, using the existing blocks of the interface as part of the ADC could be a good solution to save power consumption.

Among the various types of ADCs, based on the requirements of the ADC in this application, “Dual Slope” and “Delta Sigma” converters are considered the best candidates for this task. These two converters will be discussed in detail in Chapter2.

1.4 Summary

In this chapter, an introduction on eddy current displacement sensors was provided. In addition, the challenges in designing each block of the implemented read-out circuit, including the oscillator, the voltage-to-current converters, the comparator and the TIA stages, were briefly discussed. Finally, based on the implemented read-out circuit, the challenges in designing the dedicated ADC according to the specifications of the needed ADC were discussed. According to the required resolution and the conversion time, two topologies were proposed which will be discussed in the next chapter.

Chapter 2.

Possible solutions to realize the ADC

2.1 Methods to obtain a ratio-metric digital output

As discussed in chapter 1, obtaining a ratio-metric digital output is important because it will suppress all correlated multiplicative errors of the two analog input signals. There are three ways to obtain a ratio-metric digital output. The first one is to digitize each channel separately and to calculate the ratio-metric value of the digitized signals in the digital domain. Secondly, it is possible to digitize the signal ratio X/Y by using one channel as the input and the other as the ADC reference voltage, and then later by finding the desired output in the digital domain with the formula: ((X/Y) -1)/ ((X/Y) +1). The final solution is to produce a digital output directly corresponding to (X-Y)/(X+Y).

The advantage of the first approach is that more information becomes available as each channel is digitized separately. On the other hand, the great benefit of the second and the third solutions is that one ADC channel is omitted, which leads to a considerable reduction in power consumption. Furthermore, by measuring the ratio of input signals there is no need to provide a reference signal. To realize a ratio-metric function during the analog-to-digital conversion, one of the input analog signals can be used instead of a reference.

As depicted in Fig. 2.1, based on the required resolution and BW, and the ratio-metric principle of operation, only two types of ADCs are identified which could be used: dual-slope ADCs and delta-sigma ADCs.

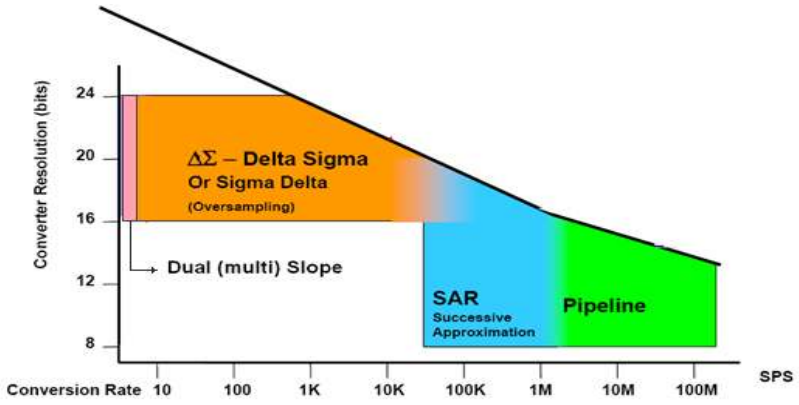


Fig. 2.1. Different types of ADCs based on resolution and conversion rate.[3]

2.2 Dual Slope ADCs

Based on what was discussed in the previous chapter, a high resolution (16-bit) A/D converter with a relatively small bandwidth (1KHz) is needed. Usually, for low speed conversions, integrating types are best candidates. With these types of conversions, like dual slope converters, an analog input signal is converted into a time. Then this time is counted by a digital counter. In fact, the reason that makes this type of ADCs low-speed is this counting procedure. The system diagram of a dual-slope ADC is depicted in Fig. 2.2. [5]

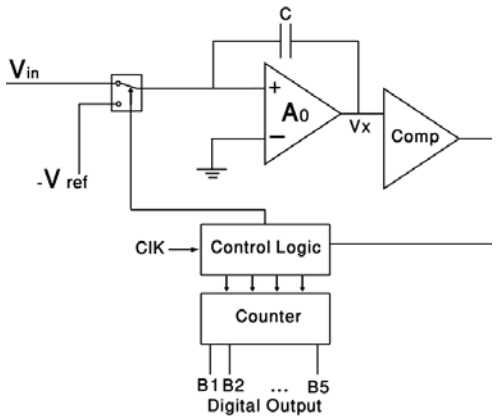


Fig. 2.2. Block diagram of the dual-slope analog-to-digital converter.[5]

Due to some main disadvantages, this type of ADCs cannot be good candidates for ECS interface application. ADC operates in two phases. In the first phase, for a fixed time called t_1 , input voltage is integrated. This time is for the full count of the counter. In the second phase, reference voltage will discharge the integrator. During this phase counter is also working until the moment the output of the comparator change. The time during which the integrator is discharged by the V_{ref} is t_2. Figure 2.3 shows the timing diagram of this conversion. [5]

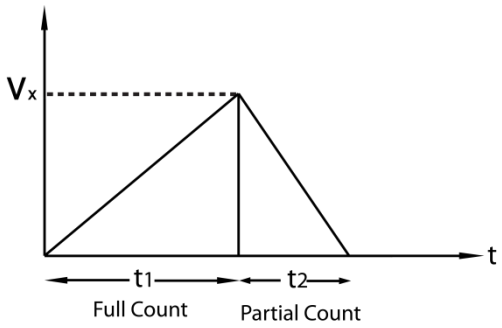


Fig. 2.3. Timing diagram of the dual-slope analog-to-digital converter.[5]

The relation between time and voltages is

$$V_{in} = V_{ref} \times \frac{t2}{t1} \tag{2-1}$$

This method can be used to digitize the two analog outputs of an ECS by using channel X as one input and channel Y as the reference of the dual slope ADC. However, there is a big disadvantage of this method. For a conversion time below 0.5 millisecond, corresponding to 1 kHz signal bandwidth, and a 16-bit resolution, a very high clock frequency is required, which raises the power consumption. To lower the clock frequency, a multi-slope ADC can be implemented. However, this deteriorates the integral and differential non-linearity. [5]

Another disadvantage of the dual/multi-slope ADC method is that the obtained ratio of the two input signals is related to their values at different moments of time. In other words, while the integrator is being charged for a fixed time t_1 by channel X, the value of channel Y, which is used as a reference, is also changing. This reduces the efficiency of suppressing the correlated noise of the two input signals, which is the main goal of using "ratio-metric" values. This noise is caused by the tail-current source of the front-end oscillator and acts as an identical multiplicative error for both channels, which ideally are removed by using ratio-metric conversion, as described in chapter one. [5]

2.3 Delta-sigma ADCs

2.3.1 CT and DT delta-sigma ADCs

There are two types of delta-sigma ADCs: discrete time (DT) and continuous time (CT). The former is implemented by switched-capacitor circuits and the latter by an active RC or by Gm-C blocks. Figure 2.4 shows the block diagram of a continuous-time (CT) ΣΔ modulator. As it is shown in this type of ADCs sampling function happens after the integration. [4]

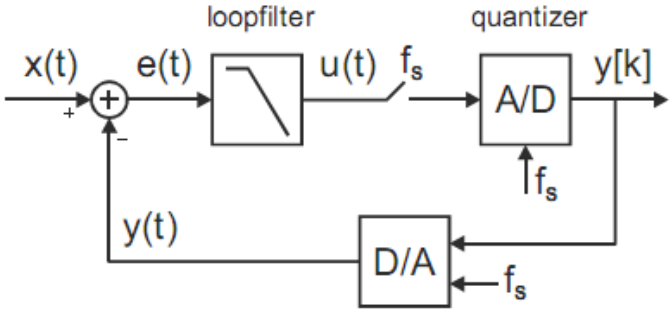


Fig. 2.4. Block diagram of a continuous time delta-sigma converter. [4]

In fact, the main difference between discrete time and continuous time ΣΔ ADCs is - where the sampling is done. In a DT ΣΔ ADC, sampling is done before the Loopfilter. As it can be seen in Fig. 2.4, for CT ΣΔ ADCs, the sampling operation takes place after the loop filter. Therefore, the quantizer input signal is filtered and all the sampling non-idealities inside the signal band are attenuated. This means that the continuous-time loop filter acts as an anti-alias filter. In this case, a CT ΣΔ is a good match for ECS interface.

As explained in the previous chapter, one of the main tasks of the proper ADC for the implemented ECS interface is to suppress the ripples existing on the two channels of input signal due to mixer characteristics. For this reason, a continuous-time delta-sigma ADC could be a better candidate due to its inherent low-pass filtering behaviour. Furthermore, discrete time delta-sigma ADCs have the disadvantage that they need an anti-aliasing pre-filtering circuit. By doing sampling, the high frequency ripples are folded back into the band of interest and increase the noise level, which is not desired. As described above, integrators are the main part of high-resolution ADCs. By looking back at the implemented ECS read-out circuit in Fig. 1.3, it can be seen that by removing the feedback resistors in the TIA stages, they can play the role of integration in the loop filter of the delta-sigma ADC. As a result it is preferable not to have any circuits (such as an anti-aliasing pre-filter) before the ADC so that the available TIA stages can be reused as part of the loop filter of the delta-sigma ADC. In this case, by combining two channels, as described in Fig. 2.1, to carry out the ratio-metric conversion and also to make use of the available TIA stages, not only would there be only one channel instead of two parallel channels (and having two of each component), but also one TIA stage can be omitted, which results in saving 2mW of power.

2.3.2 Second-order delta-sigma ADCs

First-order delta-sigma ADCs are always stable and they have a very simple architecture. On the other hand, they have a much higher tonal behavior for DC inputs. These tones reduce

the desired signal-to noise-ratio (SNR) especially when their frequency is a big division of sampling frequency which results in in-band tonal noises. In addition, to reach the desired resolution, a much higher over-sampling ratio (OSR) is needed. This results in a higher clock frequency and hence higher power consumption. According to the theory, with each doubling of the clock frequency, with a first-order delta-sigma ADC there will be a 9 dB improvement in resolution, while for a second-order delta-sigma ADC the improvement in resolution is 15 dB [2]. Figure 2.5 shows this fact [4]. Furthermore, second-order delta-sigma ADCs are much less sensitive to some circuit non-idealities such as finite gain of the integrators. Second-order delta-sigma ADCs are inherently unstable. However, by defining suitable zeroes and poles in the closed-loop system, the stability can be easily guaranteed. By going from a first-order to a second-order delta-sigma, the allowable input signal range is reduced from 95% to about 75% of the total range, which, however, is not critical in this application. In fact, this input signal range fits best according to this application. The value of each channel can change from 50mv to 400mv in opposite direction. As a result, X+Y=450mv and maximum of X-Y is 350mv which is 77% of the reference.

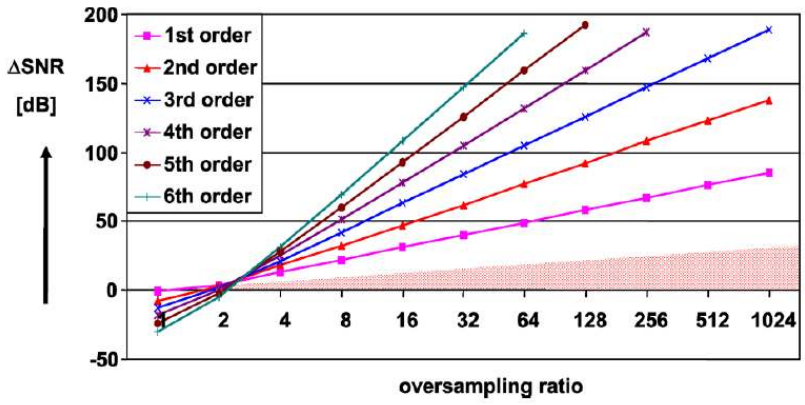


Fig. 2.5. Magnitude of the NTF bode plot of the Nth order CT ΣΔ. [3]

Based on the mentioned advantages of second-order delta-sigma ADC, this type of ADC is chosen in this project. High-order stabilization can be accomplished by means of feedforward, feedback, or any other architecture that allows filter compensation with high-frequency zeros.

2.3.3 FF and FB topologies

As mentioned in the previous section, to stabilize the higher-order ADCs, a zero can be introduced to the loop filter. This can be done by a feedback or a feedforward path. Figure 2.6 shows an ordinary FB second-order delta-sigma ADC.

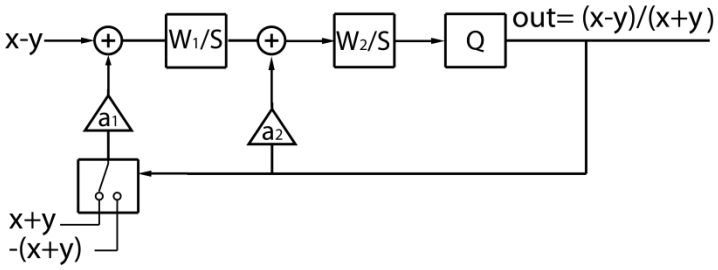


Fig. 2.6. Conventional FB CT ΣΔ ADC.

In this case, by making a path via a2, a zero is introduced. A stronger a2 makes the behavior of the system resemble to first-order behaviour more by bypassing one integrator. This increases the stability, too. The NTF and STF equations are as follows: [9]

$$STF = \frac{\omega_1\omega_2}{s^2 + a_2\omega_2 s + a_1\omega_1\omega_2} \tag{2-2}$$

$$NTF = \frac{s^2}{s^2 + a_2\omega_2 s + a_1\omega_1\omega_2} \tag{2-3}$$

The NTF and STF curves can be seen in Fig. 2.7. As can be seen, the STF displays low-pass filtering behaviour

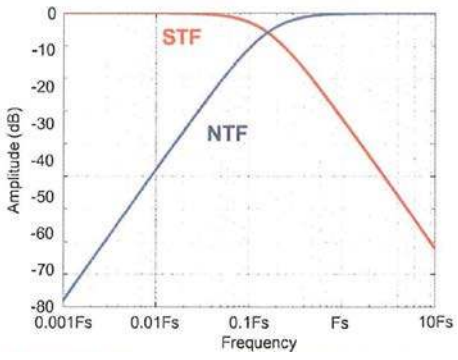


Fig. 2.7. STF and NTF plot of the FB CT ΣΔ ADC.[9]

According to Fig. 2.6, having X-Y as the input signal and choosing (X+Y) or -(X+Y) as the reference, will create an output bitstream which has the information about the ratio ((X-Y)/(X+Y)). This is the desired functionality, however producing (X-Y) and (X+Y) signals from the X and Y outputs of the two available analog channels at the same time in the analog domain is not practical. Fortunately, after a closer look at the input of the first integrator (after the first summation node), it can be concluded that based on the bitstream, which decides whether (X+Y) or –(X+Y) will be added to (X-Y), 2X or -2Y signals will be integrated. As a result, a new structure of the delta-sigma can fulfill our requirement for realizing the (X-Y)/(X+Y) function, which is shown in Fig. 2.8.

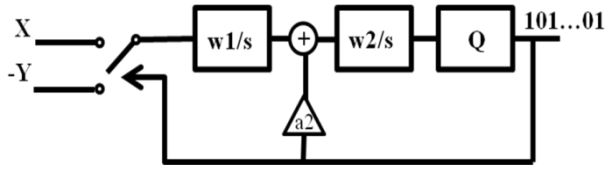


Fig. 2.8. Modified FB CT ΣΔ ADC.

However, this modified FB structure has still not fulfilled the requirements because the (X+Y) and -(X+Y) signals should still be delivered at the second summation node. Fortunately, using a feedforward realization of a second-order delta-sigma converter solves this problem, as shown in Fig. 2.9. There is also another advantage of using FF topology. As shown in Fig. 2.10 in the FF ΣΔ, the output of the first integrator is just noise, while for the FB there is a swing. This will relax the design requirements for the first integrator, which is the most important block. In other words, with a defined output swing, a higher gain (and hence less input-referred noise) can be used in the FF.

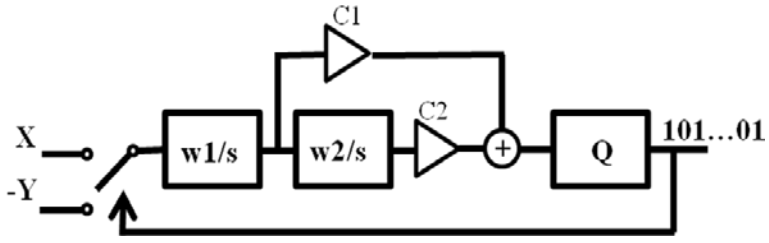
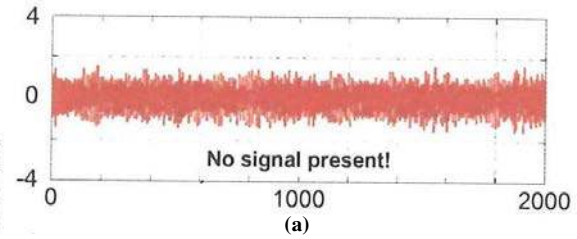
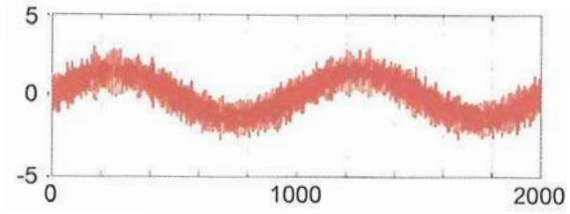


Fig. 2.9. Modified FF CT ΣΔ ADC.



(a)



(b)

Fig. 2.10. (a) Output of the first integrator of the FF; (b) output of the first integrator of the FB [9].

The FF and FB CT $\Sigma\Delta$ have almost the same STF and NTF equations. The only difference between these two is in the order of the STF. The equations for STF and NTF for the FF topology are as follows:

$$STF = \frac{c_1\omega_1 s + c_2\omega_1\omega_2}{s^2 + c_1\omega_1 s + c_2\omega_1\omega_2} \tag{2-4}$$

$$NTF = \frac{s^2}{s^2 + c_1\omega_1 s + c_2\omega_1\omega_2} \tag{2-5}$$

The zero in the transfer function of the signal reduces the slope of the STF from second order to first order, which is shown in Fig. 2.11. [9]

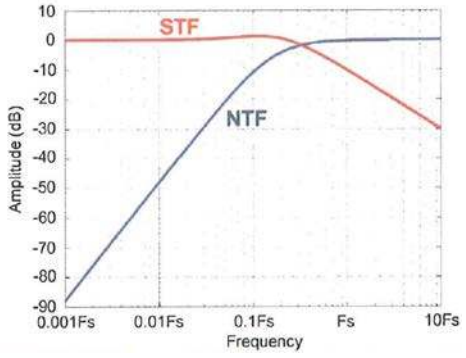


Fig. 2.11. Signal transfer function and noise transfer function of the feedforward continuous time ΣΔ ADC.[9]

2.4 Final topology and simulation results

Figure 2.12 shows the proposed ADC, which is based on the discussion in this chapter. By choosing f_s=1.25MHz (OSR=312), and closed-loop unity frequencies ω_1=100 KHz and ω_2 = 40 kHz for the first and second integrator, respectively, we have a stable second-order, feedforward, continuous time, delta-sigma ADC. The unity-frequencies are defined by G_m/C_1 and $1/(R_2C_2)$. As discussed above, there are ripples present at the outputs of the TIAs due to the mixers (40 MHz) and the chopping frequency of the TIA stages (150 kHz), which should be suppressed. These ripples exist on both channels. Hence, they are present in the input signal and the reference signal of the delta-sigma converter. They are removed by deriving the ADC clock frequency from the frequency of the front-end oscillator by using a frequency divider. In this case, a notch will appear at 40 MHz and 150 kHz, where the ripples exist. As can be seen in Fig. 2.12, the TIA stages are removed from the analog interface. They are replaced by the first integrator of the delta-sigma converter.

It should also be noted that the coupling capacitors C_{cp} (Fig. 1.3), which were placed to prevent the up-conversion of the DC current at the output of the G_{mt} stage (and in this way producing ripples), were not included in Fig. 2.13. This is because these capacitors block the DC path to the input of the sigma-delta converter, and as a result the input common mode of the first integrator is not set. This was not important for the TIA stage of the analog interface, as there was a resistor parallel to the capacitor in its feedback (see Fig. 1.3). Of course, by removing C_{cp}, the amplitude of the ripples at 40 MHz increases. However, this is negligible due to both the inherent pre-filtering of the CT delta-sigma ADCs and also the notch made at this frequency by synchronizing the ADC and the front-end oscillator.

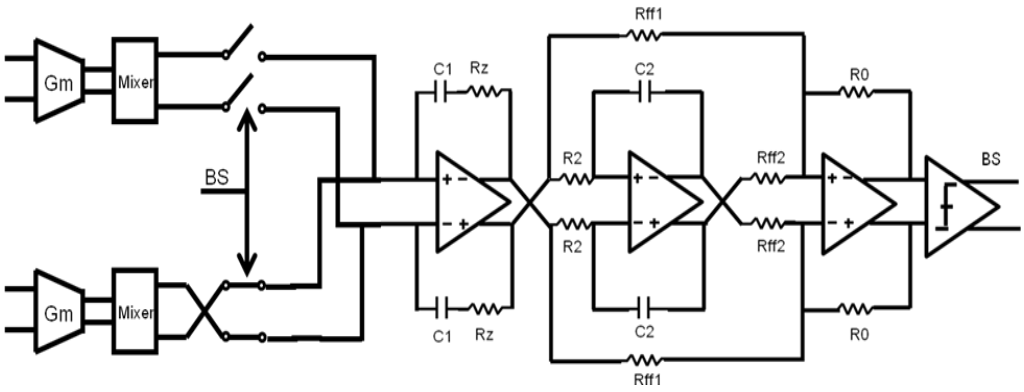


Fig. 2.12. Proposed FF CT ΣΔ ADC.

2.5 Summary

In this chapter, the different types of ADCs were studied which could be good candidates for the ECS read-out circuit based on the requirements and defined specifications. First, based on the resolution and the bandwidth of the input signal, two types of ADCs: dual slope and delta-sigma, were proposed. Dual slope ADCs have some disadvantages such as obtaining two input signal values at different times and hence reducing the advantage of the ratio-metric function, resulting in a high frequency sampling, etc. Therefore, the second proposed delta-sigma ADC was studied. The concept of oversampling and noise shaping, which are the main factors of the delta-sigma principle, was also explained. Finally, after studying the different topologies of delta-sigma ADCs, a well-matched ratio-metric second-order feedforward continuous time delta sigma ADC was proposed as an ECS read-out circuit. Based on the required resolution and according to Fig. 2.5, a sampling frequency was chosen of 1.25 MHz, which is derived from the 20 MHz front-end oscillator frequency, to synchronize the ADC with the interface. In this way a notching out of the existing ripples on the input signal, due to the mixers, is achieved.

In the next chapter, the circuit design of each block and some other non-idealities in the circuit, which reduce the performance of the system and the solution for it, will be discussed.

Chapter 3.

Design of the proposed ratio-metric ADC

3.1 First integrator

The most critical part of designing the second order delta-sigma ADC is the first integrator. The thermal noise of the system, effect of offset, effect of finite gain, and many other non-idealities are defined by the first stage. In other words, the non-idealities of the other stages, for example the second integrator or the comparator, are divided by the gain of the first integrator, which significantly relaxes the design requirements of these stages.

As explained in the previous chapters, the operational amplifier used as the first integrator of the delta-sigma ADC loop filter is in fact the TIA stage already available in the ECS interface [1]. Figure 3.1 repeats the topology of this circuit, which was already shown in Fig. 1.8.

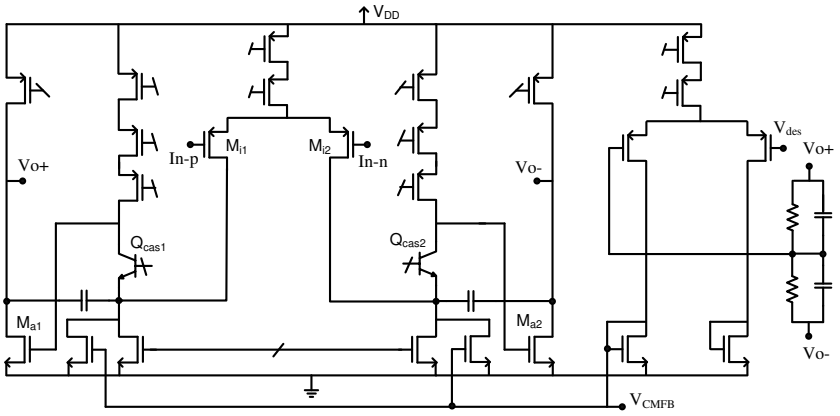


Fig. 3.1. Circuit diagram of the amplifier employed in the TIA stages [1].

The TIA stages are realized by a two-stage cascode-compensated operational amplifier, which is shown in Fig. 3.1 [1]. By using the two-stage architecture, enough gain is provided such that the amplifier gain error can be considered negligible. These conditions can also facilitate implementation of the CMFB circuit by using a passive resistive divider readily, while still satisfying the desired gain. Moreover, this architecture helps to use a resistive

feedforward path to have a second order delta-sigma modulator, because it can still maintain the gain with a resistive load. To keep the amplifier active at the ripple frequency of about 40 MHz (i.e. 2 times the oscillation frequency), its unity-gain frequency was chosen above this frequency. In order to improve the bandwidth while maintaining the phase margin of the amplifier in a two-stage cascode-compensated amplifier, it is necessary to have [1]:

$$g_{m,cas}\beta g_{m,cas} >> g_{m,i}, \tag{3-1}$$

where $g_{m,cas}$ and $g_{m,i}$ are the transconductances of the cascode and the input transistors, respectively, and β is the feedback factor, which is ~1 here. BJTs at the same biasing current can provide a transconductance that is several times higher. As a result, choosing a BJT cascode efficiently satisfies expression (3-1). It should be mentioned that the output impedance of the BJTs in the employed technology is also about 10 times larger than a counterpart MOS transistor. As a result, three PMOS devices are stacked in the first stage to create an equal output impedance compared to the BJTs, therefore maintaining the voltage gain. As seen in Fig. 3.1, the common-mode level is determined by a single loop. This single loop compares the average output voltage with the desired value, which is usually 1/2 V_{DD}. The difference between these two values is fed back to the tail current sources of the first stage to produce a negative feedback, and finally in ideal circumstances to make these two voltages equal. Based on simulation results, the unity gain frequency of the OTA is about 55 MHz with a phase margin of more than 55° at a load of 10 pF. The amplifier gain is about 90 dB at 1 kHz (and is above 120 dB around DC), and its power consumption is approximately 1.8 mW.

TIA stage noise

The noise of the amplifiers in the TIA stages $v_{ampi,n}$ is amplified due to the presence of a quasi-static resistor at their inputs. Fig. 3.2(a) shows the TIA stage in the presence of the parasitic components. To investigate the effect of the TIA offset (as well as *1/f* noise), the offset can be separated into v_{nz} and $-v_{nz}$ during the switching operation, as depicted in the simplified model in Fig. 3.2(a). When S_{n1} is on, the capacitor C_p is charged to:

$$Q_x = C_p v_{nz}. \tag{3-2}$$

And when the bottom switch is on, it is charged to:

$$Q_y = -C_p v_{nz}. \tag{3-3}$$

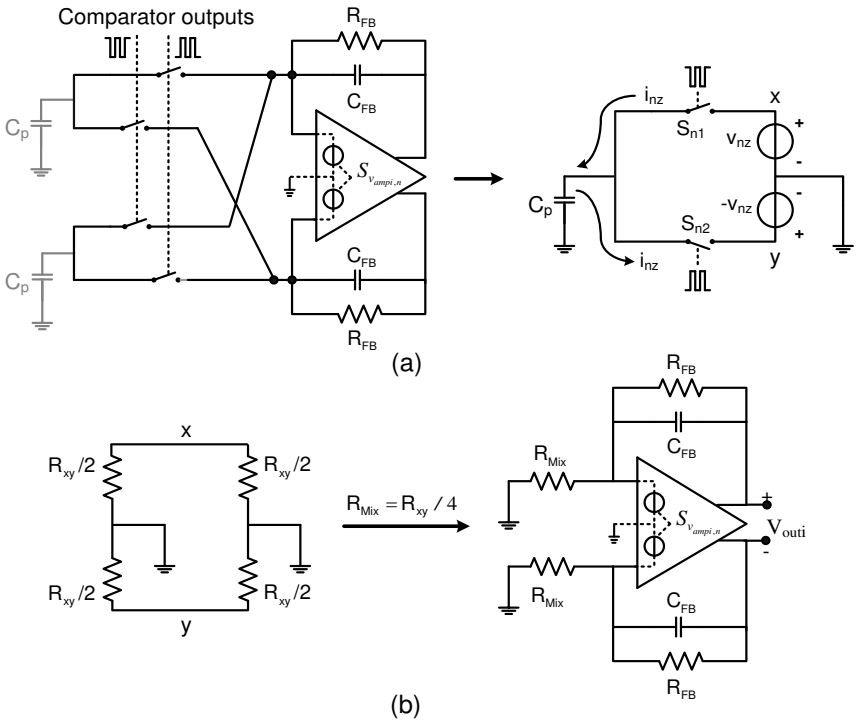


Fig. 3.2. (a) TIA stage in the presence of the parasitic switched-capacitor network; (b) equivalent circuit for modelling TIA stage noise behaviour [1].

Consequently, a change in the charge of C_p appears. Therefore, we can assume that C_p transfers a certain amount of charge between the nodes x and y, which is given by:

$$Q_{xy} = 2C_p v_{nz} = I_{xy} T_{osc} . \tag{3-4}$$

In expression (3-4), I_{xy} represents the average current transferred by C_p from node x to node y during one clock period. As a result, between nodes x and y an equivalent resistor appears, which can be calculated from:

$$R_{xy} = \frac{v_{xy}}{i_{xy}} = \frac{2v_{nz}}{2C_p f_{osc} v_{nz}} = \frac{1}{C_p f_{osc}} . \tag{3-5}$$

Since the circuit is differential, one more R_{xy} appears in the circuit model, as illustrated in Fig. 3.2(b). Accordingly, the resistor R_{Mix} shown in the equivalent circuit is obtained from:

$$R_{Mix} = \frac{1}{4C_p f_{osc}} . \tag{3-6}$$

As a result, the output referred offset is given by:

$$v_{out,offset} = \left(1 + \frac{R_{FB}}{R_{Mix}}\right) \cdot v_{offset} = a_n \cdot v_{offset} \tag{3-7}$$

where v_{offset} is the input-referred offset of the amplifier, and a_n is the noise gain. Likewise, the output-referred noise of the TIA stage can be computed from:

$$S_{V_{ampi,out,n}} = 2\left(1 + \frac{R_{FB}}{R_{Mix}}\right)^2 \cdot S_{V_{ampi,n}}, \tag{3-8}$$

where $S_{V_{ampi,n}}$ is the single-ended input-referred noise power density of the amplifier. Fig. 3.3 shows the flicker noise and the corner frequency at 100 Hz.

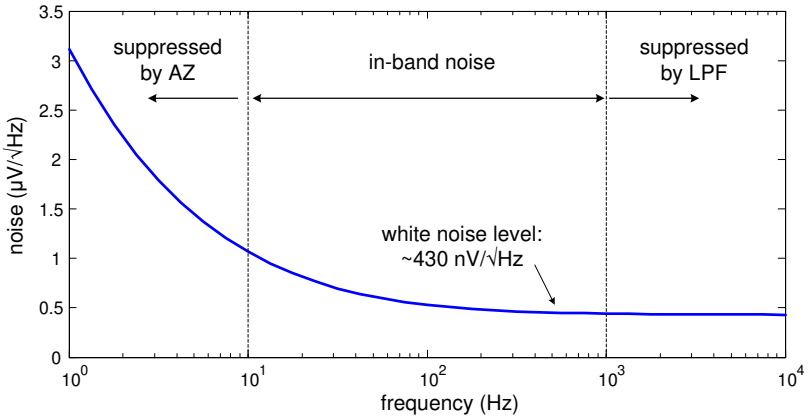
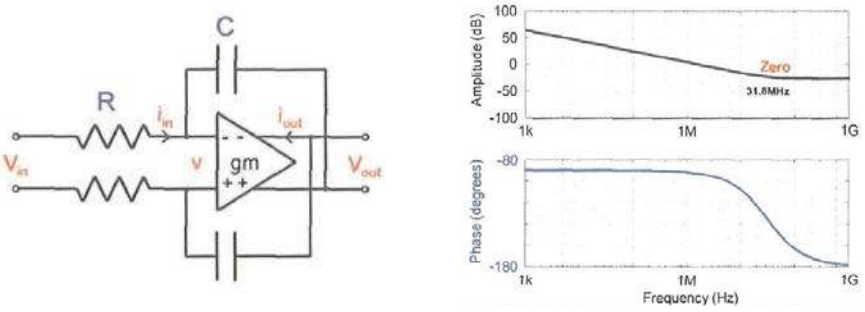


Fig. 3.3. Simulated demodulator noise [1].

3.1.1 Effect of limited gain of the integrator on the total operation

As mentioned in the previous chapter, to ensure a stable modulator with an optimum zero and poles, by means of MATLAB simulations, ω_1=100 KHz and ω_2=40 KHz were chosen. ω_1 is realized by multiplying the Gm and the integration cap. By choosing a value of 80 pF for the capacitor and 200 mS for the Gm, which are already designed and realized in the Nabavi circuit, based on the MATLAB simulations, a 4V p-p output swing is needed for the first integrator. The condition which fulfils this swing requirement is provided by a two stage topology, as is shown in Fig. 3.1.

Furthermore, finite gain has an effect on the desired SNR. According to MATLAB simulations, to reach a 16-bit resolution, a gain of at least 60dB is needed for this opamp. This requirement is fulfilled with a DC gain higher than 100dB. However, as shown Fig. 3.4, due to the finite gain of the OpAmp, the RC integrator has a right half-plane zero.



(a) (b)

Fig. 3.4. (a)RC integrator; (b) bode plot [9].

This zero can be cancelled out by means of a series resistor with the integrator capacitor. The place of this zero and the value of compensation resistor are as follows:

$$i_{in} = \frac{V_{in} - v}{2R}$$

$$i_{out} = -g_m . v$$

$$i_{in} + i_{out} = 0 \qquad (3\text{-}9)$$

$$-V_{out} - v = \frac{2}{sC} i_{out}$$

$$\frac{V_{out}}{V_{in}} = \frac{-sC + 2g_m}{sC(1 + 2g_m R)} \approx \frac{\omega_u}{s\left(1 - \frac{sC}{2g_m}\right)}.$$

By adding a series resistance to the integration capacitor the equation becomes:

$$\frac{V_{out}}{V_{in}} = \frac{2g_m + (2g_m R_z - 1)sC}{sC(1 + 2g_m R)} \approx \frac{\omega_u}{s\left(1 - \frac{(2g_m R_z - 1)sC}{2g_m}\right)} . \qquad (3\text{-}10)$$

By choosing Rz=1/(2g_m), the zero is cancelled out. In practice, the integrator is loaded by the feedforward resistors, resulting in a finite DC gain and also one pole located at $\omega_1 = \frac{1}{2g_m R_L RC}$. This is shown in Fig. 3.5. As long as we have a high DC gain value, this loading effect will have no significant effect on the functionality of the ADC. As mentioned above, this block consumes 2mw.

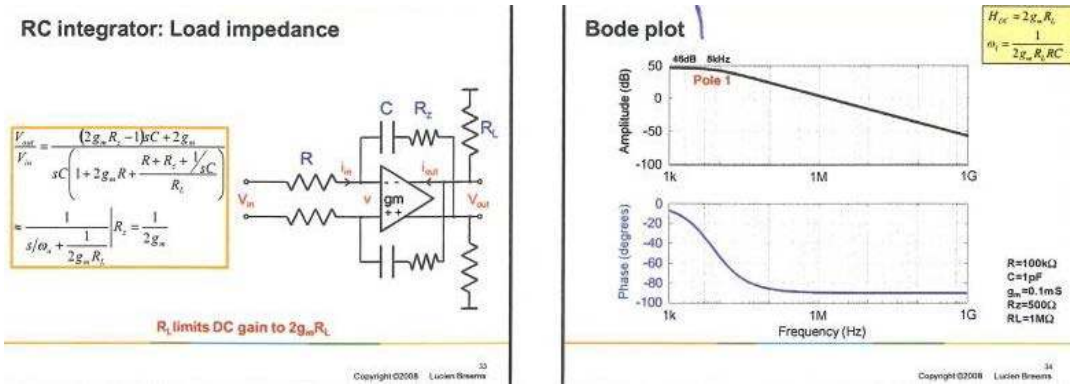


Fig. 3.5. Effect of the resistive load on the diagram bode [9].

3.1.2 Effect of offset

The error at the input of the first integrator should not be more than 1 LSB. As a result, the maximum allowed offset for the input referred is:

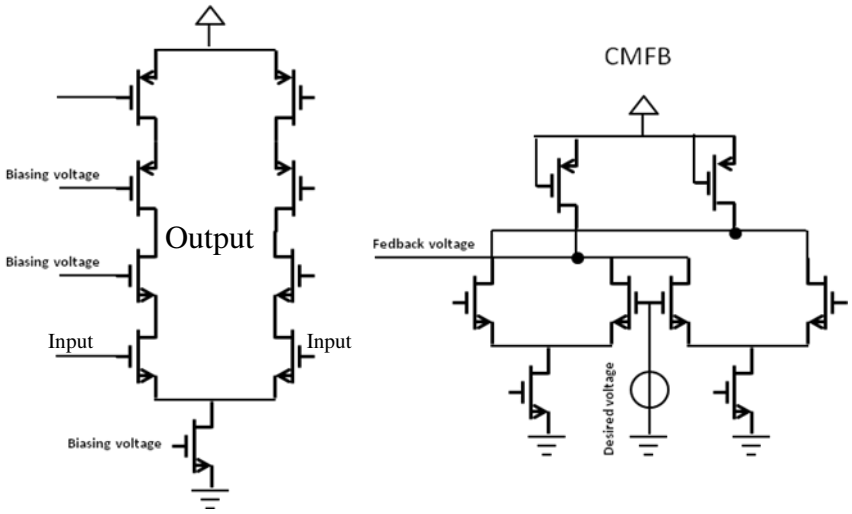
$$e < \frac{\frac{4}{\pi} \times \frac{300mv}{5k\Omega}}{2^{16}} \times Rmix = 10\mu v \quad . \tag{3-11}$$

R_{mix}, as described in chapter one, is a virtual resistor because of the existence of the parasitic caps and the switching of them. This allowed offset value is obtained after chopping the OpAmp based on a Monte Carlo simulation.

3.2 Second integrator

As explained in the previous section, since errors introduced by the second integrator are attenuated by the gain of the first integrator, no offset cancellation is needed. In this case, because of ω_2=40 KHz, which is realized by the RC, a 20pf cap and 200 KΩ for the resistor were chosen. Based on MATLAB modeling, the required swing is 2V p-p. As a result, a simple telescopic structure is used for this stage, which is shown in Fig. 3.6. The simulation results for the minimum gain for this stage according to MATLAB modelling shows that a minimum 40 dB DC gain is needed.

Telescopic architecture



(a) (b)

Fig. 3.6. (a) Circuit diagram of the second integrator; (b) CMFB circuit.

According to Fig. 3.7, the DC gain of this stage is above this value. The final SNR is obtained based on this formula:

$$\frac{S}{N} = 10\log\left(\frac{1}{1/\frac{S}{N_{qt}} + 1/\frac{S}{N_{th}} + 1/\frac{S}{N_{jitter}}}\right) . \quad (3\text{-}12)$$

Where, N_{qt} is the quantization noise, N_{th} corresponds to thermal noise and finally N_{Jitter} is the clock jitter noise. The thermal noise of the system, which is defined by the Gm stage in the interface, is 54nv/$\sqrt{Hz}$. In this case the SNR for the thermal noise is 96dB. According to the chosen OSR, the quantization noise is also 107dB, as was shown in the simulation results in the previous chapter. The SNR of the jitter will also be calculated in this way:

$$\frac{S}{N_{jitter}} = 10\log\left(\frac{OSR}{8f_s^2.\sigma_s^2}\right) = 108\ dB \quad . \quad (3\text{-}13)$$

in which OSR is the over sampling ratio, fs is the sampling frequency, and σ_s is the uncertainty in the sampling clock. The total SNR then is 96.1 dB.

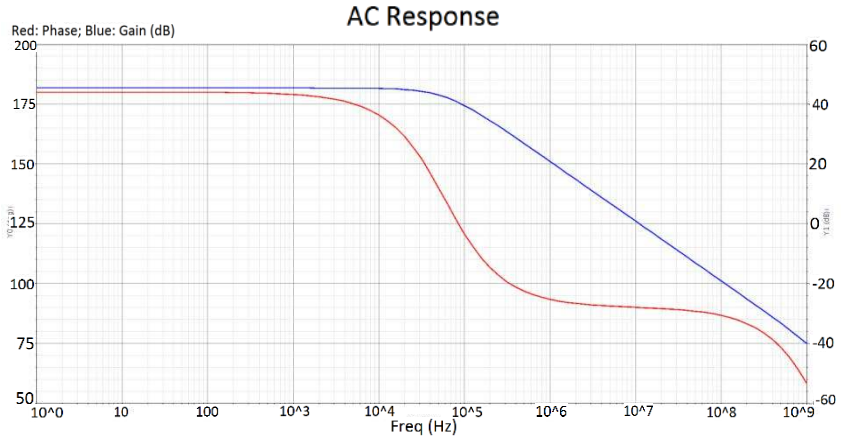


Fig. 3.7. Frequncy response of the second integrator.

3.3 Comparator

The comparator is implemented as a dynamic latch proceeded by a preamp, which prevents kickback to the output of the summation block. Figure 3.8 shows the circuit diagram of the comparator. [10]

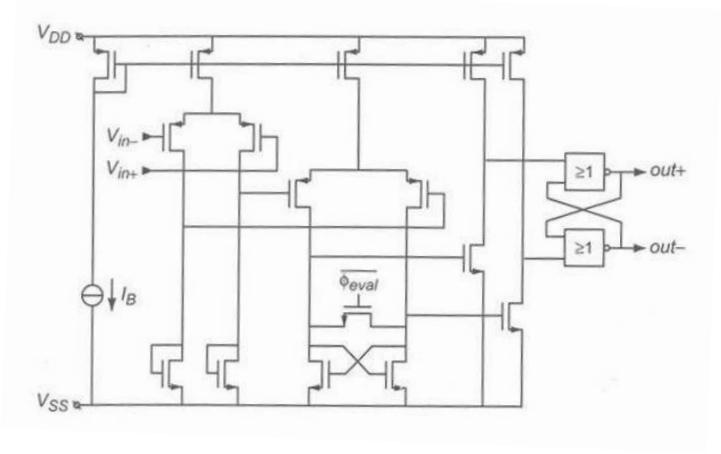


Fig. 3.8. Circuit diagram of the latched comparator [10].

3.4 Necessity of synchronized clock

As mentioned above, due to the existence of the mixers after the Gm stages, some ripples are introduced to the input of the delta-sigma ADC. These ripples are placed at the 40MHz which is two times the oscillator frequency. In addition, there is also another source of error located at the 156.25 KHz (division of 20MHz) which is due to the chopping of the TIA stage. These errors directly have an effect on the achieved SNR and reduce this value. This problem is solved by using the oscillator to synchronize the clock of the ADC. Hence the clock of the ADC is built by division blocks which divide the 20MHz oscillator frequency

into 1.25MHz. As a result, in the frequency domain a notch is produced at the mentioned frequencies to filter them out. This synchronization is more important in the new design because the decoupling capacitors after the Gm stages are removed, which prevents the up-conversion of the DC errors of the Gm stages. This is done to provide the input common mode voltage of the TIA stage by the output CMFB of the Gm stages.

3.5 Bit stream-controlled chopping

As described above, there are two ripples on the input signal and reference signal. The ripple which occurs at 40 MHz is suppressed by the inherent filtering of the continuous time delta-sigma ADC, and also by the clock synchronization of the ADC with the interface. However, the main problem with the ripples caused by the chopping is that they may be correlated with the bitstream of the modulator, and will be modulated back to the DC when multiplied by that bitstream. One solution to prevent this problem is to use "bit-stream controlled chopping". This method is similar to the method which is used in [10] for DEM with the difference that here it is used for chopping.

Figure 3.11 shows the effect of applying bs-controlled chopping in the MATLAB modelling of the system. As it is depicted, by using this method the noise floor drops about 20dB, which is a considerable value. The ripples on the reference voltage where chosen for 10mv which is close to real values.

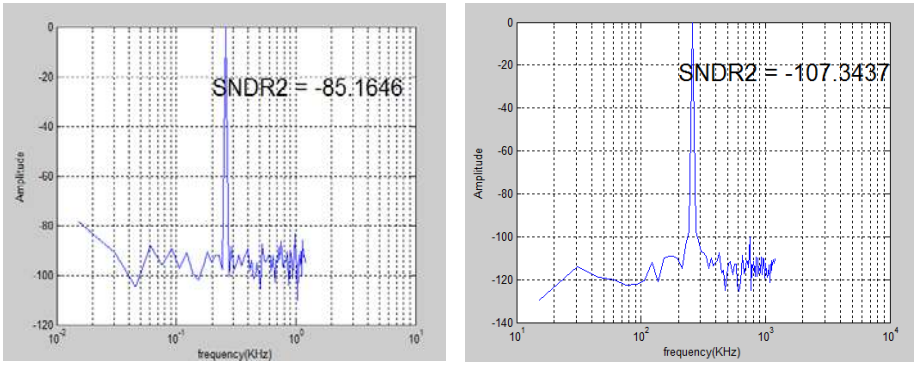


Fig. 3.11. (a) Noise spectrum before bs-controlled chopping; (b) after bs-controlled chopping.

3.6 Decimation filter

The decimation filter is the last part of the delta-sigma ADC. In fact, the delta-sigma ADC is realized by combining the delta-sigma modulator and the decimation filter. There are various types of digital filters that can be used. Some of these filters are shown in Fig. 3.12. As can be seen, the rectangular decimation filter provides less high-frequency noise

suppression but narrower bandwidth, while the Kaiser filter suppresses the high frequency noise very well, but the first notch is at higher frequency compared to other decimation filters. In conclusion, the decimation filter has been chosen based on the application that will be used. As a result, to ensure both good suppression of high frequency noise and a sufficiently narrow bandwidth, a suitable decimation filter should be chosen. It should also be mentioned that the decimation filter should be synchronized with the clock of interface. In this specific application, because of both: the slope of 40dB resulting from a second order delta-sigma and the 1KHz bandwidth, the desired decimation filter should also have the same bandwidth and a higher falling slope. To achieve the desired SNR, the decimation filter which is used is a Hanning filter with a length of 512. With this length, this filter would have a first pole at 2KHz, which defines the first pole of the whole system, too. Using 512 as the length means a conversion time of about 410μs . To reduce this time it is possible to use overlapping windowing. The decimation filter in this project is done offline by MATLAB coding.

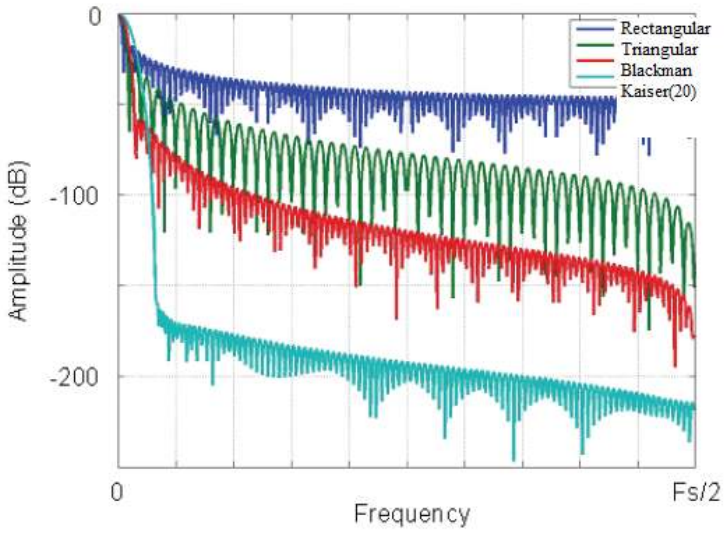


Fig. 3.12. Examples of some decimation filters [11].

Figure 3.13 shows the Hanning window in both the time and frequency domains for the length of 512.

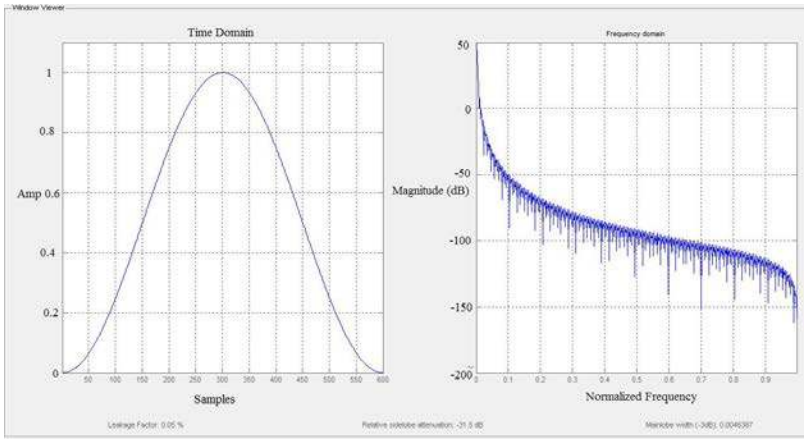


Fig. 3.13. Time and frequency domain of the chosen Hanning window.

3.7 Post layout simulation results of the ADC

Figures 3.14 and 3.15 show the final post-layout simulation results. In this case, the input signal is chosen at an arbitrary frequency in the bandwidth. The slope of the 40dB/decade is clearly shown in Fig. 3.14. The achieved SNR is about 101 dB. The total harmonic distortion of the ADC is also more than 14 bits, which is much better than the sensor distortion, meaning the ADC is not the limiting block.

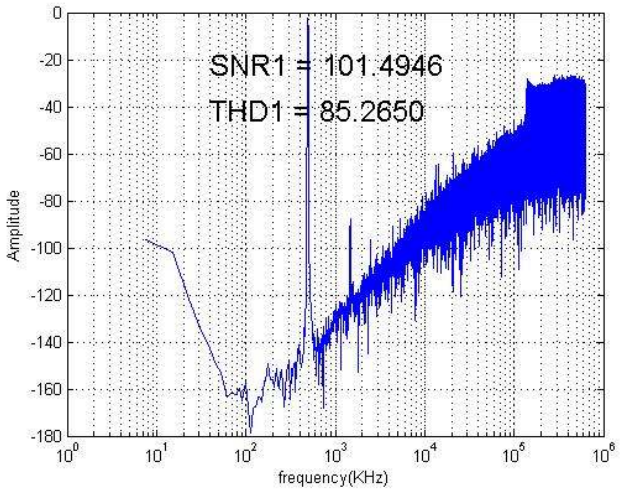


Fig. 3.14. Final simulation results of the output decimated bs.

3.8 Summary

In this chapter the design of each block in the block diagram discussed in the previous chapters was explained. The importance of the first integrator and the effect of the non-idealities of this stage, such as finite gain, offset, effect of resistive loading, etc., were

discussed. Next, the topology of the second integrator and comparator was shown. It was also explained that because of the suppression of the non-idealities of these stages by the gain of the first integrator, the designs of these stages are much relaxed.

The necessity of synchronizing the ADC with the interface was then discussed. In this way the ripples on the input signals can be notched out. Then it was explained that this synchronization is not good enough to prevent reduction of SNR due to the correlation of these errors with the bitstream. To solve this problem, bitstream-controlled chopping was proposed and explained. Finally the post-layout simulations of the proposed ratio-metric delta-sigma ADC were shown. In the next chapter the measurement results of the chip will be presented.

Chapter 4.

Measurement results

4.1 Block diagram of the measurement setup

The technology used to design this chip is 0.35um BiCMOS. The chip has 48 pins and it is packaged in QFN package. In order to control the designed chip properly, many control signals have been considered during the chip design. These control signals are produced by the FPGA, which is programmed by VHDL code. The most important of these control signals is the one which disables the interface. In this case, the input signals can be provided by off-chip signal sources. Hence, the delta-sigma ADC can be tested separately. In addition, it is possible to close the feedback of the ADC off-chip, meaning that the bitstream can exit the chip (to the FPGA) and then be fed back to the chip by synchronous CLK produced by the FPGA. Important clock signals such as the CLK of the delta-sigma, the evaluation clock of the comparator, and the bitstream-controlled chopping, etc., are also generated by the FPGA. The bitstream with a trigger clock, which is in fact the falling edge of the main clock of the delta-sigma, is sent to a DAQ (Data Acquisition board). The bitstream is captured by the DAQ and then sent to a PC for further data processing such as filtering and decimating in MATLAB. Figure 4.1 shows the block diagram of the measurement set-up. Here is the list of signals which are provided by the FPGA:

- **BS-control**: Defines the delta-sigma feedback as being closed on-chip or off-chip.
- **BS-Chop-control**: Defines the chopping signal as on/off chip.
- **A_MUX, BMUX**: Defines the polarity of the input signals.
- **Reset**: Resets the capacitors at the starting point of the delta-sigma to ensure a good initial charge on the capacitors.
- **CLK-control**: Defines the chip clock as on/off chip.

- **BS-Chop**: The chopping signal which is produced based on the BS-controlled chopping concept. This signal is generated by the FPGA.
- **En, Dis, Out-control**: Enables the interface as input of the delta-sigma and disables the off-chip inputs and vice versa.
- **Eval**: Clock of the delta-sigma comparator.
- **CLK-out**: CLK of the whole delta-sigma (1.25MHz), which is provided by the FPGA.

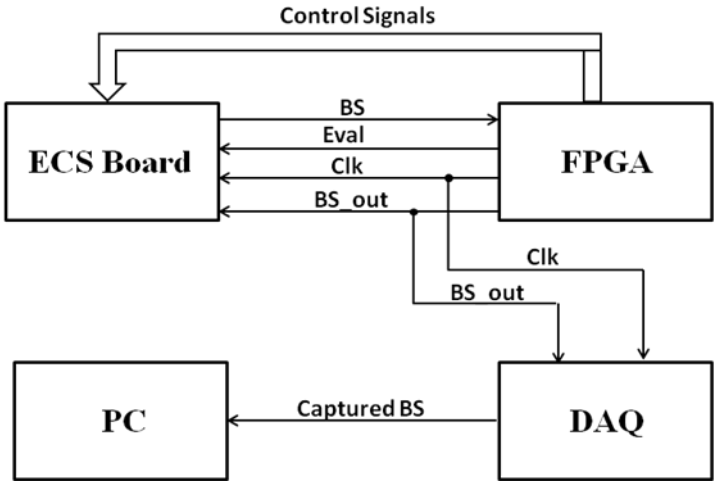


Fig. 4.1. Circuit block diagram of the measurement setup.

Figure 4.2 shows the timing of the generated clock signals by the FPGA. At the rising edge of the CLK, the BS is fed back to the input of the modulator. As is shown, the BS is quite valid at the rising edge of the CLK signal. Therefore this clock is also sent to the DAQ to capture the valid BS. The BS will be updated during the evaluation mode of the comparator, which was discussed in the previous chapter.

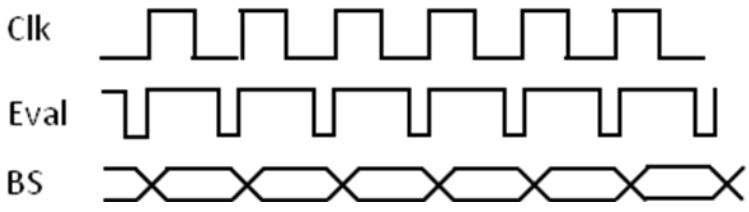


Fig. 4.2. Timing issue of the generated signals.

After preparing the control and clock signals by writing the VHDL code of the FPGA, different tests were done on the chip. At first, the delta-sigma was tested separately by off-chip input signals. The noise shaping behaviour of a second-order delta-sigma is clearly

shown in Fig. 4.3. The achieved SNR according to this test is 108 dB, which is quite good. In this figure red line shows the main tone, green one is the input bandwidth and the blue is the out of band spectrums.

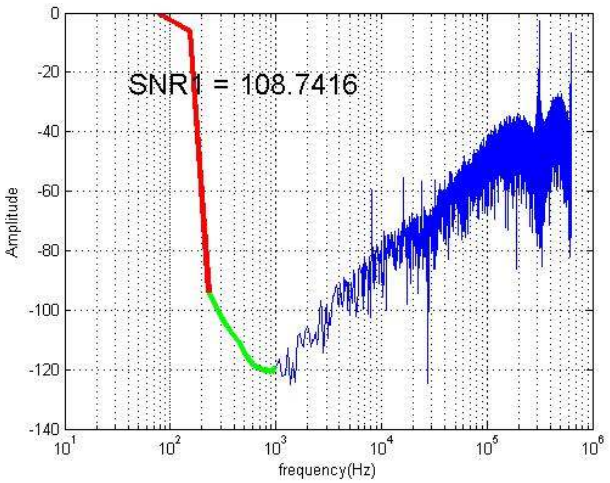


Fig. 4.3. Noise spectrum of ADC with external DC input signals.

In the second measurement the input signal was swept for the whole range to check the linearity of the system. The result is shown in Fig. 4.4. In this graph the red line is the ideal linear curve and the blue line is the output of ADC. The achieved linearity is about -84dB which is good enough and is much more than the total linearity of the system.

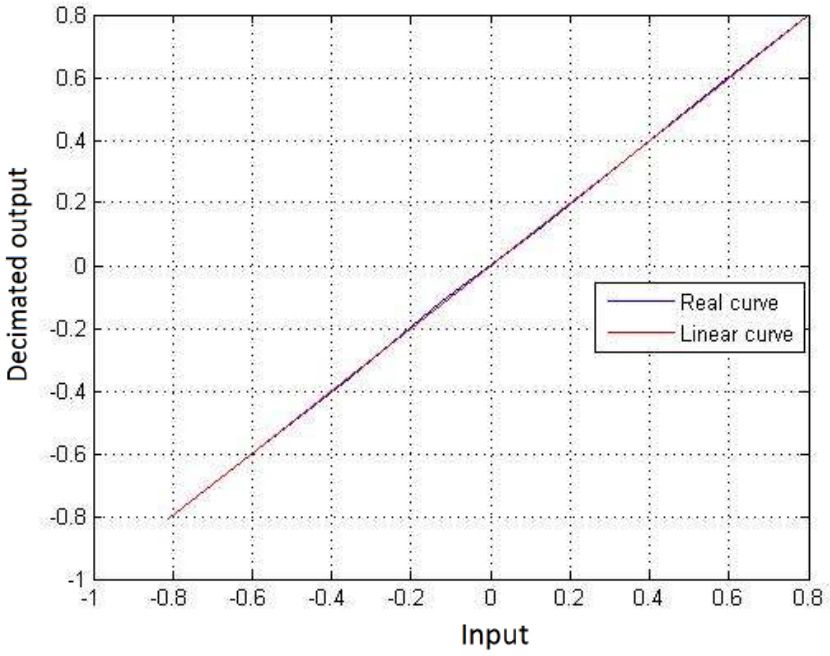


Fig. 4.4. The linearity of ADC with external input signals.

In the second phase of the measurements, the whole chip was tested. In other words, the off-chip input signals were disabled and the input signal of the ADC was provided by the ECS read-out circuit [Nabavi]. In this case, a metal target was installed close to one of the coils and the SNR of the output of ADC was calculated. Figure 4.5 shows the 40dB/dec noise shaping of the ADC and the achieved SNR. As is shown, about 74 dB was achieved in this test. It should be mentioned that this value is not for the full-range of the ADC.

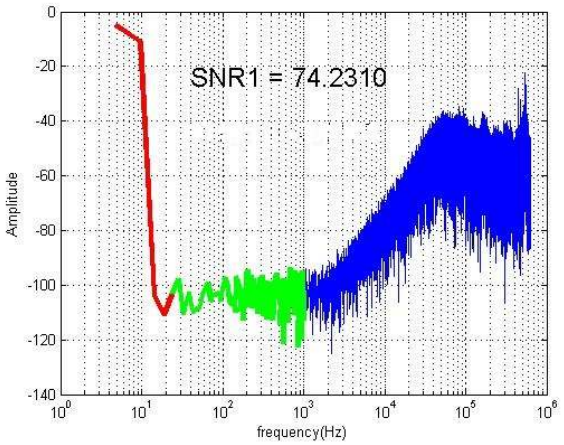


Fig. 4.5. Noise spectrum of the whole displacement sensor.

Figure 4.6 shows the same noise spectrum after the Hanning filter is applied to it.

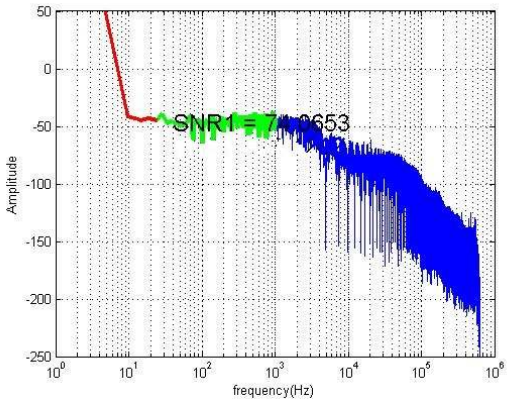


Fig. 4.6. Noise spectrum of the whole displacement sensor with Hannin filtering.

Finally, Figure 4.7 shows the noise level of the output decimated values for interested bandwidth.

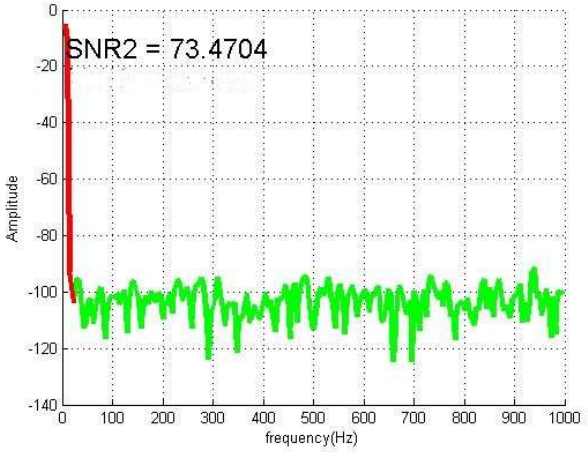


Fig. 4.7. Noise spectrum of the decimated values in the interested bandwidth.

The decimated value related to the position of the metal to the coils was -0.247. The SNR for the full range of the ADC should be calculated as:

$$SNR_{full} = 74 + 20 \log (1.55/0.245) = 74 + 16 = 90\text{dB} . \qquad (4\text{-}1)$$

The 90 dB resolution calculated with 4-1 corresponds to about 15 bits. The input analog signals of the ADC which were produced by the interface had about 94dB SNR. This means that the SNR is about a half a bit below the target. This problem needs to be found and debugged in the future. This value shows that a displacement resolution of about 15 bits has been achieved with the design and proven with the tests in this master's project. It should be mentioned that by adding the on-chip ADC to the system, the total power consumption of the system, as was expected, did not change and was kept at a value of 18mW. Fig. 4.8 shows the final layout of the chip.

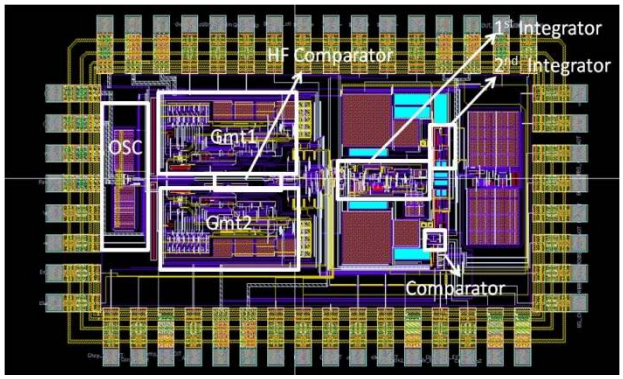


Fig. 4.8. Layout plot of the ECS interface included the analog front-end and ADC.

Chapter 5.

Conclusion and future work

In this project, an eddy current displacement sensor interface with an integrated ADC has been discussed. It employs a continuous-time Delta-Sigma ADC with a feed-forward loop-filter topology, which is well matched to the sensor front-end. It directly provides the desired ratio metric digital output, and is operated synchronously with the front-end to suppress ripple. Power is saved by replacing the trans-impedance amplifiers used in a previous interface [1] by the first integrator of the ADC loop filter. Thus, a digital output is obtained without increasing the overall power consumption of the interface. The remaining area is occupied by capacitors. It was also shown that the measurement results were also quite well matched with the simulation results at system level and also with the post-layout simulations. The final resolution, which was achieved by only the ADC, was about 16.8 bits, and the whole system, which can be named a displacement-to-digital converter, reaches about 15 bits.

In future work, to further qualify this chip, the first step could be to work more on the BS-controlled chopping, which could be the reason for the missing half bit. Secondly, it could be also good to sweep the target and do the linearity test of the whole system. In principle, because the linearity of the ADC was much better than the sensor, which was -60dB, it is expected that the same value will be achieved. Regarding the circuit-level design, some modifications can be made to the first integrator, which has already been used in previous work to reduce the power consumption.

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