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## A Real Time Coincidence System for High Count-Rate TOF or Non-TOF PET Cameras Using Hybrid Method Combining AND-Logic and Time-Mark Technology

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### Abstract

A fully digital FPGA-based high count-rate coincidence system has been developed for TOF (Time of Flight) and non-TOF PET cameras. Using a hybrid of AND-logic and Time-mark technology produced both excellent timing resolution and high processing speed. In this hybrid architecture, every gamma event was synchronized by a 125 MHz system clock and generating a trigger associated with a time-mark given by an 8-bit high-resolution TDC (68.3 ps/bin). AND-logic was applied to the synchronized triggers for the real-time raw sorting of coincident events. An efficient FPGA based Time-mark fine-sort algorithm is used to select all the possible coincidence events within the preset coincidence time window. This FPGA-based coincidence system for a modular PET camera offers reprogrammable flexibility and expandability, so the coincidence system is easily employed, regardless of differences in the scale of the PET camera detector setup. A distributed processing method and pipeline technology were adopted in the design to obtain very high processing speed. In this design, both prompt and time-delayed accidental coincidences are simultaneously processed in real time. The real-time digital coincidence system supports coincidence in 2 to 12 detector module setups, capable of processing 72 million single events per second with no digital data loss and captures multiple-event coincidence for better imaging performance evaluation. The coincidence time window-size and time-offset of each coincidence event pair can be programmed independently in 68.3 ps increments (TDC LSB) during the data acquisition in different applications to optimize the signal-to-noise ratio. The complex coincidence system is integrated in one circuit board with 1.5 Gbps fiber optic interface. We demonstrated the system performance using the actual circuit and Monte Carlo simulations.

### Index Terms

Coincidence; positron emission tomography (PET); real-time; time of flight (TOF); TDC; time-mark

## I. INTRODUCTION

The coincidence electronics is an important part of a Positron Emission Tomography (PET) camera. Usually, there are two methods of achieving coincidence: one is implemented by AND-logic in FPGA [1] or by custom chips [2], and the other is time-mark sorting implemented by on board CPU or by offline software. A traditional AND-logic based engine can achieve real time coincidence but has less flexibility in timing assignment and is

difficult to implement in a Time of Flight (TOF) PET. Nowadays, the TDC has a very high resolution for timing measurement; the time-mark generated by a TDC can also be used in coincidence measurement. But a pure time-mark based coincidence method is complex [3] and a long time-mark [4], [5] increases the complexity when the data is processed in real time. By combining AND-logic and time-mark, we developed a coincidence system that can be used to upgrade our high-resolution oncologic transformable PET (HOTPET) [6], [7] camera to a TOF-PET camera or our new animal Non-TOF PET camera. Processing the gamma events in real time using this hybrid method only requires a short time-mark to identify coincidental gamma events and when count rate was high, it reduces the bandwidth for data transmission compared with the offline process.

## II. METHOD AND SYSTEM DESIGN

### A. Overall Description

As shown in Fig. 1, the coincidence system was designed to be reconfigurable and expandable to handle from 2 to 12 detector modules. This design allows the coincidence electronics to be used in different size-scale PET cameras, such as an animal PET camera, a breast PET camera or a whole-body PET camera.

### B. Two Level Coincidence Architecture

Firstly, we use a 125-MHz system clock to synchronize the analog trigger signals from the gamma events to the system clock synchronized triggers. Secondly, TDCs measure the time difference between the analog trigger signal and the clock synchronized trigger (see Fig. 2) in 68.3 ps/bin time resolution. Since the TDC output generated from different detector modules may have different scales and start points, the TDC time-marks from different modules are corrected and normalized by lookup tables. These corrected TDC outputs are called the time-marks. The analog trigger generates a combination of a clock-synchronized trigger and a time-mark.

The 2-level coincidence architecture is used in this study. The first level coincidence is an AND-logic gate that pre-sorts coincidence pairs from the system clock-synchronized triggers coming from the different modules within 2 clock cycles. Like a snapshot, it collects all possible coincidence pair combinations. In a 12-detector-module coincidence system, each detector module looks for coincidences with seven opposite detector modules, so there are 42 detector-module pair combinations. The AND-logic gate generates a 42-bit combination code to indicate which pairs were qualified for the further fine sort. It also generates the raw code to indicate the raw timing. The time-mark difference range and the raw code between two modules produce four cases, (See Fig. 2), as described in Table I.

The second level coincidence uses the raw code and time-mark to derive the difference between 2 single events and obtain the coincidences within time window  $W$ .

### C. System Diagram of Coincidence System

Fig. 3 is the diagram of the coincidence system, which is composed of a prompt coincidence unit, a random coincidence unit, and some peripheral units such as command/control and data transmission units. The command/control unit decodes the command (such as size of the coincidence window) sent from the computer and sets the operating configuration. The data transmission unit arranges coincidence results and sends them to the computer through a fiber optic interface. Between these 2 level coincidences, FIFOs are used to buffer the first coincidence results to reduce the dead time.

In the prompt coincidence unit, data from TDC board included clock-synchronized trigger, time-mark, energy and location information for every event. After the first level AND-logic coincidence filtering, if the digitalized triggers are within two clock cycles, the corresponding combination code bit which is used as an enable flag in the second level sorting is set to 1, otherwise is 0. A 12 to 42 structure arranges all qualified event pairs and distributes them to 42  $128 \times 64$  deep raw data FIFOs. There are 42 64-bit outputs for 42 possible coincidence combinations. Each output included coincidence pair ID, energies, position information, TDC codes for these two single gamma events and the raw timing information between them (in one clock cycle or in two adjacent clock cycles).

There are 42 parallel processing cells to realize the second level time-mark sorting at the same time. They read data from these raw FIFOs and finish the fine time discrimination with pre-set coincidence time window parameters. Pairs of events inside each cell may require processing in every clock, but the fine discrimination may not be completed within one clock cycle. To avoid data loss in these instances, we designed a pipeline. The data path of fine discrimination is cut into several partitions to fit the system clock speed. Every event pair qualified by the second level coincidence is packaged to a 64-bit coincidence result and stored in a  $128 \times 64$  deep second level coincidence result FIFO. The readout logic reads data from these 42 second-level coincidence FIFOs in turn and buffers the data; an  $8 \text{ k} \times 64$  deep FIFO is used to prevent digital data loss.

When the system clock is set at 125 MHz, because the 9-bit TDC time-mark and the raw rode can only cover two clock cycles, the maximum window size is 16 ns. When a slower system clock is used with a longer TDC time-mark, the maximum window size will increase, but it will cost more FPGA logic resources in the TDC implementation.

#### D. Random Coincidence and Multiple Coincidence

There are several basic methods [8] for random background estimation in the coincidence data acquisition. Compared with the profile distribution method and countrate method, the delay method is easy to implement in real-time in a hardware circuit. In this project, the delay method is used in the random coincidence estimation.

In the random coincidence unit, before the first level AND-logic coincidence, each module has a digital programmable shift time-delay driven by the system clock for acquiring random coincidences. The events picked up from the coincidences of these delayed triggers are regarded as random coincidence events. The delays are implemented with RAM-based shift registers [9] which are driven by the system clock. The delays for each module is set to  $16 \times (N + 1)$  clock cycles ( $N$  is the module number from 0 to 11). After the delays, the random coincidence unit has the same structure as the prompt coincidence unit.

In this system, multiple-coincidence acquisition is optional. Since we use *snapshot* in the first level coincidence and all possible combinations are sent to the second level coincidence for sorting in parallel, all possible coincidence pairs are recorded if the multiple coincidence flag register is set, otherwise, only two events coincidence will be recorded.

#### E. Circuit Board Design

The coincidence main functions were implemented in an Altera Cyclone III CY3C80F780C6 [10] low-cost field programmable gate array (FPGA) and the whole system was integrated in an 8 inch  $\times$  10 inch 10-layer PCB board. Totally, the FPGA logic consumption is logic element 66%, on chip memory 94% and I/O pin 89%. The 125 MHz LVPECL system clock is provided by a clock distribution board, which also provides clocks to the TDC boards for synchronization (Fig. 1). The clock delay can be adjusted in 10-ps

steps. In the system design, the 2.5 V low-voltage logic level is widely used to reduce power consumption.

As can be seen in Fig. 4, there are 12 input connectors for up to a 12 detector-modules PET camera setup. A 1.5 Gbps HOTLink II [11] fiber optic interface is used for the high speed data transmission. A USB2.0 and a RS232 interface are used for command download and debugging.

## F. Performance Evaluation

GATE (the Geant4 Application for Emission Tomography) [12] Monte Carlo simulation is now widely used in PET detector simulations [13]–[15]. Using data generated from GATE simulation instead of using the real data from detector is more convenient for evaluation of the electronics system in different detector and phantom setups, especially in the system design period.

Since the coincidence input data from GATE simulation can also be processed offline, it gives a good reference to evaluate the performance (such as data loss, FWHM, etc.) of the hardware coincidence system, such as data loss.

To evaluate the performance of the TOF-coincidence system for a brain-PET camera imaging a brain phantom, we used GATE to model the PET detectors and the phantom, and to generate locations and times of gamma events. Fig. 5 illustrates the GATE simulation models of the brain PET detector and gives an expanded view of the module, block and crystal arrangement.

Table II shows the parameter details of the GATE simulation. The energy window used in the GATE events generation is 340 to 750 keV, and the energy resolution is 20%. The simulation output includes the time, module number, crystal location, and energy of each single event. Fig. 6 illustrates an energy spectrum of the simulation result. From this spectrum, a scatter factor of 0.46 can be derived.

The times of GATE simulation gamma events are sampled by a 125 MHz system clock to generate clock-synchronized triggers. The time-mark is the digitization of the time difference between one gamma event and one clock-synchronized trigger. The time-mark has a time-resolution of 68.3 ps/bin. This timing digitization has a 2-clock-cycle dead time. The 68.3 ps/bin resolution was measured from the TDC performance evaluation. The TDC outputs were downloaded to the coincidence system for coincidence evaluation. In this test, the delays for random coincidence were set from 128 ns to 1536 ns with 128 ns difference between adjacent modules.

## III. RESULTS AND DISCUSSION

### A. Count Rate

The coincidence system was tested in the data acquisition mode as if it was in a PET camera but the input data were generated from the GATE simulations. We downloaded the simulated data of different PET camera operating conditions to the coincidence system board (dose, coincidence time window size and multiples rejection) and compared the coincidence results with the ideal coincidence results that were directly derived from offline-sorting of the original GATE simulation data.

Fig. 7 illustrates the random coincidence count rates as a function of dose with and without rejection of multiples, for a 6-ns coincidence time window. Two observations can be made: (a) the coincidence hardware random rate closely followed the ideal rate for the whole dose

range when there is no multiple rejection, and (b) as the dose increased, the rejection of multiple coincidences caused the measured random count rate to drop significantly (i.e., larger error in random estimation). Fig. 8 illustrates the total or prompt coincidence count rate (true + scatter + random) as a function of dose with and without multiple rejection, and Fig. 9 shows the true + scatter coincidence count rate as functions of dose with and without multiples rejection. The rejection of multiples also caused reductions in both the total coincidence rate and the true + scatter rate to drop more from ideal as dose increased.

Figs. 8 and 9 indicate that, if a 15% coincidence error in the true + scatter data is accepted, this TOF-coincidence hardware can process 5 mCi of activity contained totally within the axial field of view (AFOV) with a total coincidence rate of  $7 \times 10^6$  coincidences/sec, which exceeds the processing requirement for most clinical applications. At this rate and dose concentration, the random coincidence rate is already 2.5 times that of the true + scatter coincidence rate.

Fig. 10 is the true + scatter count rate versus coincidence window curve. From Fig. 10, we can determine when using wider coincidence window multiples rejection will cause more significant drop of true + scatter count rate. The wider coincidence time window strengthens the effect of multiples rejection in losing true + scatter data. Since the expected coincidence window FWHM in this project is 6 ns, the effect of multiple rejections should be considered.

In all these curves, the difference between ideal results and measure results is caused by the TDC 16 ns dead time.

## B. Noise-Equivalent Count Rate (NECR) Study

In emission tomography, the Noise Equivalent Count Rate (NECR) is given by (1) [17]

$$\text{NECR} = \frac{[(\text{True} + \text{Scatter})(1 - \text{SF})]^2}{\text{True} + \text{Scatter} + 2 \text{ Random}} \quad (1)$$

Fig. 11 represents NECR as a function of dose with multiples and with rejection of multiples. In this setup, the NECR drops almost 50% when multiples are rejected. With Fig. 11, we can choose the optimal imaging dose to maximize NECR for this brain-PET camera when imaging the human brain. Typically with the standard 10 mCi of FDG tracer injection for the whole body plus a 1-hour tracer-uptake waiting time before imaging, the brain has less than 1 to 1.5 mCi of activity during imaging, which is below the 2.5 to 3 mCi at the peak NECR, assuming a 6-ns coincidence window is used.

Fig. 12 illustrates a curve of NECR versus dose at different coincidence time windows. It shows that if possible, smaller coincidence windows improve the NECR. With the typical brain size of 18-cm, a 3-ns coincidence window should be adequate for a TOF brain-PET, and with a 3-ns window, the peak NECR occurs at 5 mCi of activity in the brain.

## C. Statistical Noise

Using the delay coincidence method for random background subtraction produces more statistical noise than using the profile distribution and count rate methods. For extremely small, high resolution detectors, [18] each small detector acquires fewer counts than a larger detector under the same conditions. It will suffer even more from statistical noise in random coincidence. In our future work, we are planning to apply software filters in several adjacent small detectors to increase the statistical performance of random coincidence evaluation.

## IV. CONCLUSION

In this article, we describe a low-cost TOF-coincidence system using a hybrid method combining AND-logic and time-mark technology that we developed and tested using GATE simulation data. This system can be applied to both TOF and non-TOF PET cameras. It offers the option of accepting and rejecting multiples coincidences and the coincidences window can be adjusted to optimized system NECR. This FPGA-based coincidence system for modular PET camera offers reprogrammable flexibility and expandability; the same circuit board can be used for animal PET, breast PET, brain PET and wholebody PET camera. This TOF coincidence processing system when used in our brain PET camera can process  $7 \times 10^6$  total coincidences/sec with 2.5 to 5 mCi within the AFOV depending on the timing window used (6 to 3 ns).

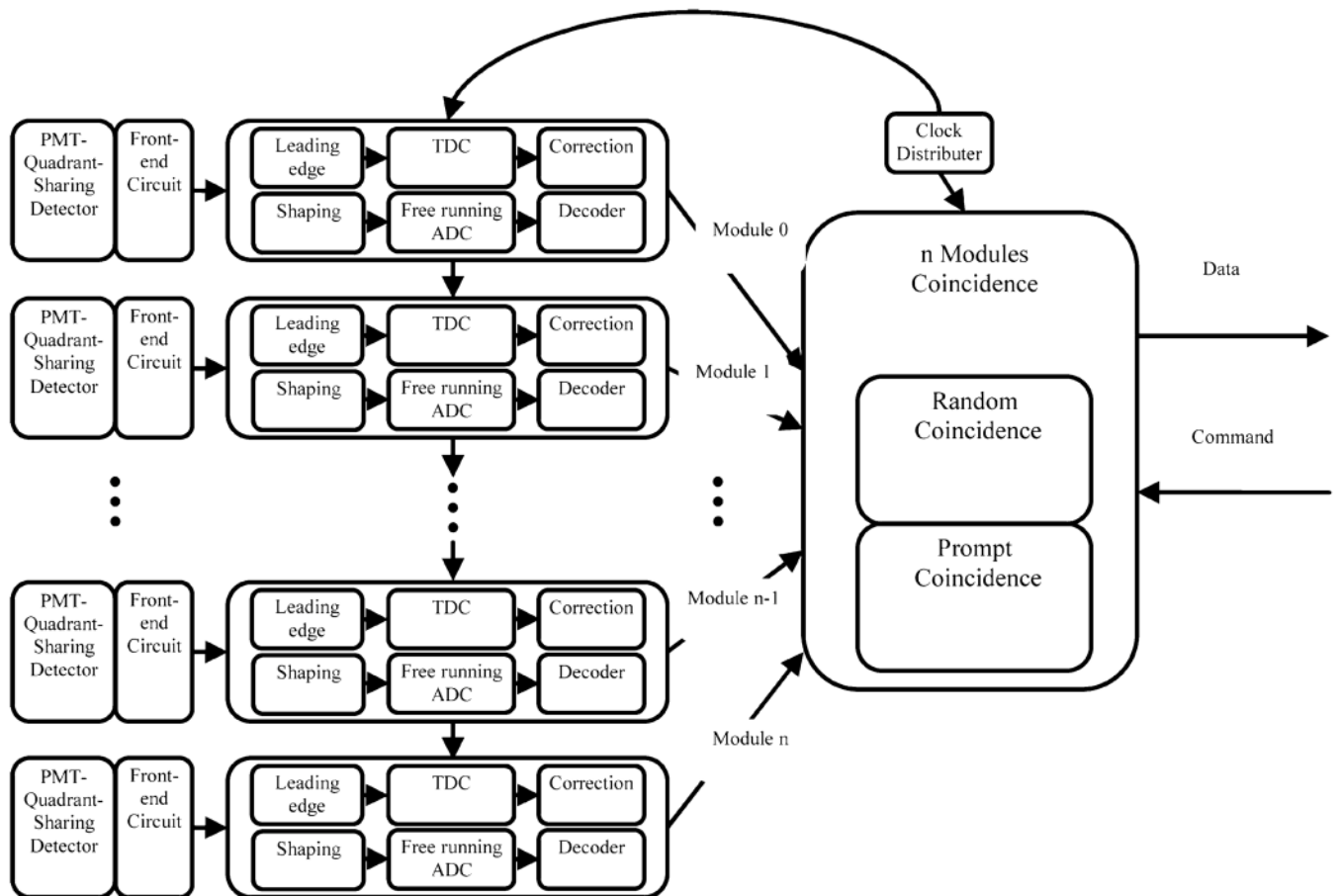
## Acknowledgments

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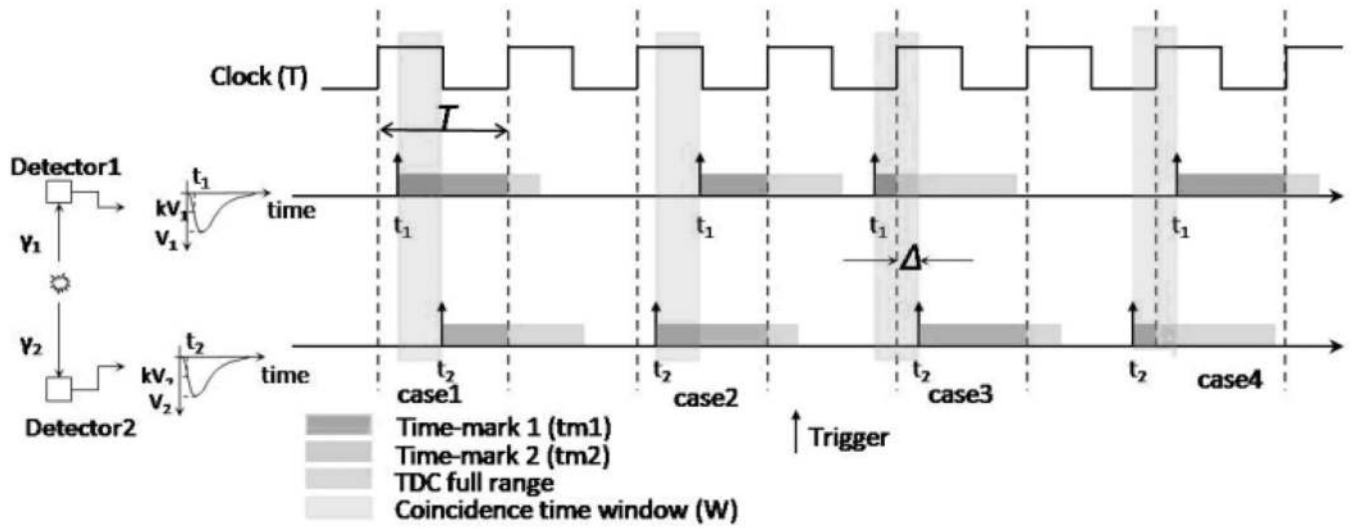
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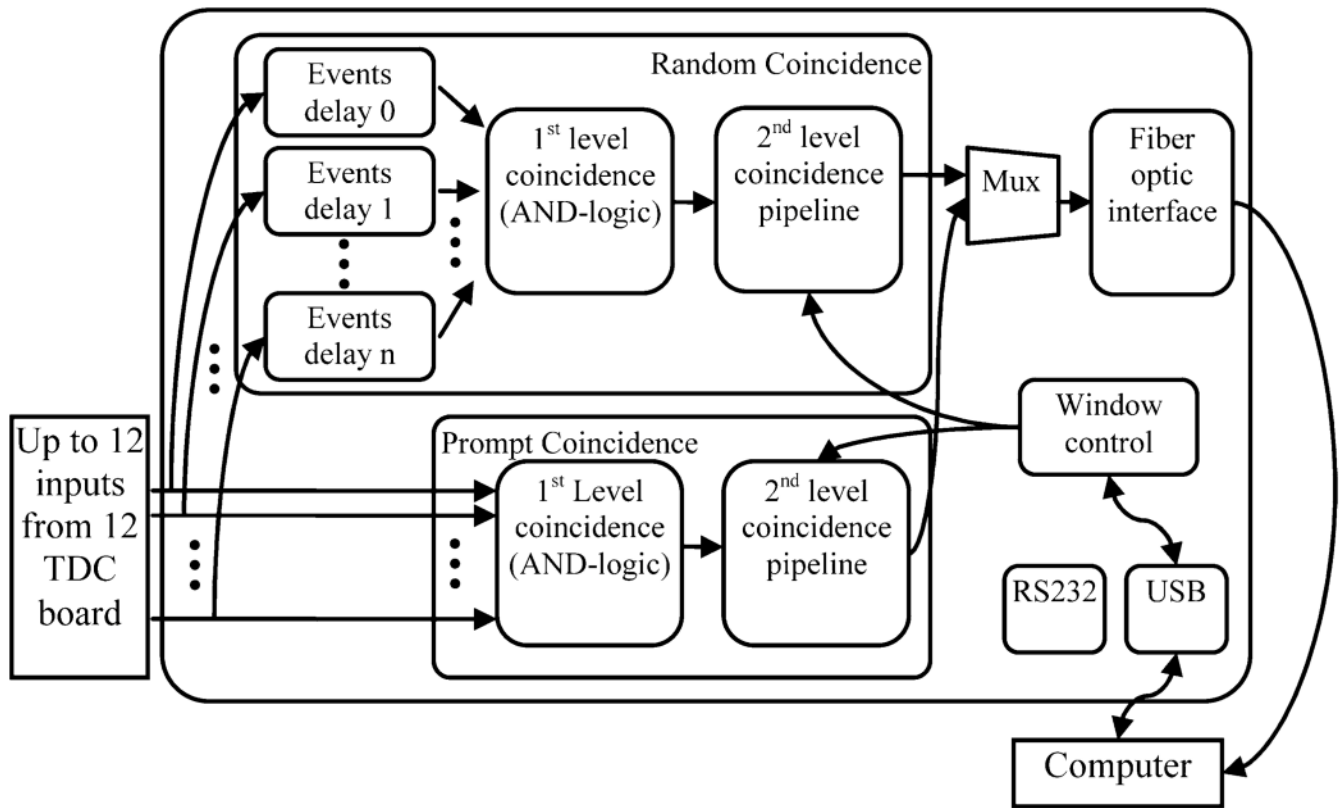


**Fig. 1.**  
Electronics system diagram for a module-based PET camera.

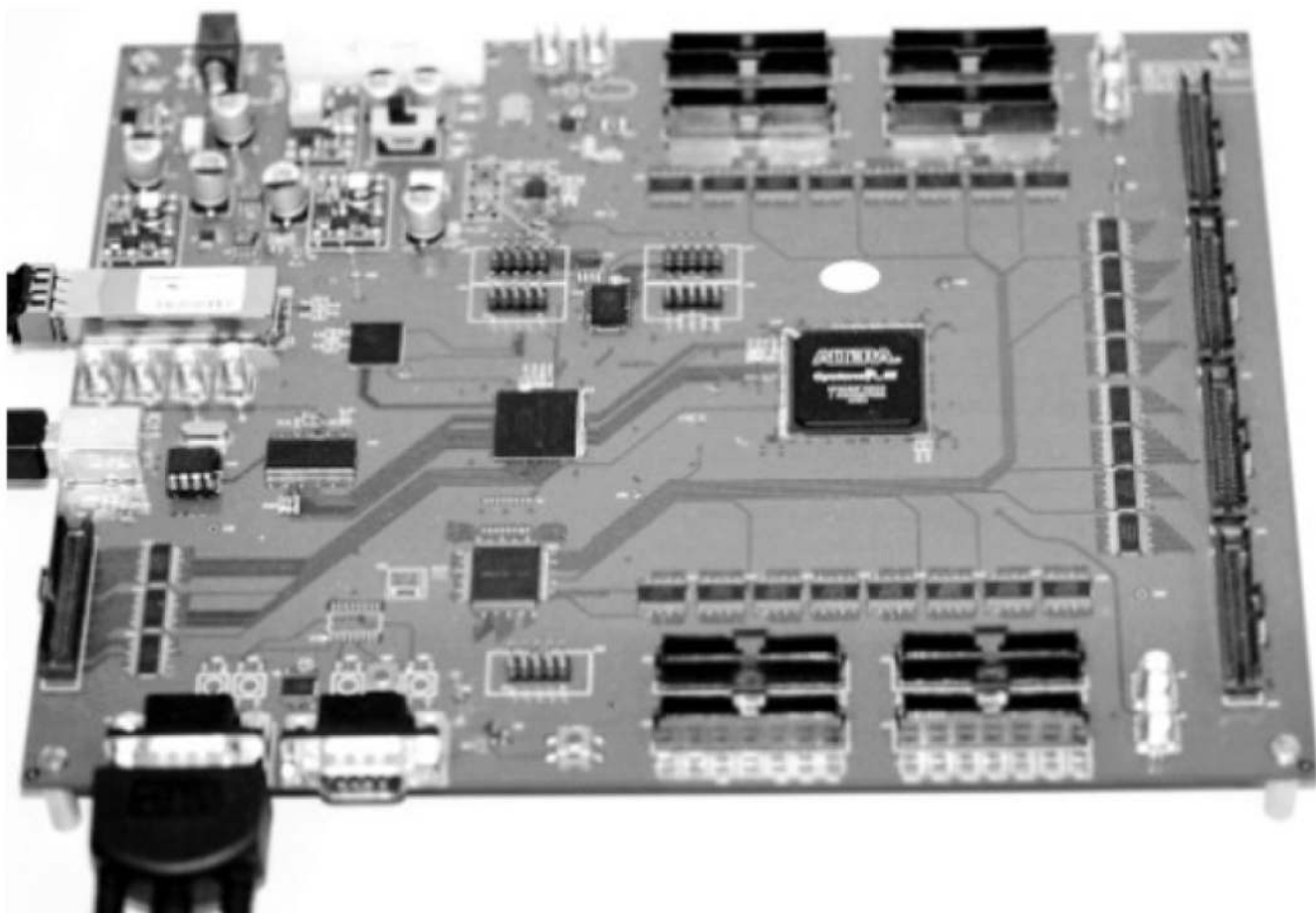




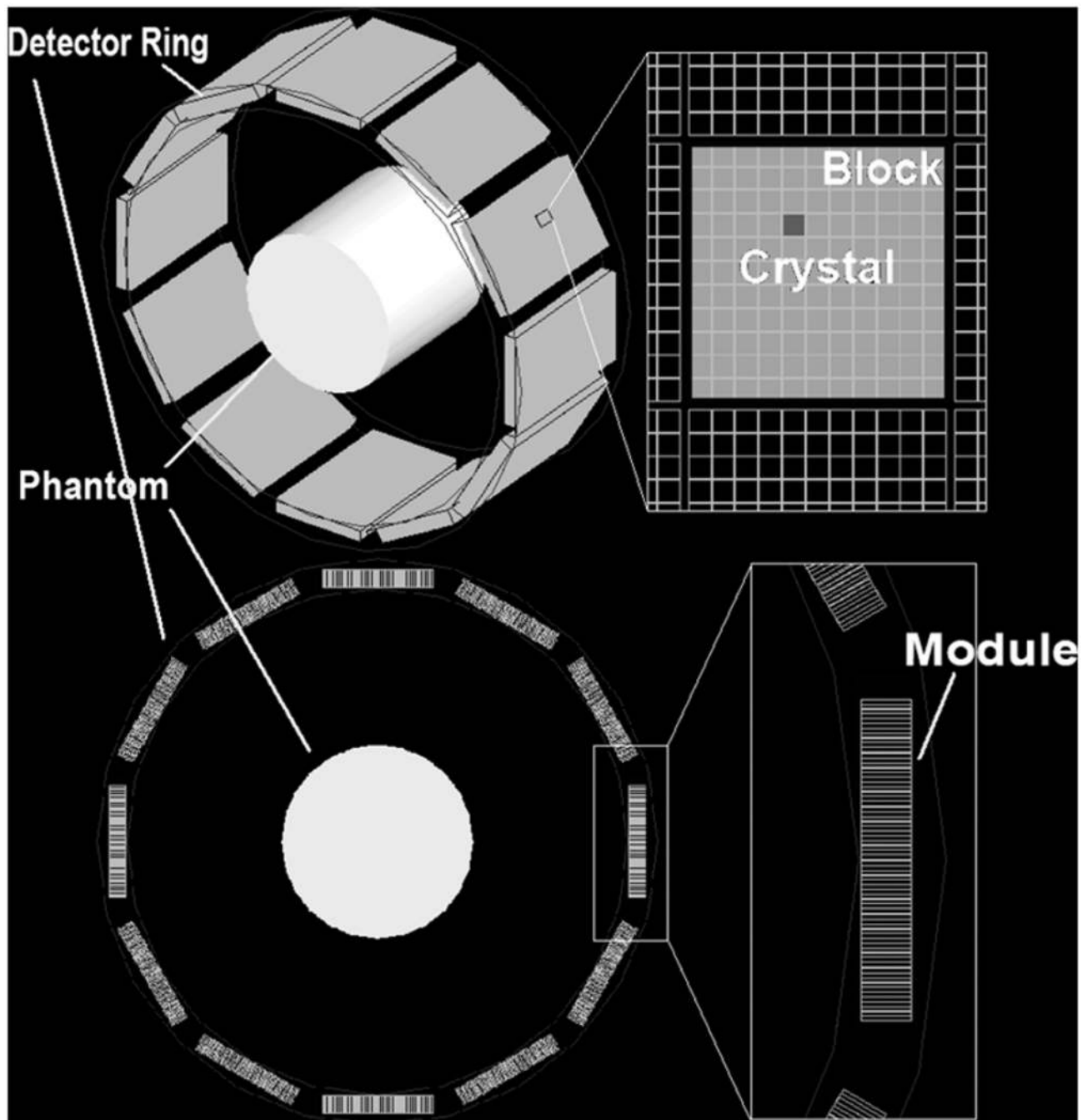
**Fig. 2.** System clock synchronized triggers and time-mark generation by TDC.



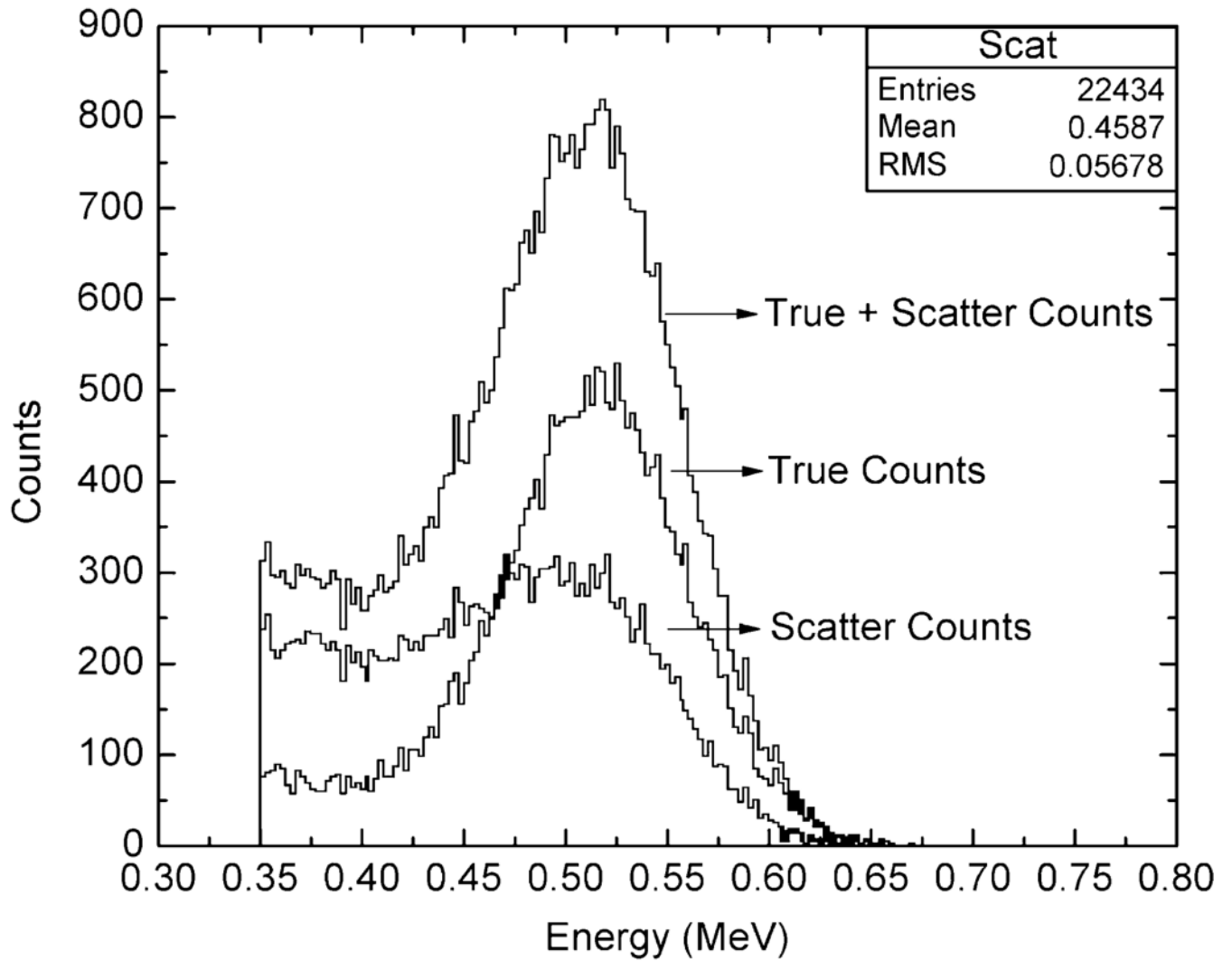
**Fig. 3.**  
System diagram of the coincidence system.



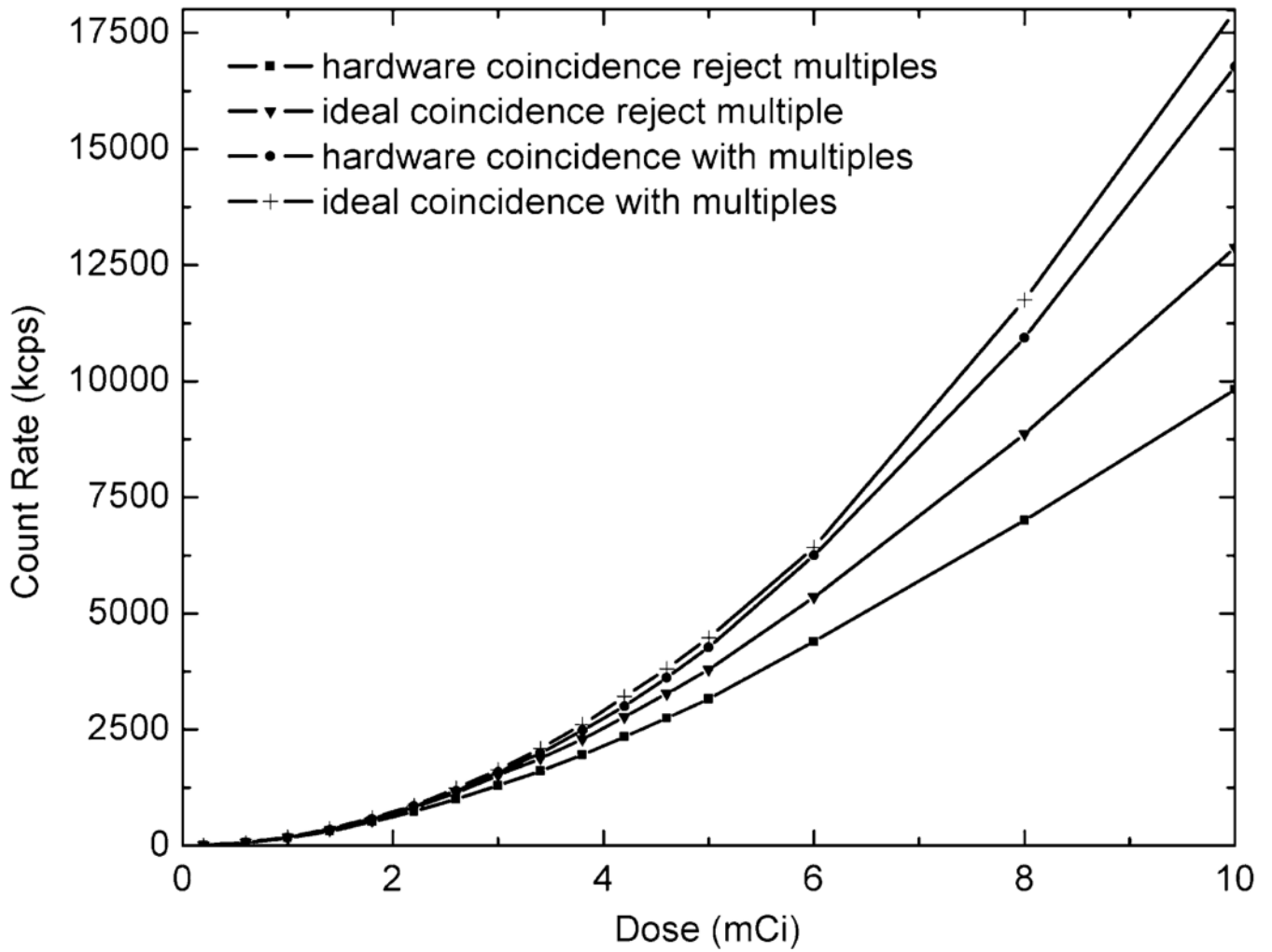
**Fig. 4.**  
Coincidence system (photo).



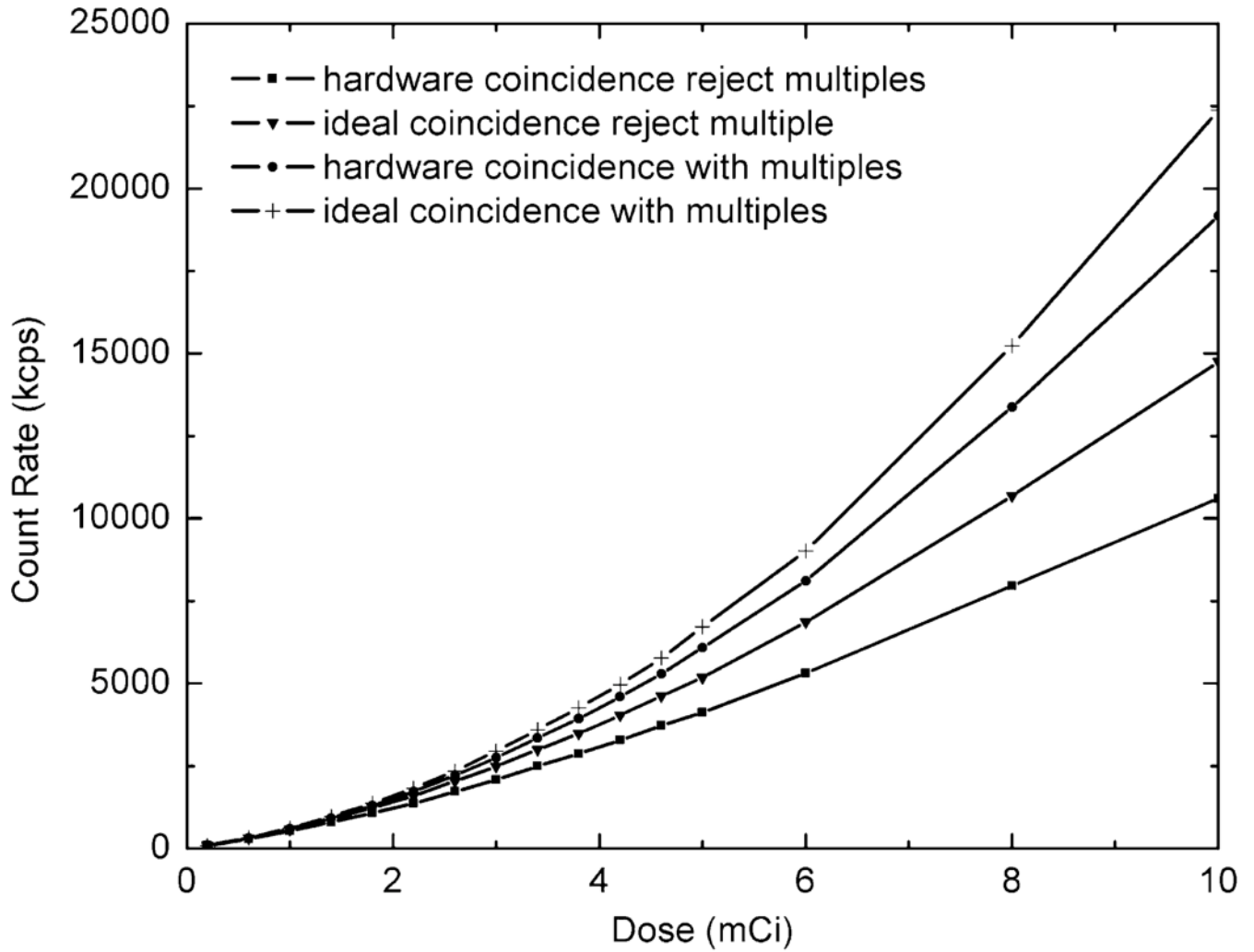
**Fig. 5.** GATE Monte Carlo simulation model of the PET in brain mode and the expanded view of module, block and crystal arrangements.



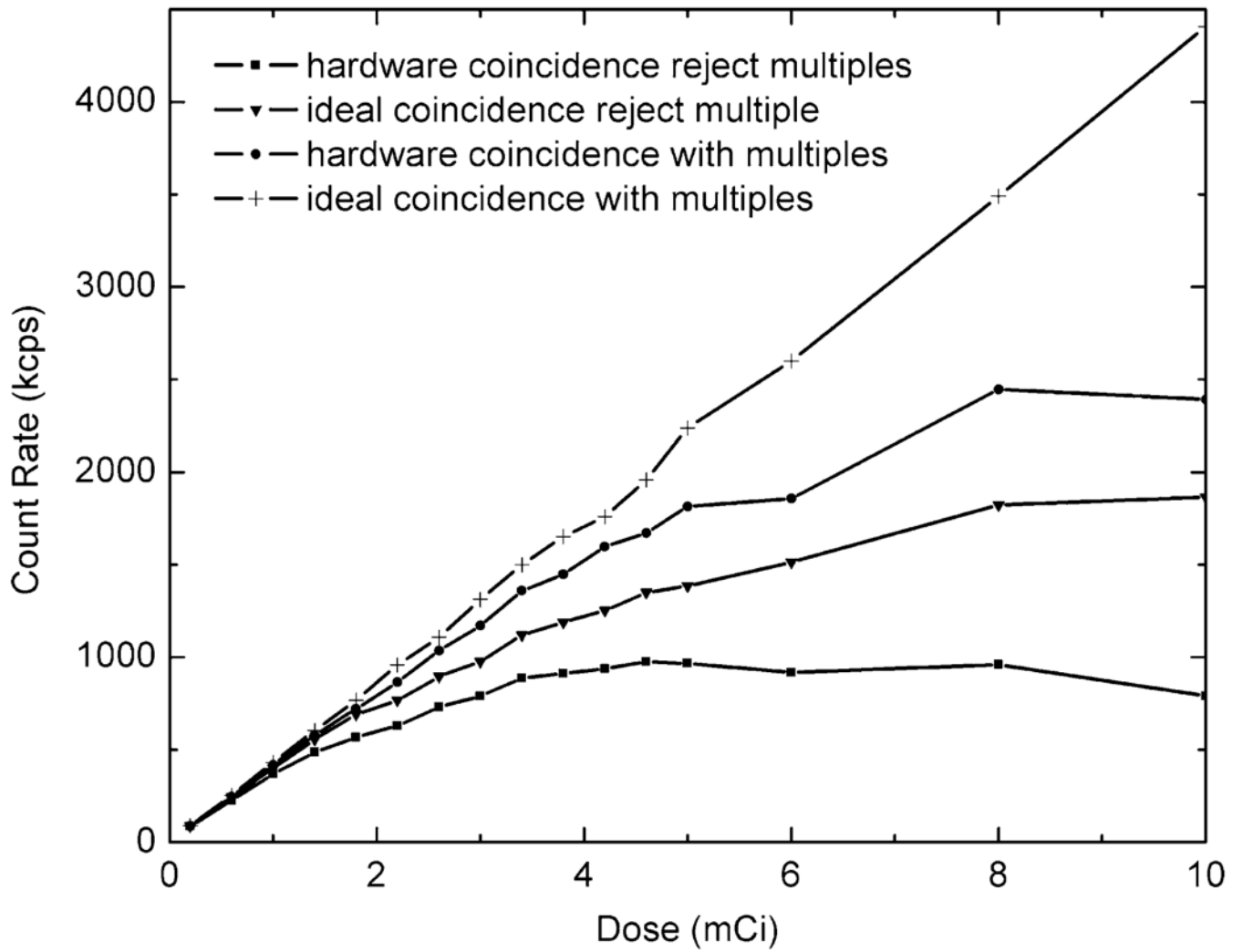
**Fig. 6.** Energy spectrum of GATE simulation result for scatter factor evaluation. The scatter factor is 0.46.



**Fig. 7.**  
Random coincidence count rate versus dose. Scatter factor = 0.46.

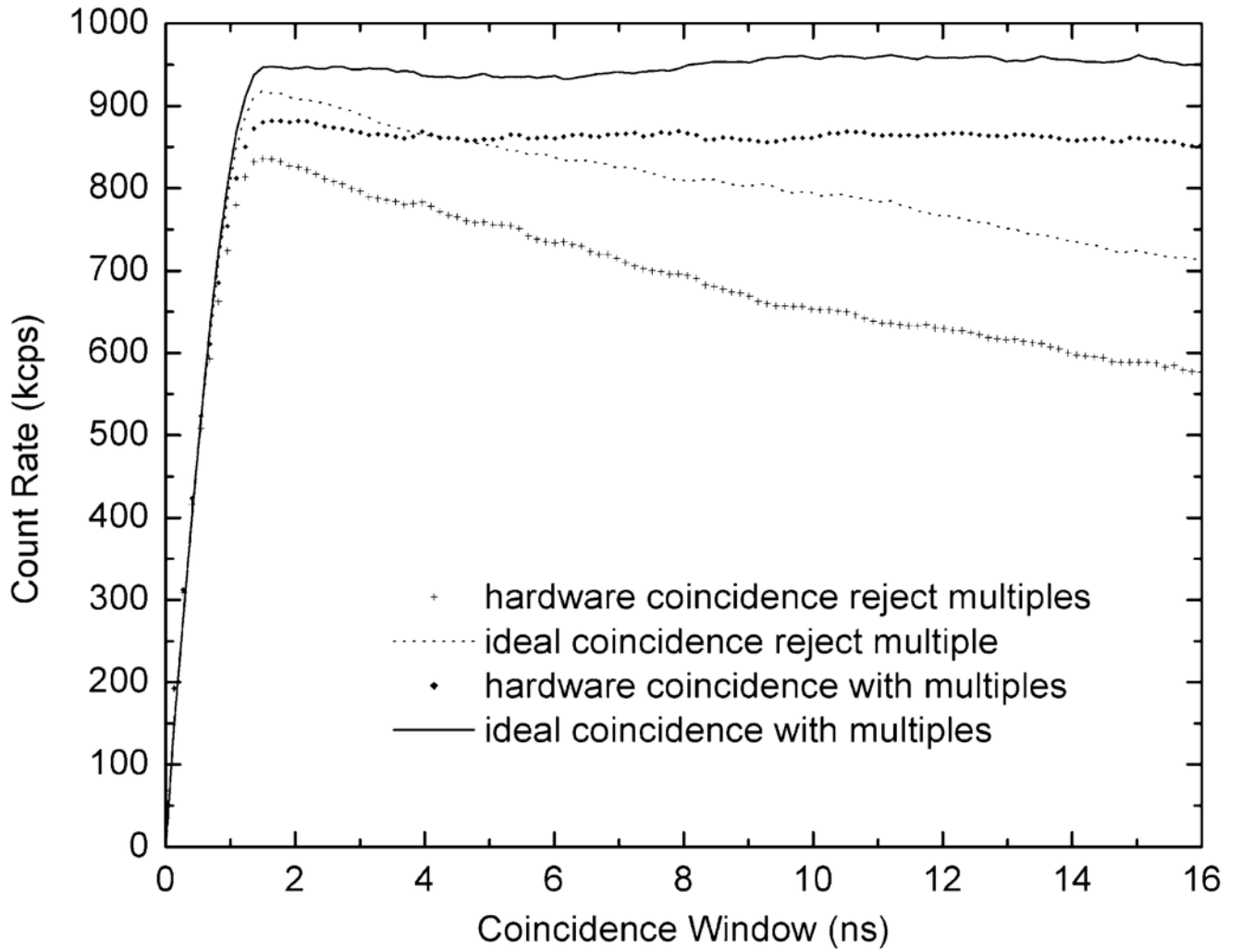


**Fig. 8.** Prompt coincidence count rate versus dose. Scatter factor = 0.46.

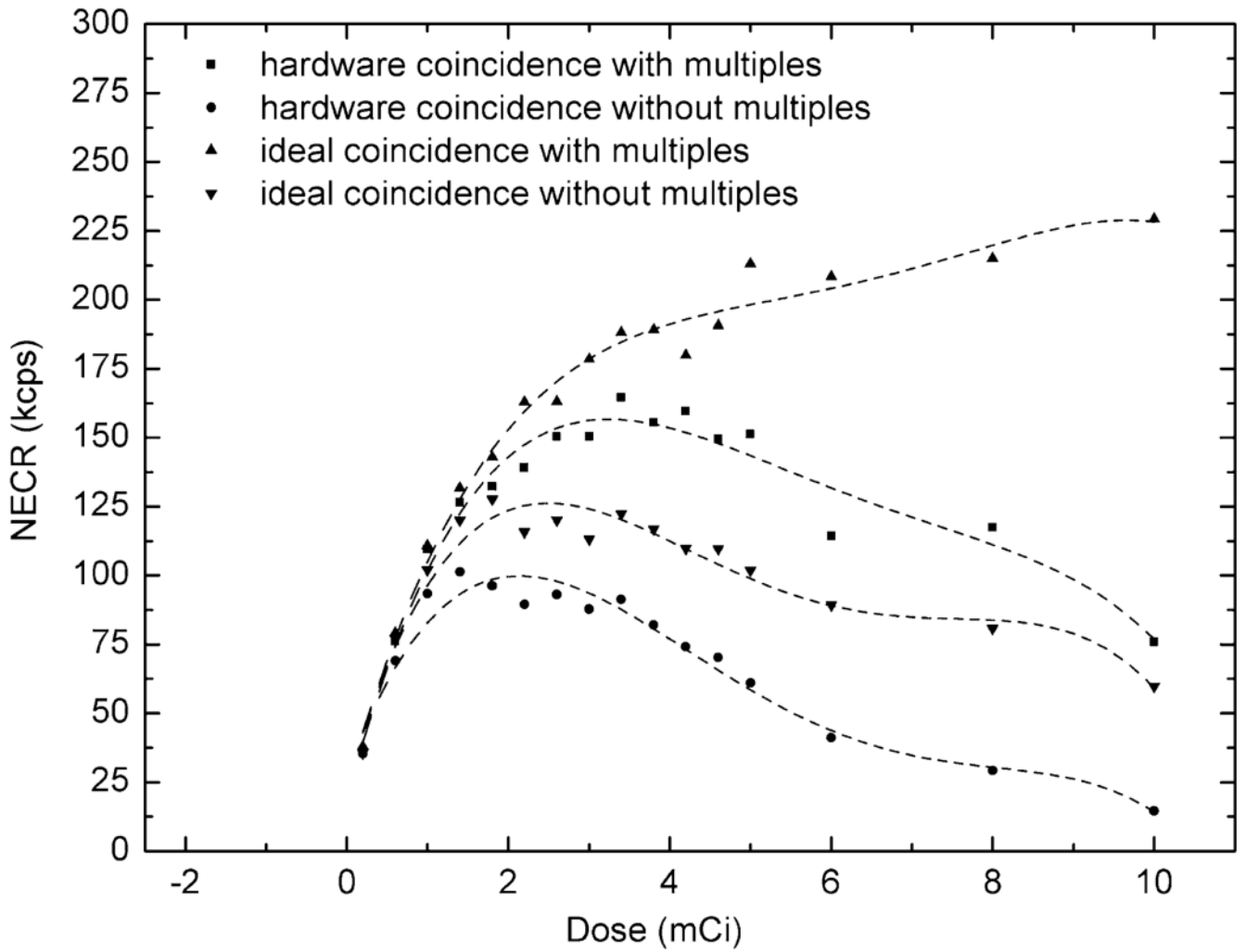


**Fig. 9.**  
True + scatter coincidence count rate versus dose. Scatter factor = 0.46.

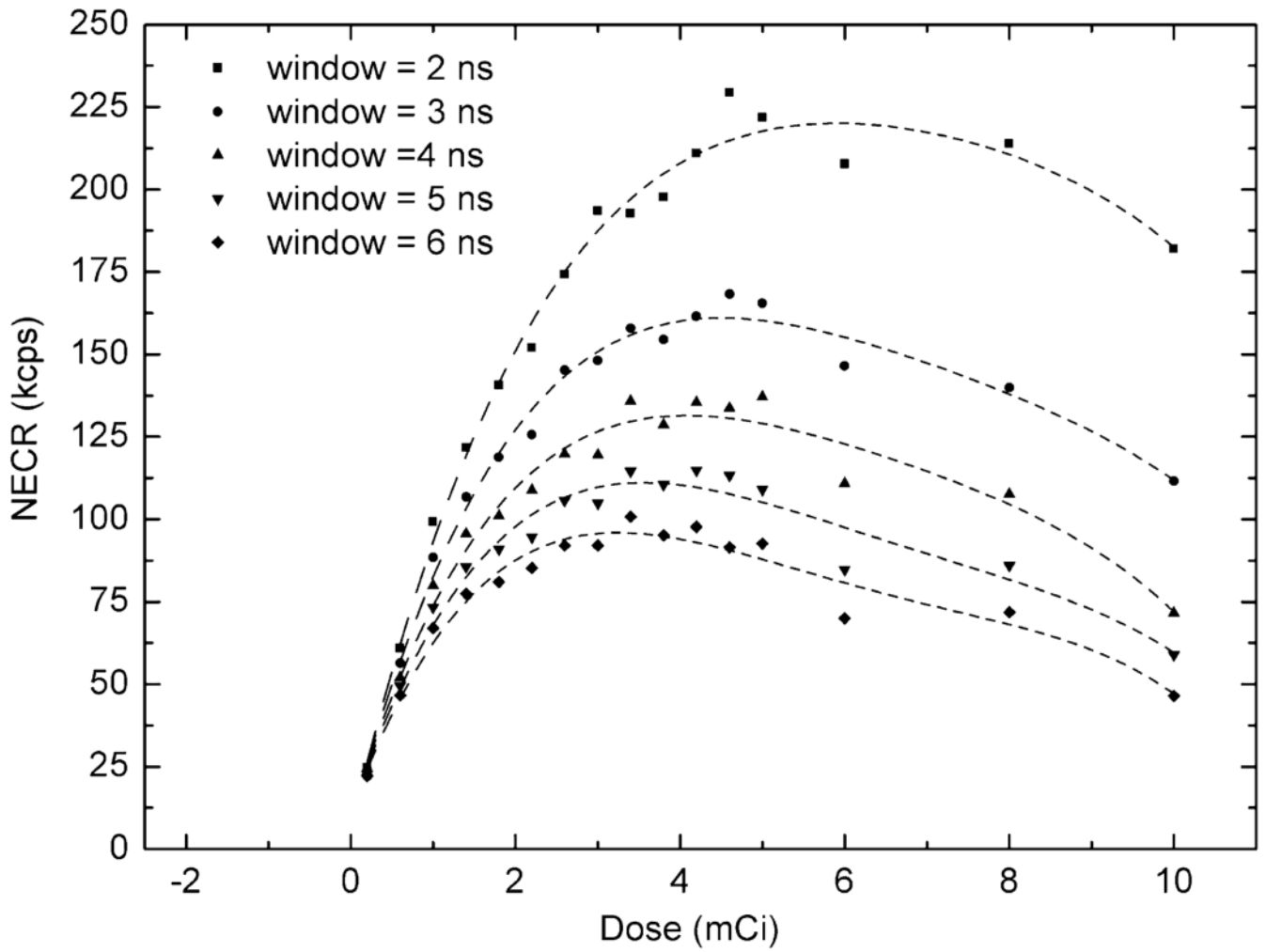




**Fig. 10.** True + scatter coincidence count rate versus coincidence window. Scatter factor = 0.46.



**Fig. 11.**  
NECR versus dose, coincidence window = 6 ns, scatter factor = 0.46.



**Fig. 12.** NECR versus dose, hardware coincidence with multiples. Result in different coincidence time windows. Scatter factor = 0.46.

**TABLE I**

Time-Mark Difference Range and Raw Code Between Two Modules (Four Cases)

Range	Raw Code	Case
$[-T, W-T]$	-1	3
$[-W, W]$	0	1&2
$[T-W, T]$	1	4

**TABLE II**

GATE Simulation Set-Up for Evaluation (Brain-PET Mode)

Specifications	Parameters
Ring diameter	540 mm
Number of modules per Ring	12
Ring axial field of view	21 cm
Module block-array	10×6
Module size	19.36 × 19.36 × 18 mm
Block pitch	19.65×19.65 mm
Scintillator material	LYSO
Block Array	11×11 LYSO
Phantom type	Ø20 cm × 19 cm (uniform)
Protocol [16]	NEMA NU2-1994
Dose	F <sup>18</sup> , from 0.2 mCi to 10 mCi