A Reappraisal of Optimum Output Matching Conditions in Microwave Power Transistors

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***Abstract*— This paper presents a novel approach to the identification of output power and efficiency contours in microwave power transistors in compressed regime. The formulation is based on a polynomial representation of the drain–source voltage profile accounting for the knee region. Closed-form equations for the output power and efficiency as function of the fundamental load are demonstrated, enabling the plot of contours on a Smith Chart. From these, a further simplified drawing procedure for approximated contours is also derived, differentiating between two families of output characteristic. The first, with smooth knee, is usually experienced in GaN devices, while the second exhibits a steep knee which can be associated with GaAs devices' typical behavior. A 5-W GaN HEMT, a 2.5-W GaN HEMT, and a 0.7-W GaAs pHEMT are characterized with load-pull measurements. In all the three cases, the proposed method results in a very accurate contour construction, despite being based on an approximated output current/voltage profile and on a rough estimate of output equivalent capacitance.**

***Index Terms*— Field-effect transistors, high-efficiency amplifiers, power amplifiers (PAs).**

I. Introduction

IT HAS long been recognized that loadline considerations can be used to design power amplifiers at higher frequencies, so long as the impedance reference plane is set at a conceptual point which lies "inside" the device output parasitics [1]–[3]. Over thirty years ago, one of the present authors [3] showed how the basic loadline method could be extended to take account of reactive loads and as such showed how plausible "load–pull contours" could be constructed with minimal large-signal power measurements. This analysis, however, made several simplifying assumptions; in particular, it only accounted for situations where the device plane voltage swing remained outside of the I–V "knee" region. This assumption is especially restrictive for cases where the device is presented with an impedance whose magnitude is higher than the loadline resistance. Nevertheless, the technique in [3] has been widely and successfully used for the design of linear RF power amplifiers (RFPAs) operating up to, but not beyond, the 1-dB compression point.

Other approaches have been pursued to approximate the optimum load conditions without relying on large-signal measurements or models. The simple model proposed in [4] explicitly includes device parasitics to predict the contours at different frequencies. The work presented in [5] uses a small signal equivalent model to extract a first approximation of class-A power amplifier (PA) optimum power loads. It takes into account the voltage/current device limitations, in this case a GaAs pHEMT, by imposing elliptic dynamic I–V curves tangential to the maximum current/voltage limits. The methodology of [3] is extended to Cascode stages in the work presented in [6].

The need to predict, at least in a first approximation, the efficiency of the PA for varying load has become particularly important for the design of Doherty amplifiers. In fact, the simplistic assumption frequently made in the literature that constant efficiency can be maintained using the textbook load modulation has been shown to be inaccurate; this is due in part to the knee clipping of the device current during the entire load modulation regime. In [7], this phenomenon is explained relying on a simplified device (LDMOS in this case) model taking into account for R_{ON} and for the smooth turn-ON of the transcharacteristic. The proposed model in [7] is able to accurately predict power and efficiency contours in linear operation (around 1-dB gain compression), as it has been refined and extended to higher power LDMOS transistors in [8]. On the other hand, the different knee interaction for varying load can be exploited, as shown by [9] and [10], to increase the average efficiency of the Doherty PA.

Recently, some advanced PA architectures that intentionally drive the device into the saturated region have been reexamined as candidates for highly linear RFPA applications. For example, the Chireix outphasing PA is receiving renewed attention, largely due to the now widespread use of digital signal processing and the consequent ability to generate complex baseband and IF signal formats [11]. Moreover, numerous nontelecom applications often make use of PAs with devices operated well into saturation. As such, this paper addresses a need for a more generic theory that characterizes the power and efficiency behavior of an RF power transistor that may include operation well into the clipping, or saturation, region. The approach, however, still attempts to retain the simplistic spirit of the original analysis in [3], and it is based on the approximation of the I–V output characteristics by means of a polynomial.

This paper is organized as follows. Section II explains the applied approximations and derives the closed-form equations for output power and efficiency. Section III uses the obtained equations to analyze the variational trends of optimum power/efficiency loads for different knee profiles, and proposes a further simplified method for graphically build-

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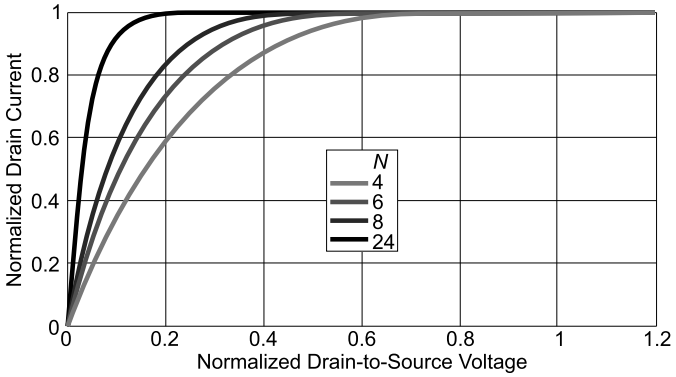


Fig. 1. Knee profile versus v_{ds} for $N = 4$ (light gray), 6 (gray), 8 (dark gray), and 24 (black).

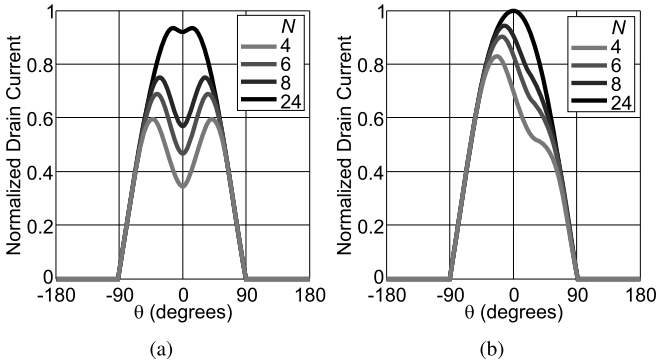


Fig. 2. Intrinsic current waveforms for $N = 4$ (light gray), 6 (gray), 8 (dark gray), and 24 (black). (a) $V = 0.9$ and $\phi = 0$. (b) $V = 0.8$ and $\phi = -(\pi/8)$.

ing the contours. Section IV reports the comparison between estimated and measured power/efficiency contours for GaN and GaAs devices. Finally, Section V draws some conclusions.

II. Basic Concept

Loadline-based PA design of a tuned class-B amplifier defines the optimum load for output power as $R_{opt} = 2V_{DD}/I_{MAX}$, where V_{DD} is the drain bias voltage, and I_{MAX} is the maximum of the truncated sinewave that represents the drain current. In a normalized representation, where $V_{DD} = I_{MAX} = 1$, R_{opt} results equal to 2, the maximum output power is $(V_{DD}I_{MAX})/4 = 0.25$, and the maximum efficiency is $\pi/4$. In this paper, the normalized drain current is defined as

$$i_{ds}(\theta) = A(\theta)k(v_{ds}) \tag{1}$$

where $A()$ is the baseline function, determined as the transconductance function applied to the input voltage, thus a periodic function of the angle θ, while $k()$ describes the knee as the function of the normalized drain–source voltage v_{ds}.

A simple polynomial form is used for $k()$

$$k(v_{ds}) = 1 - (1 - v_{ds})^N \tag{2}$$

where N is an even integer identifying the polynomial order. The profile of $k()$ is shown in Fig. 1, for different N values. For N that tends to very high values, function tends toward the "text book" approximation of zero knee voltage. A realistic approximation of a typical GaN device behavior is obtained with $4 \leq N \leq 8$, while a higher N should be adopted for GaAs devices (e.g., $N > 20$). It is important to notice that the knee profile to be approximated must refer to a pulsed I–V measurement or a dynamic RF "fan diagram," to account for dispersion and thermal issues. The fan diagram is a collection of dynamic load line measurements on different intrinsic resistive loads that highlights the profile of the knee [12]. The formulation of (2) is particularly convenient when assuming short-circuited harmonics, writing v_{ds} as

$$v_{ds}(V, \phi) = 1 - V\cos(\theta + \phi) \tag{3}$$

where V and ϕ are free parameters that can be swept to simulate arbitrary complex terminations at fundamental. If harmonic loads are not short circuited, as in the case of exploiting different PA classes [13], it is not possible to identify unequivocally the voltage waveform shape, and a numerical approach may be followed for the determination of the contours [14]. With shorted harmonics, the knee description becomes

$$k(v_{ds}) = 1 - V^N\cos(\theta + \phi)^N. \tag{4}$$

Two examples of current profiles are shown in Fig. 2, with $V = 0.9$ and $\phi = 0$ and $V = 0.8$ and $\phi = -(\pi/8)$, $N = 4$, 6, 8, and 24, and assuming a class-B baseline current. Notice that V can be actually pushed slightly above 1 to emulate very compressed behavior of the transistor [15].

An important consideration to be drawn is related to the nonphysical behavior of the polynomial function when $v_{ds} \gg 1$, that corresponds to $k(v_{ds})$ approaching zero for $v_{ds} = 2$. The impact of this approximation will be negligible for $|\phi|$ close to 0, when considering class-B or deep-class-AB cases, since the current baseline function $A()$ is also very close to zero in that output characteristic region. For $|\phi|$ approaching $(\pi/2)$, an error in the evaluation of dc and fundamental components of current is present. However, the amount of this error is very low, even for low N, and will only result in a limited distortion of contours in the extreme cases of highly reactive loads that are seldom exploited in PA design.

The knee function of (4) can be expanded in

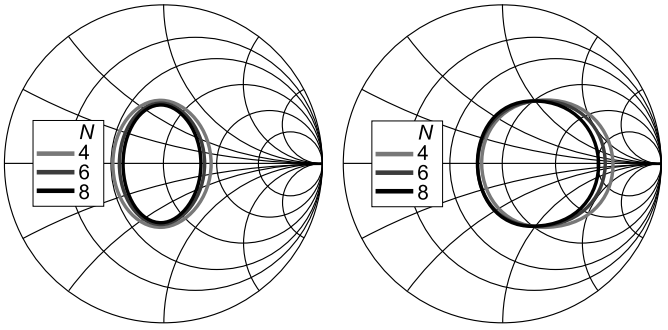
$$k(v_{ds}) = k_0 + \sum_{n=1}^{\frac{N}{2}}[k_{2n,R}\cos(2n\theta) + k_{2n,Q}\sin(2n\theta)]. \tag{5}$$

The k_j terms are functions of (V, ϕ)

$$\begin{aligned} k_0 &= 1 - \left(\frac{V}{2}\right)^N \binom{N}{N/2} \\ k_{2n,R} &= -2\left(\frac{V}{2}\right)^N \binom{N}{N/2 - n}\cos(2n\phi) \\ k_{2n,Q} &= 2\left(\frac{V}{2}\right)^N \binom{N}{N/2 - n}\sin(2n\phi). \end{aligned} \tag{6}$$

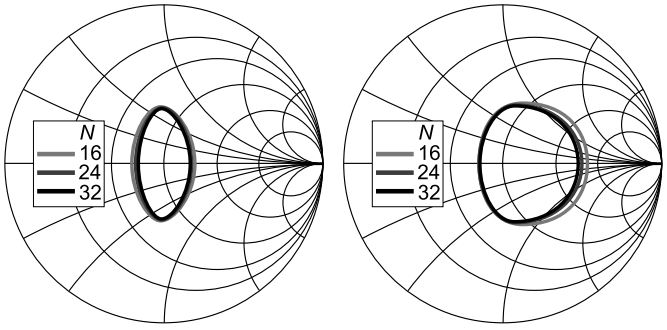
The terms $\binom{N}{N/2}$ are a binomial form. If the current baseline function $A()$ is even, as normally assumed in theoretical PA analyses, it can be expanded as

$$A(\theta) = A_0 + \sum_{n=1}^{\infty}[A_n\cos(n\theta)]. \tag{7}$$



(a) (b)

Fig. 3. (a) Power and (b) efficiency contours with $N = 4$ (light gray), 6 (dark gray), and 8 (black).



(a) (b)

Fig. 4. (a) Power and (b) efficiency contours with $N = 16$ (light gray), 24 (dark gray), and 32 (black).

The dc and fundamental components of $i_{\rm ds}$ result, after some rearrangement, as

$$I_0 = A_0 k_0 + \frac{1}{2}\sum_{n=1}^{\frac{N}{2}}[A_{2n}k_{2n,\rm R}]$$
$$I_{1\rm R} = A_1 k_0 + \frac{1}{2}\sum_{n=1}^{\frac{N}{2}}[(A_{2n-1}+A_{2n+1})k_{2n,\rm R}]$$
$$I_{1\rm Q} = \frac{1}{2}\sum_{n=1}^{\frac{N}{2}}[(A_{2n-1}-A_{2n+1})k_{2n,\rm Q}]. \quad (8)$$

Writing the fundamental voltage and current in phasor form

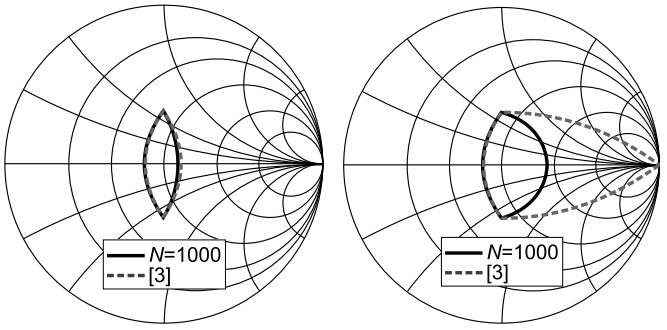
$$V_{\rm DS} = V(-\cos(\phi) + j\sin(\phi)), \quad I_{\rm DS} = I_{1\rm R} + jI_{1\rm Q} \quad (9)$$

allows evaluating output power, efficiency, and load

$$P_{\rm OUT}(V,\phi) = \frac{1}{2}\Re\{V_{\rm DS}(-I_{\rm DS}^*)\}$$
$$\eta(V,\phi) = \frac{P_{\rm OUT}}{I_0}$$
$$Z_1(V,\phi) = -\frac{V_{\rm DS}}{I_{\rm DS}}. \quad (10)$$

Now, for each current and knee profile, it is possible to trace power and efficiency contours by sweeping the (V,ϕ) values.

Fig. 3 shows the power and efficiency contours, obtained with a truncated sinewave for the current, class-B bias, and for knee polynomial orders of $N = 4$, 6, and 8. The Smith chart normalization impedance is $R_{\rm opt} = 2$. Calculations are performed in MATLAB using the expressions (6)–(10), and the contours are traced with the native *contour* function. Fig. 4 reports the same type of contours but evaluated for $N = 16$, 24, and 32, representing realistic knee approximations for GaAs devices. It can be seen that the obtained power contours are distinctly noncircular, and that they converge for increasing N. Fig. 5 reports the contours for $N = 1000$, where the polynomial knee function tends to an ideal abrupt knee function, compared with the contours proposed in [3]. On the left Smith chart quadrants, the contours are identical, being the region not affected by current clipping; the impedance magnitude is lower than that required to cause the voltage to reach the knee region. Since the current is unclipped, power and efficiency contours are coincident. On the other hand,



(a) (b)

Fig. 5. (a) Power and (b) efficiency contours with $N = 1000$ (black solid) compared with the contours proposed in [3] (gray dashed).

the right-hand quadrants show significant separation of power and efficiency contours due to the current clipping effects. Although this has been cited as a flaw in the theory proposed in [3], this difference is mainly due to the fact that the contours in [3] were defined by reducing the maximum current so as not to clip the waveforms, thus avoiding any knee effect. So this discrepancy in fact only applies to efficiency; the clipped (right-hand) power contours are quite close to the original circular arc proposed in [3]; this is somewhat fortuitous inasmuch as the derivation in [3] was based on backed-off current swing rather than the clipped current waveform analysis.

III. Predicting Power and Efficiency Contours

A. Locating Maximum Values and Optimum Loads

By observing the contour plots in Figs. 3 and 4, it can be seen that the maximum for power ($P_{\rm max}$) and efficiency ($\eta_{\rm max}$) always correspond to loads R_p and R_η on the real axis, i.e., to $\phi = 0$. This is consistent with the previous results on tuned load PAs [8], [16]. It can be demonstrated that, for $\phi = 0$, the output power and the efficiency can always be written as

$$P_{\rm OUT}(V,\phi=0) = \frac{aV(1-pV^N)}{4}$$
$$\eta(V,\phi=0) = \frac{\pi b}{4}\frac{V(1-pV^N)}{(1-dV^N)}. \quad (11)$$

The real coefficients a, p, b, and d are function of N and of the baseline current waveform. The value of V that maximizes

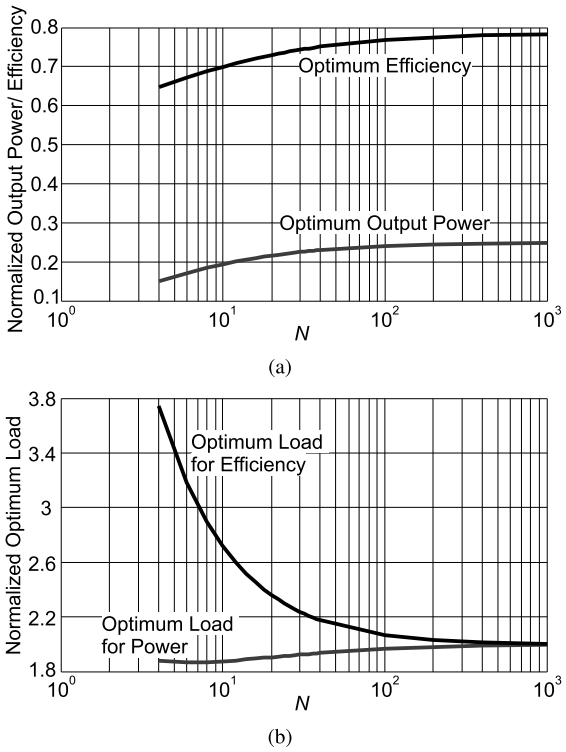


Fig. 6. (a) Power (gray) and efficiency (black) optimum value and (b) load versus N.

the output power ($V = V_p$) and the efficiency ($V = V_\eta$) can be determined after equating to 0 the derivative of (11)

$$\frac{a\left(1-(N+1)pV_p^N\right)}{4} = 0$$

$$\frac{\pi b}{4}\frac{1-((N+1)p-(N-1)d)V_\eta^N+pdV_\eta^{2N}}{\left(1-dV_\eta^N\right)^2} = 0. \quad (12)$$

This results in

$$V_p = ((N+1)p)^{-\frac{1}{N}}, \quad V_\eta = \sqrt[N]{t} \quad (13)$$

where t is the only solution to the second-order polynomial $1-((N+1)p-(N-1)d)\,t+pdt^2$ giving positive dc current.

Once V_p and V_η are known, the corresponding real loads can be calculated. Fig. 6 reports the values of $P_{\max}$, $\eta_{\max}$, R_p, and R_η versus knee order N, considering a class-B current baseline waveform. As expected, for N that tends to very high values, R_p and R_η tend to converge to $R_{\text{opt}} = 2$, and the values of $P_{\max}$ and $\eta_{\max}$ achieve their theoretical limits of 0.25 and $\pi/4$, respectively. For $4 \le N \le 8$, R_p is around 1.9, and R_η is around 1.5–2 times R_p.

B. Construction of Approximated Contours for Smooth Knee Devices

The proposed method permits to build the contours solving few equations. However, a further simplification is possible by graphically approximating the contours, enabling an even simpler implementation of this method in a CAD environment. From Fig. 3, it can be seen that efficiency contours for low values of N, typical of GaN devices, can be reasonably approximated by circles centered on the real axis. To determine the center and radius of these circles, it is sufficient to know the intersections with the real axis that can be found as the real roots to the following $N+1$ order polynomial equation:

$$10^{-\alpha/10}\eta_{\max} = \frac{\pi b}{4}\frac{V(1-pV^N)}{(1-dV^N)}. \quad (14)$$

The coefficient α, in dB, determines the level of the efficiency contour. The obtained solution in V variable leads to two points on the Smith chart, assuming a normalization impedance of $R_{\text{opt}} = 2$. Conversely, the power contours are not well approximated by circles, but they result more similar to ellipses with the vertical axis (y-radius) longer than the horizontal one (x-radius). The center and the horizontal radius of the ellipse can be found in a similar manner to the efficiency contour derivation, by solving the equation

$$10^{-\alpha/10}P_{\max} = \frac{aV(1-pV^N)}{4}. \quad (15)$$

Vertical radius can be found by locating the points on the contour where the real part of Γ equals the ellipse center.

Considering a class-B truncated cosine as current baseline, the center and radii for $N = 4$, 6, and 8, and different α values are reported in Tables I and II for efficiency and power, respectively.

TABLE I
CENTER AND RADIUS FOR APPROXIMATED EFFICIENCY CONTOURS IN Γ

α	Center			Radius		
(dB)	N=4	N=6	N=8	N=4	N=6	N=8
0	0.30	0.23	0.18	0	0	0
0.5	0.29	0.24	0.21	0.31	0.30	0.29
1	0.28	0.24	0.22	0.42	0.40	0.39
2	0.26	0.24	0.23	0.55	0.53	0.51
3	0.23	0.22	0.21	0.63	0.62	0.60

TABLE II
CENTER AND RADII FOR APPROXIMATED POWER CONTOURS IN Γ

α	Center	x-radius			y-radius		
(dB)		N=4	N=6	N=8	N=4	N=6	N=8
0	-0.03	0	0	0	0	0	0
0.5	-0.02	0.22	0.19	0.17	0.28	0.27	0.27
1	-0.01	0.31	0.27	0.25	0.40	0.39	0.37
2	0	0.44	0.4	0.37	0.55	0.53	0.52
3	0.01	0.55	0.50	0.47	0.65	0.63	0.62

C. Construction of Approximated Contours for Steep Knee Devices

For the approximation of contours when N is large, for example, around 24 for GaAs devices, ellipses can still be used for power contours. The center and the axis-radii, indicated in Table III, have been extracted graphically.

Efficiency contours for $N = 24$, as can be seen in Fig. 4, can be approximated combining a partial ellipse (on the left hand) and a partial circle (on the right hand), whose centers and radii are reported in Table IV, and have been graphically approximated.

TABLE III

CENTER AND RADII FOR APPROXIMATED POWER CONTOURS IN Γ FOR $N = 24$ (OR SIMILAR STEEP KNEE APPROXIMATION)

α (dB)	Center	x-radius	y-radius
0	-0.022	0	0
0.5	-0.01	0.11	0.25
1	0	0.175	0.35
2	0.008	0.288	0.495
3	0.01	0.395	0.595

TABLE IV

CENTER AND RADII FOR APPROXIMATED EFFICIENCY CONTOURS IN Γ FOR $N = 24$ (OR SIMILAR STEEP KNEE APPROXIMATION)

α (dB)	Center Ell.	x-radius	y-radius	Center Circ.	Radius
0	0.07	0	0	0	0
0.5	0.03	0.11	0.25	0.105	0.265
1	0.04	0.175	0.35	0.13	0.37
2	0.008	0.288	0.5	0.14	0.52
3	0.192	0.55	0.625	-	-

D. Guidelines for Contours Drawing

Following the results of Sections II and III, a procedure for contours drawing can be identified as follows.

1) Identify N by analyzing the output I–V characteristics from pulsed I–V or fan diagram measurements.
2) Draw the normalized power/efficiency contours using the equations of Section II or the tabulated values of this section.
3) Denormalize the contours to the estimated R_{opt}.
4) Account for the frequency dispersion by rotating the contours on the Smith chart according to the parasitic/package definition.

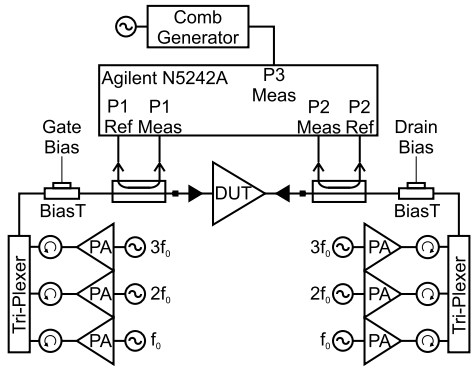
This last step is actually very important. In fact, if strong nonlinear capacitive effects are present, nonlinear embedding procedure must be applied to properly move the reference plane from the intrinsic current generator to the device tabs [17], [18].

IV. EXPERIMENTAL RESULTS

The simplified contour drawing procedure is tested and compared with load–pull characterization results for all the three devices using the Cardiff University harmonic source/load–pull setup. The measurement setup block diagram and photograph are shown in Fig. 7 consisting of a real-time, two-port, source/load–pull measurement system [19]. Active harmonic source/pull strategy is adopted, with frequency multiplexers enabling the independent behavior of the different source/load–pull harmonic sources. The use of a large-signal vector analyzer, and of a comb-generator as reference for phase realignment of harmonic components, enables the measurement of the waveforms at the device-under-test (DUT) plane [20]. The system is computerized and controlled by *ad hoc* software.

The three devices are as follows:

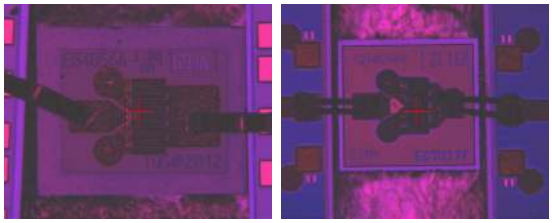
1) A 0.25-μm GaN HEMT on SiC, the TGF2023-01 from Qorvo Inc. [photograph in Fig. 8(a)], named here GaNFET1. I_{MAX} of 1.2 A. Operating at $V_{\text{DD}} = 28$ V. Estimated $R_{\text{opt}} \approx 47\ \Omega$.



(a)

(b)

Fig. 7. (a) Block diagram and (b) photograph of the adopted active source/load–pull setup.



(a) (b)

Fig. 8. Microscope photographs of (a) GaNFET1 and (b) GaAsFET devices.

2) A 0.5-μm GaN HEMT on SiC, named here GaNFET2. I_{MAX} of 0.72 A. Operating at $V_{\text{DD}} = 20$ V. I_{MAX} of 0.34 A. Operating at $V_{\text{DD}} = 10$ V. Estimated $R_{\text{opt}} \approx 58\ \Omega$.
3) A 0.35-μm GaAs pHEMT, the TGF2022-06 from Qorvo [photograph in Fig. 8(b)], named here GaAsFET. Estimated $R_{\text{opt}} \approx 58\ \Omega$.

It has to be noticed that, while GaNFET1 and GaAsFET are both based on commercial available processes, GaNFET2 is based on a research-driven process.

Fan diagram measurements [12] on the devices are shown in Fig. 9, together with the selected $k()$ functions with $N = 4$, $N = 6$, and $N = 24$ for the GaNFET1, GaNFET2, and GaAsFET case, respectively.

The GaNFET1 device has been measured at 3 GHz, with drain bias voltage of 28 V and quiescent current of 15 mA. The GaNFET2 device has been characterized at 2 GHz,

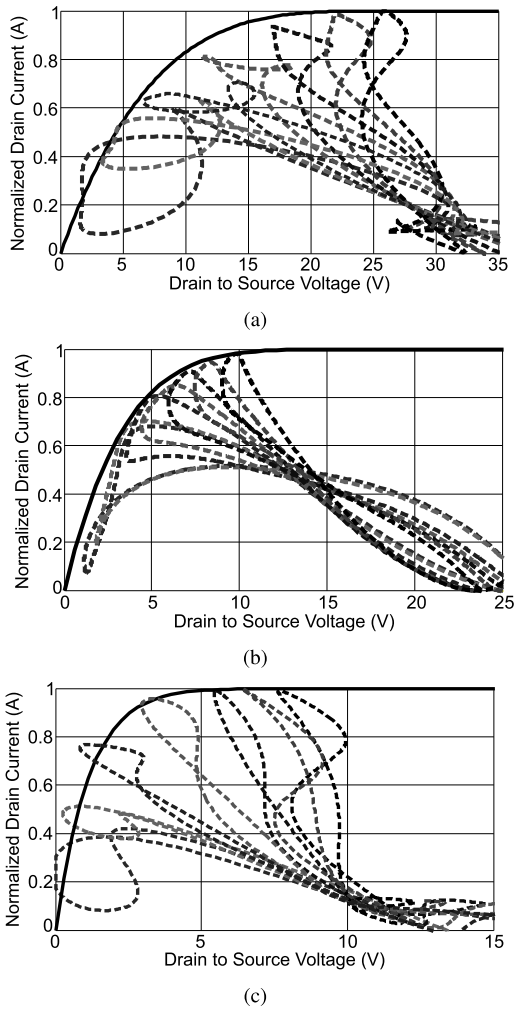


Fig. 9. Measured fan diagrams (dashed) for the GaN (a) device 1, (b) device 2, and (c) GaAs device, with adopted $k()$ functions (solid) with (a) $N = 4$, (b) $N = 6$, and (c) $N = 24$.

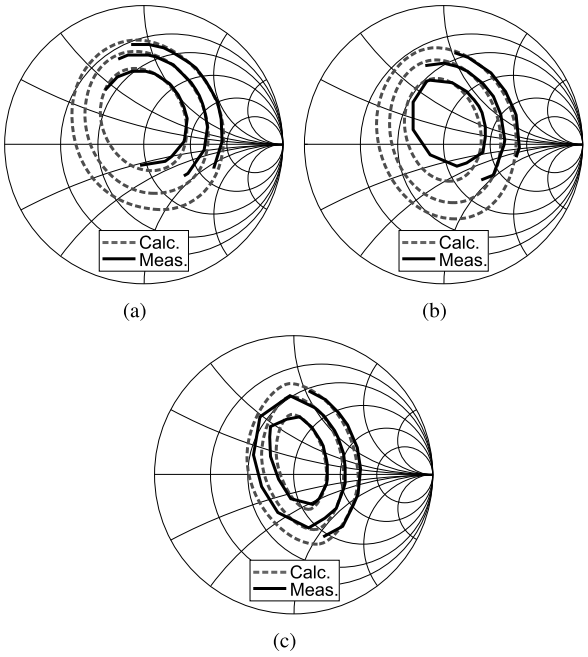


Fig. 10. Output power contours for the (a) GaNFET1, (b) GaNFET2, and (c) GaAsFET devices. Comparison between measurements (black solid) and calculated (gray dashed). Contour step: 1 dB.

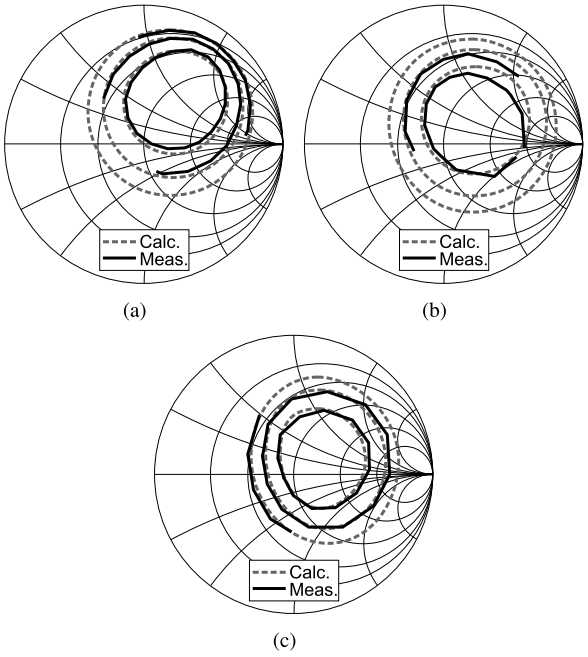


Fig. 11. Efficiency contours for the (a) GaNFET1, (b) GaNFET2, and (c) GaAsFET devices. Comparison between measurements (black solid) and calculated (gray dashed). Contour step: 1 dB.

with drain bias voltage of 20 V and quiescent current of 5 mA. The GaAsFET has been characterized at 2 GHz with drain bias of 10 V, 10 mA. A constant input drive, corresponding to roughly 3-dB compression at the optimum power load, is applied. For a proper comparison with the theory, the second and third harmonics are shorted on the device terminals. For the GaNFET1 device, the maximum measured output power is 5.4 W, while the maximum efficiency is 63%, reasonably in agreement with the estimation provided by Fig. 6, from which 5 W and 65% are expected, respectively. The intrinsic optimum load for output power is around 55 Ω, slightly higher than the estimated value. For the GaNFET2, the maximum measured output power and efficiency are 2.4 W and 58%, respectively. The output power is in good agreement with Fig. 6, that estimates 2.5 W, while the efficiency is lower than expected, probably related to the immaturity of the process. In this case, the measured intrinsic optimum load for output power is 55 Ω, very close to the expected 51 Ω. Regarding the GaAs device, the maximum measured output power and efficiency are 0.72 W and 72%, respectively, again in good agreement with Fig. 6, that estimates 0.7 W and 74%, respectively. In this case, the measured intrinsic optimum load for output power is around the expected 58 Ω. Figs. 10 and 11 show the measured output power and efficiency contours compared with the contours estimated using the equations of Section II. The calculated contours are moved to the extrinsic plane by assuming an equivalent output capacitor $C_{\text{out}} = 0.43$ pF, $C_{\text{out}} = 0.4$ pF, and 0.3 pF for the GaNFET1, GaNFET2, and GaAsFET devices, respectively. Figs. 10 and 11 demonstrate good agreement between the calculated power/efficiency

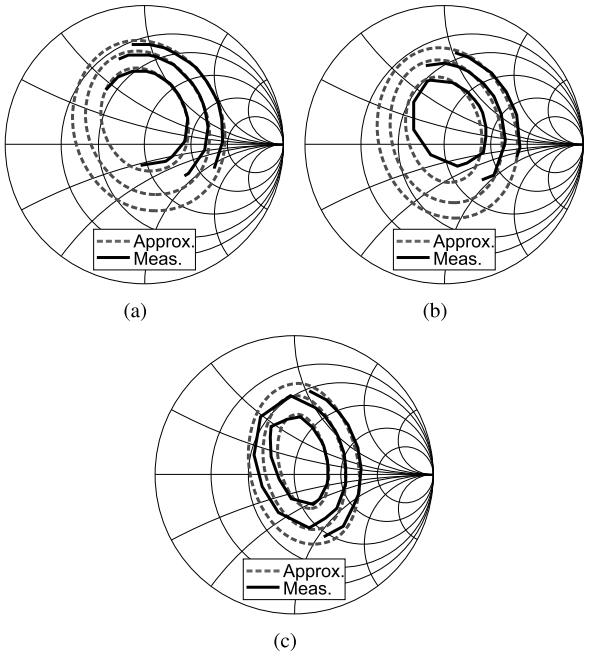


Fig. 12. Output power contours for the (a) GaNFET1, (b) GaNFET2, and (c) GaAsFET devices. Comparison between measurements (black solid) and approximated (gray dashed). Contour step: 1 dB.

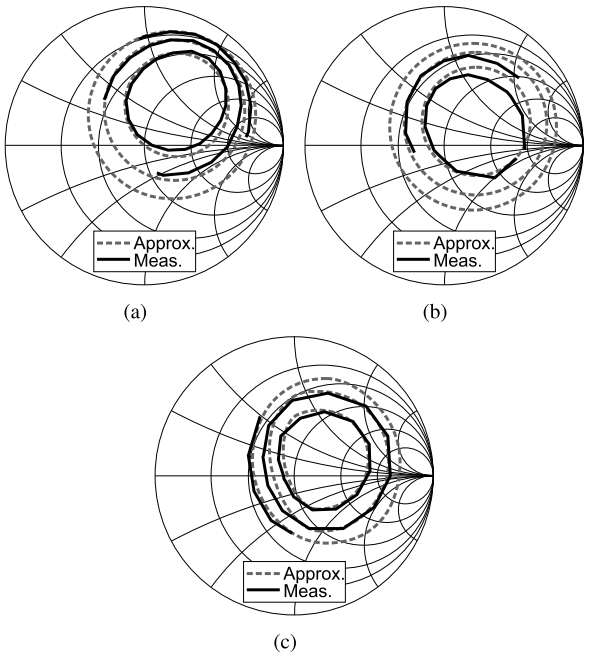


Fig. 13. Efficiency contours for the (a) GaNFET1, (b) GaNFET2 and (c) GaAsFET devices. Comparison between measurements (black solid) and approximated (gray dashed). Contour step: 1 dB.

contours, shifted to the external device plane using the equivalent capacitances, and the measured ones. The reflection coefficient error between the measured and computed contours is always lower than -19 dB.

Similarly, Figs. 12 and 13 compare the measured contours with the ones constructed using the approximated shapes of the tables of Section III. As can be seen, the approximated contours show good agreement with the measured ones, and the error of the reflection coefficient is always lower than -19 dB.

V. Conclusion

In this paper, a novel and simple method to estimate power and efficiency contours in microwave power transistors has been proposed. Closed-form equations for power and efficiency in saturation regime, using a polynomial approximation of the device's output characteristics, have been derived. While any contour level can be obtained through the solution of the proposed equations, approximated contours have also been proposed based on simple shapes as circles and ellipses. Center and radii at some significant contour levels, for devices exhibiting either a smooth or a steep knee, are tabulated for a fast reference. The contour drawing procedure does not require, at least in principle, microwave large-signal measurements, and represents a useful tool for power amplifiers design.

References

[1] P. A. Blakey and E. M. Johnson, "Generalized Kushner analysis of RF power amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 2. Jun. 1999, pp. 521–524.

[2] J. P. Mondal, "Frequency normalization of constant power contours for MESFETs," *IEEE Trans. Microw. Theory Techn.*, vol. 36, no. 6, pp. 1107–1110, Jun. 1988.

[3] S. C. Cripps, "A theory for the prediction of GaAs FET load–pull power contours," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 1983, pp. 221–223.

[4] H. Kondoh, "FET power performance prediction using a linearized device model," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 2. Jun. 1989, pp. 569–572.

[5] P. Colantonio, F. Giannini, E. Limiti, and A. Ticconi, "Prediction of PA optimum load by small signal parameters," in *Proc. Int. Workshop Integr. Nonlinear Microw. Millim.-Wave Circuits*, Jan. 2006, pp. 183–186.

[6] S. Hauptmann and F. Ellinger, "Optimized transistor output power—Extending Cripps' loadline method to cascode stages," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 8, pp. 2017–2023, Aug. 2011.

[7] J. C. Pedro and L. C. Nunes, "Efficiency dependence on the load-pull ratio of a Doherty PA," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–4.

[8] J. Pedro, L. Nunes, and P. Cabral, "A simple method to estimate the output power and efficiency load–pull contours of class-B power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1239–1249, Apr. 2015.

[9] J. Moon, J. Kim, J. Kim, I. Kim, and B. Kim, "Efficiency enhancement of Doherty amplifier through mitigation of the knee voltage effect," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 1, pp. 143–152, Jan. 2011.

[10] P. Colantonio, F. Giannini, R. Giofre, and L. Piazzon, "Increasing Doherty amplifier average efficiency exploiting device knee voltage behavior," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 9, pp. 2295–2305, Sep. 2011.

[11] J. H. Qureshi *et al.*, "A 90-W peak power GaN outphasing amplifier with optimum input signal conditioning," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 8, pp. 1925–1935, Aug. 2009.

[12] C. Roff *et al.*, "Analysis of DC–RF dispersion in AlGaN/GaN HFETs using RF waveform engineering," *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 13–19, Jan. 2009.

[13] F. H. Raab, "Class-E, Class-C, and Class-F power amplifiers based upon a finite number of harmonics," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 8, pp. 1462–1468, Aug. 2001.

[14] M. Roberg and Z. Popovic, "Analysis of high-efficiency power amplifiers with arbitrary output harmonic terminations," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 8, pp. 2037–2048, Aug. 2011.

[15] S. C. Cripps, "Pulling up [microwave bytes]," *IEEE Microw. Mag.*, vol. 9, no. 6, pp. 40–48, Dec. 2008.

[16] S. C. Cripps, P. J. Tasker, A. L. Clarke, J. Lees, and J. Benedikt, "On the continuity of high efficiency modes in linear RF power amplifiers," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 10, pp. 665–667, Oct. 2009.

[17] A. Raffo, F. Scappaviva, and G. Vannini, "A new approach to microwave power amplifier design based on the experimental characterization of the intrinsic electron-device load line," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 7, pp. 1743–1752, Jul. 2009.
[18] F. Vanaverbeke, W. D. Raedt, D. Schreurs, and M. V. Bossche, "Real-time non-linear de-embedding," in *Proc. Microw. Meas. Conf. (ARFTG)*, Jun. 2011, pp. 1–6.
[19] V. Camarchia, V. Teppati, S. Corbellini, and M. Pirola, "Microwave measurements. Part II—Non-linear measurements," *IEEE Instrum. Meas. Mag.*, vol. 10, no. 3, pp. 34–39, Jun. 2007.
[20] V. Teppati, A. Ferrero, V. Camarchia, A. Neri, and M. Pirola, "Microwave measurements—Part III: Advanced non-linear measurements," *IEEE Instrum. Meas. Mag.*, vol. 11, no. 6, pp. 17–22, Dec. 2008.

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