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A reconfigurable cryogenic platform for the classical control of quantum processors

Harald Homulle,[1] Stefan Visser,[1] Bishnu Patra,[1] Giorgio Ferrari,[2] Enrico Prati,[3] Fabio Sebastiano,[1] and Edoardo Charbon[1,a)]
[1]*QuTech, Delft University of Technology, 2628CD Delft, The Netherlands*
[2]*Politecnico di Milano, 20133 Milan, Italy*
[3]*Istituto di Fotonica e Nanotecnologie, 20133 Milan, Italy*

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The implementation of a classical control infrastructure for large-scale quantum computers is challenging due to the need for integration and processing time, which is constrained by coherence time. We propose a cryogenic reconfigurable platform as the heart of the control infrastructure implementing the digital error-correction control loop. The platform is implemented on a field-programmable gate array (FPGA) that supports the functionality required by several qubit technologies and that can operate close to the physical qubits over a temperature range from 4 K to 300 K. This work focuses on the extensive characterization of the electronic platform over this temperature range. All major FPGA building blocks (such as look-up tables (LUTs), carry chains (CARRY4), mixed-mode clock manager (MMCM), phase-locked loop (PLL), block random access memory, and IDELAY2 (programmable delay element)) operate correctly and the logic speed is very stable. The logic speed of LUTs and CARRY4 changes less then 5%, whereas the jitter of MMCM and PLL clock managers is reduced by 20%. The stability is finally demonstrated by operating an integrated 1.2 GSa/s analog-to-digital converter (ADC) with a relatively stable performance over temperature. The ADCs effective number of bits drops from 6 to 4.5 bits when operating at 15 K. [http://dx.doi.org/10.1063/1.4979611]

I. INTRODUCTION

In a fault-tolerant quantum computing system based on either electron or hole spin in semiconductors, or superconductors, each virtual qubit generally operates at sub-1 K temperatures and it requires a classical control loop capable of reading its state and controlling it based on a (localized) decision. To be effective, such error-correcting loops need to perform a complete correction cycle faster than the virtual qubit coherence time, which, depending on the qubit technology, can vary from ms to μs.[1–12] This implies that future classical control systems need to be capable of measuring, calculating, and correcting a virtual qubit error within this time frame to deploy error free logical qubits. Large scale systems require more data to be processed in the same time frame, therefore demanding physically small control units capable of massively parallel processing. The hardware infrastructure will most likely be implemented in micro-architectures operating at cryogenic temperatures, so as to ensure proximity to qubits and thus compactness. Moreover, to avoid time- and energy-consuming cooling cycles, micro-architectures supporting error correction should be programmable and/or reconfigurable. To meet the reconfigurability requirement, the obvious choice is an FPGA (field-programmable gate array) or CPLD (complex programmable logic device) fabricated in a deep-submicron (DSM) CMOS process (see Table I for the definitions of acronyms used in this paper), due to its density, versatility, and full compatibility with standard CMOS circuits. The use of standard CMOS processes can leverage a mature infrastructure that is cheap, scalable, and likely to continue improving for several more decades.[13]

FPGAs have been proposed as the digital controller at room temperature for error-correction due to parallelism (faster decision times), small system size, and possible integration.[14–17]

DSM CMOS circuits have been known to operate at deep cryogenic temperatures, down to several hundreds of mK.[18–23] However, operating semiconductor devices at deep cryogenic temperatures is a challenge, due to freeze-out, non-idealities in transistor I-V characteristics, and increased mismatch.[24] While freeze-out effects at 4 K are less problematic in DSM CMOS technologies due to the high levels of doping, MOS transistors I-V characteristics exhibit a so-called "kink," which causes elevated current levels at high V_{DS}, due to a reduction in the transistors threshold voltage V_t, caused by the self-polarization of the bulk generated current by the impact ionization at the drain.[25] Furthermore, hysteresis in the drain current when sweeping the drain voltage upwards or downwards is increased at cryogenic temperatures. Both effects can be clearly observed for the measured DSM CMOS transistors shown in Figure 1.

To overcome these limitations, we opted for a fully digital approach by way of FPGAs. The redesign of analog circuits adjusted to cryogenic conditions can (at least partially) be avoided, since the large majority of the required

a)Electronic mail:e.charbon@tudelft.nl

TABLE I. Definition and description of the various abbreviations and acronyms as used in the text.

Class	Abbreviation	Definition	Description
Device	ASIC	Application specific integrated circuit	
	CMOS	Complementary metal-oxide-semiconductor	
	ADC	Analog-to-digital converter	
	DAC	Digital-to-analog converter	
	TDC	Time-to-digital converter	
	CPLD	Complex programmable logic device	
	FPGA	Field-programmable gate array	
	MUX	Multiplexer	
	DEMUX	De-multiplexer	
FPGA block	LUT	Look-up table	Programmable element to function as combinatorial logic gate
	CARRY4	Carry chain element	Ripple counter dedicated hardware block
	BRAM	Block random access memory	RAM dedicated hardware block
	MMCM	Mixed-mode clock manager	Digital clock manager to provide the FPGA with different clocks and phases
	PLL	Phase-locked loop	Subset of MMCM functionality
	IDELAYE2	Input delay element	Programmable hardware block capable of delaying the signal
	DSP48 $\times 10^1$	Digital signal processing element	Dedicated hardware block for signal operation with adders, multipliers and comparators
Communication	IO	Input-output	General input-output interface
	LVDS	Low-voltage differential signalling	Differential signalling for high frequencies with low voltage swing to reduce noise and interference
	UART	Universal asynchronous receiver/transmitter	Basic (low speed) communication protocol
	JTAG	Joint test action group	FPGA programming interface with daisy chained structure
	GPT	General purpose transceiver	Dedicated high-speed communication interface
Other	ESR	Effective series resistance	Resistive loss of a capacitor
	ESL	Effective series inductance	Inductive loss of a capacitor
	ENOB	Effective number of bits	Indication of the performance of ADCs
	DNL	Differential non-linearities	Step-wise deviation from ideal ADC, DAC, TDC transfer curve
	INL	Integral non-linearities	Integrated deviation from ideal ADC, DAC, TDC transfer curve

components can be implemented as a digital block. FPGAs have been shown to operate at deep cryogenic temperatures and have been proposed as the digital controller in the error-correcting control loop.[26–28] Implementing an FPGA at cryogenic temperatures will satisfy the requirements in terms of system reconfigurability and physically close operation to the qubits, besides the benefits already shown at room temperature. The Spartan 3, Spartan 6, and Artix 7 FPGAs by Xilinx were shown to operate at 4 K;[26,27] however the limits of operability at 4 K are still largely unknown. In this study, we focus on the characterisation of individual logic blocks inside the FPGA to an unprecedented level granularity and completeness, with measurements in the complete 300 K–4 K range. Our work suggests that future cryogenic FPGA firmware can be better optimised with those results and potentially profit from higher logic speeds and more stable operation.

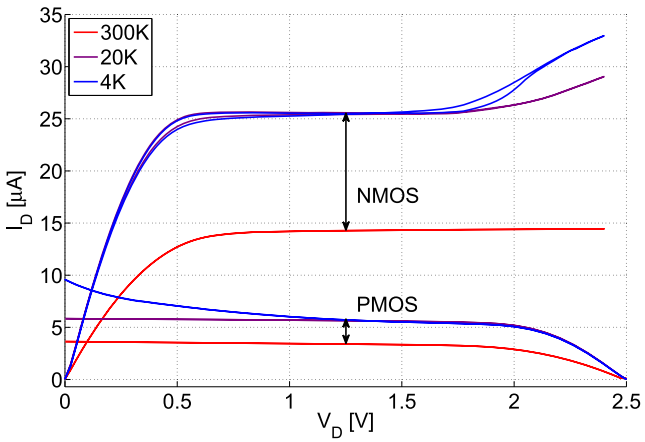

FIG. 1. I-V characteristics (I_D versus V_D at a constant V_{GS} of 1.5 V) of PMOS and NMOS transistors fabricated in a standard 0.16 μm CMOS technology, when operating at various temperatures from 300 K to 4 K. A significant increase in hysteresis of the drain current can also be seen at deep cryogenic temperatures.

We explore the regime of operability of a commercial FPGA (Artix 7 from Xilinx) to enable a full error-correction loop for fault-tolerant operation of solid-state qubits. The resulting infrastructure is scalable, as it can be extended to multiple qubit control channels, efficiently integrated in an FPGA and operating at low power. In order to implement such a platform, extensive characterisation of the FPGA performance in cryogenic conditions was carried out, demonstrating the possibility of using the FPGA at cryogenic temperatures for the error-correction control loop.

II. AN FPGA BASED CONTROL PLATFORM

The architecture of the control electronics of quantum devices is shown in Figure 2; it comprises multiplexers and demultiplexers, in close proximity to or integrated with the qubits, amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), oscillators, down- and up-converting mixers, and general-purpose digital logic. In this work, we mainly focus on the implementation of the digital controller, being the FPGA. Furthermore, the FPGA can host the ADCs, which are detailed later on, and DACs.

The error-correction loop would be implemented as follows: first the analog signals coming from the physical qubits are converted to digital codes at the interface with the FPGA. These data are processed digitally to measure the virtual qubit states and to synthesize the appropriate correction. To avoid further unnecessary signal conversions, and thus maximizing signal-to-noise ratio (SNR) and signal integrity, control signals are generated directly by the FPGA, whenever possible, or by DACs.

Operating an FPGA almost 250 K below its standard operating range is not trivial and it comes with several challenges.

When reducing the temperature, power dissipation budgets become increasingly stricter, down to a few watts at 4 K, due to limitations in refrigeration technologies. It imposes care in designing custom integrated circuits, and even more so in FPGAs. To fully characterize the FPGA performance, the platform is first tested in liquid helium directly, thus maximizing cooling power if compared to closed-loop refrigeration.

Next, we consider the physical implementation of the platform, needing *ad-hoc* printed circuit boards (PCBs) dedicated to cryogenic conditions that host robust passive components and connectors that can reliably survive several cooling cycles without performance degradation. In our design, we used a minimal number of discrete components certified for operation over a temperature range, much wider than industrial and military standards.

The most critical challenge is the operating condition and the corresponding behaviour of the FPGA. Especially for high performance circuits, such as time-to-digital converters (TDCs) and ADCs, the FPGA behaviour has to be well understood.

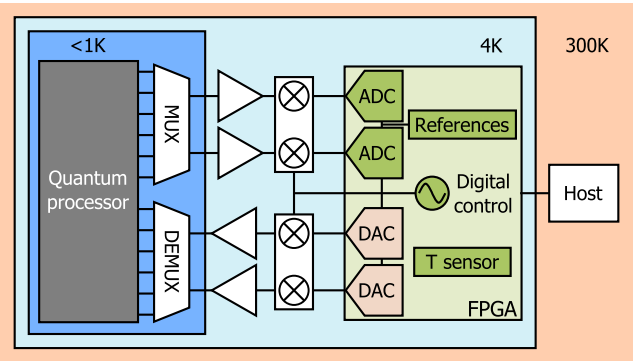

FIG. 2. Cryogenic control platform implementing the infrastructure supporting error-correcting micro-architectures. An all-digital implementation of the main components and integration inside the FPGA is shown. Although in theory both red and green components can be integrated, in the remainder of the paper we focus on the green parts.

III. CRYOGENIC FPGA DESIGN AND TEST

A small PCB with a Xilinx Artix 7 FPGA as the sole active component was designed for cryogenic testing. The PCB is shown in Figure 3. Besides the FPGA, various passive components, most noticeably the decoupling capacitors, are present on board.

The PCB was fabricated with standard FR4 as dielectric material and consists of 4 metal layers (one ground plane and three signal/power planes). The FPGA (Xilinx Artix 7 series), the high-frequency connectors, and some resistors were placed on the front side. The back-side hosts only decoupling capacitors. A detailed list of the components on the PCB can be found in the Appendix.

In particular, we chose the FPGA XC7A100T-2FTG256I due to its small size, low power consumption (28 nm process node), and industrial grade. Capacitors were chosen after selecting the best materials for cryogenic conditions and their availability in various capacitor values. Low permittivity materials, such as ceramic NP0/COG materials, are generally well behaved at 4 K.[29,30] However, since they are only available up to 0.47 μF format, tantalum polymer or high permittivity ceramic capacitors were used for bigger capacitances. Results for some of the used tantalum and ceramic capacitors are shown in Figure 4. Capacitance drops as much as 90% and the effective series resistance (ESR) increases as much as 40× for the high permittivity ceramic capacitor (4.7 μF). Tantalum capacitors are more stable (47, 100, and 330 μF), but still lose up to 20% of their room temperature capacitance. Our results suggest that for high value capacitors (>0.47μF), tantalum polymer might be a more stable alternative with respect to ceramic capacitors.

As the FPGA is powered over long cables (over 4 m to be inserted into a liquid helium dewar, see the Appendix for details), special care was taken in minimizing the total capacitors effective series resistance and inductance (ESR and ESL). ESR and ESL affect the capacitors' ability to quickly source and sink current, especially in fast current switching applications. Also for other capacitor types, besides the ones noted before, the capacitance can drop significantly at cryogenic temperatures, and the ESR can increase up to 1.000×,[29] stressing the importance of selecting the appropriate capacitor types for operation in a cryogenic environment.

Cryogenic tests were executed using a dip-stick (as described in the Appendix) at various temperatures ranging

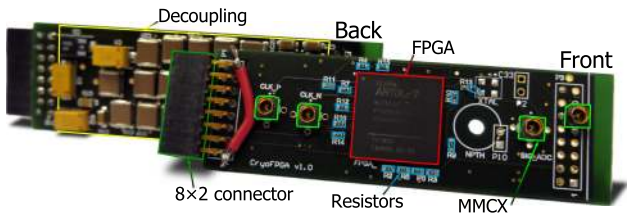

FIG. 3. Cryogenic FPGA PCB (25 × 75 mm) with the most important components highlighted. A simplified overview of the components mounted on the board is presented in Table V.

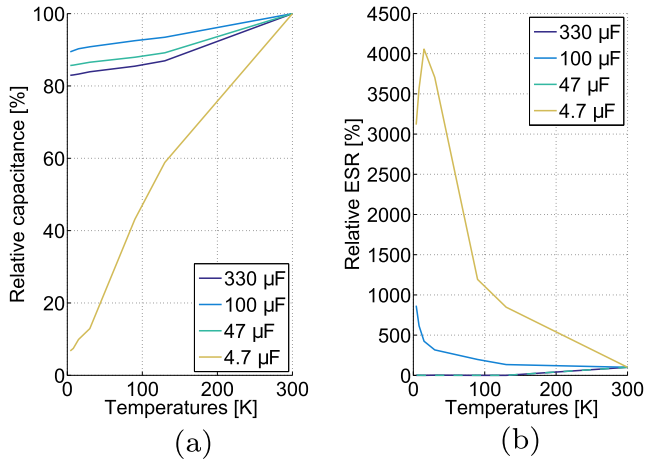

FIG. 4. (a) Capacitances relative to their room temperature values for various capacitors. (b) Corresponding relative ESR.

from 4 K to 300 K. The sample is immersed directly into liquid helium or helium vapours in order to achieve a fast cooling process and a relatively high cooling power.[31] The dipstick houses 16 RG174/U coaxial wires for low frequencies, 4 coaxial wires with MMCX connectors for higher frequencies, and several DC wires for power sourcing and temperature read-out.

IV. CRYOGENIC FPGA RESULTS

A. FPGA characterisation

Modern FPGAs, such as the Artix 7, integrate a variety of different building blocks, from simple look-up tables (LUTs) to advanced clock managers (MMCM).[32] We highlighted the main FPGA building blocks in Table I together with a short description of their functionality. In order to test these building blocks, a test procedure was defined to sequentially test the most vital FPGA components. As each component requires a different test procedure, different VHDL programs were designed and programmed on the FPGA through the JTAG interface. It should be noted that programming was working over the complete temperature range, allowing us to test the different components separately in the cryogenic environment, without the need for time consuming cooling/heating cycles. In Table II, an overview of the main FPGA building blocks is given together with the performance change when operating at 4 K and the executed test protocol. All these building blocks are functional and their performance is comparable at room temperature.

Figure 5 shows that the delay change of look-up tables and carry chains is less than 5%. While this is negligible in most applications, the change in logic speed is significant for the performance of both ADC and TDC.

Therefore the main structure of those two circuits, i.e., the carry chain (used as delay line) is characterized more extensively over both FPGA internal voltage and temperature. Figure 6 shows the average delay per carry block versus the FPGA voltage for 300 K and 4 K. The delay change is significantly larger over the voltage range than over temperature, again signifying the performance stability over temperature. However, it also shows that the voltage must be very stable in order to achieve TDCs and ADCs that can be properly calibrated.

A second observation is that the voltage range, in which the FPGA operates, changes over temperature. The range is significantly wider at room temperature (0.85 V–1.1 V) than the specified range (0.95 V–1.05 V). At low temperature, it reduces significantly on both ends (0.92 V–1.02 V).

The IOs of the FPGA are studied for their output drive strength in standard LVCMOS25 mode at various signal frequencies and temperatures. In Figure 7, the IOs can be seen to be operable at significantly higher frequencies compared to the FPGAs rated maximum of 450 MHz. Although the IOs maximum frequency was found to be slightly higher at cryogenic temperatures (710 MHz versus 675 MHz), the increase of output swing is more significant with almost

TABLE II. Overview of the working elements inside the CryoFPGA operating around 4 K.

Module	Functional	Test	Performance with respect to RT
IOs	✓	Output swing tested at different frequencies	Increased drive strength
LVDS	✓	Differential clock provided from RT to clock the FPGA	
LUTs	✓	LUTs connected to form oscillator of approximately 100 MHz at RT	Propagation delay changes <5%, jitter increases <15% (11.8–13.5 ps)
CARRY4	✓	Carry chains connected to form oscillator of approximately 100 MHz at RT	Propagation delay changes <2%, jitter increases <3% (11.5–111.8 ps)
BRAM	✓	Transfers of 8 kB (write and read)	No corruption in 10 test sets of 80 kB
MMCM	✓	100 MHz differential input clock multiplied by 10 and divided by 20–50 MHz single ended output	Jitter reduction of roughly 20% (11.4–8.9 ps)
PLL	✓	100 MHz differential input clock multiplied by by 20–50 MHz single ended output	Jitter reduction of roughly 20% (12.2–9.7 ps)
IDELAYE2	✓	IDELAYE2 elements connected to form a tunable oscillator (output frequency variable 13-70 MHz)	Delay change of up to 30%, jitter increase up to 50%
DSP48 $\times 10^1$	✓	Random calculations with additions, subtractions, and multiplications	No corruption in 400 random calculations
Temperature diode	✓	Operating range 4 K–300 K	

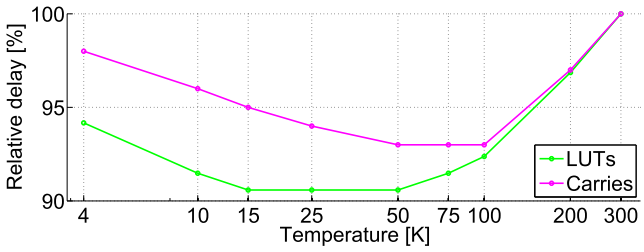

FIG. 5. Relative propagation delay for both LUTs and CARRY4 building blocks over temperature.

70% higher observed output voltage at 450 MHz. The maximum operating frequency, before errors appear, of the internal FPGA logic largely depends on the logic circuit. For a simple counter circuit of 12 bits, the maximum operating frequency was found to be 650 MHz at both room and cryogenic temperatures.

To study self-heating effects of the FPGA, first the internal FPGA diode was calibrated against a LakeShore DT-670 reference diode. The result of this calibration is shown in Figure 8 and was obtained while cooling the switched-off FPGA down, while constantly measuring both diodes.

With the obtained diode calibration data, the FPGAs self-heating was studied with a circuit capable of sweeping the power consumption of the FPGA. The sweep was repeated at different temperature levels as shown in Figure 9(a). A significant difference is observed in the response at the different temperatures. First, the idle power consumption is reported in Table III and can be seen to be increased from 83 mW at 300 K to 228 mW at 4 K. Since leakage is expected to decrease at lower temperatures, the increase of idle power is attributed to malfunctions of the support bias circuitry.

Second, a change in logic efficiency occurs. Namely, the average power per transition decreases and the power consumption starts to scale non-linearly, while lowering the temperature. The average energy used per LUT decreases from 32 to 21 μW, i.e., the energy consumed per transition in a LUT decreases from 23 to 15 pJ. This implies a decrease in dynamic power consumption of over 30%.

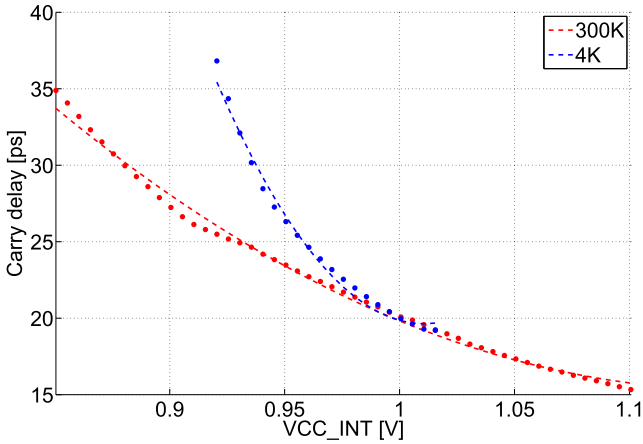

FIG. 6. Delay of the carry elements in the carry chain versus FPGA voltage (VCC_INT) for multiple temperatures.

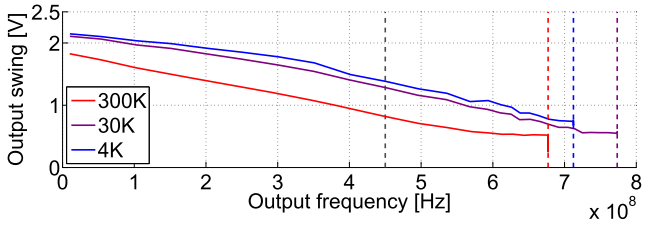

FIG. 7. IO output swing (LVCMOS25) versus output signal frequency for various temperatures. Indicated are the maximum achieved IO operating frequencies and the rated maximum of 450 MHz. The IOs were loaded with 4 m of coaxial cable into a high-impedance.

As shown in Figure 9(b), the FPGAs substrate temperature increases with power consumption from 4.3 K (powered off FPGA) to 17.3 K (at 1.25 W power consumption). While the die temperature is elevated due to self-heating, the environment remained stable at a temperature of 4.2 K (±0.1 K).

From the slope, we can estimate a thermal resistance of the FPGA package of 8.5 K/W, which is lower than the thermal resistance at room temperature in air (31 K/W).

B. FPGA analog-to-digital converter

One of the most important elements in the quantum error-correcting control loop is the analog-to-digital converter. Various attempts have been undertaken to optimize ASIC ADCs for cryogenic conditions, but reaching high performance is still challenging. Therefore, we opted to implement the ADC as a completely digital building block inside the FPGA. The operating principle is shown in Figure 10.[33] A high speed clock signal is output on an FPGA pin connected, through a resistor, to an LVDS capable input pin. Thanks to the resistor and the parasitic capacitance of the LVDS buffer, an *RC*-ramp is created. The conversion is based on measuring the time required for the *RC*-ramp to cross the input signal, as done in a single-slope converter. The LVDS, used as comparator, switches as soon as the ramp voltage exceeds the input voltage and the LVDS switching time is measured using a TDC.

With the use of multiclock-phase interleaving and calibration features, sampling rates, up to 1.2 GSa/s, above the clock frequency (400 MHz) are achieved. Furthermore, thanks to the calibration, the ADC performance can be better controlled over temperature, process, and voltage variations. The calibration is done in four steps. First, the TDC length is adjusted to match exactly the clock period. Second, the different TDCs

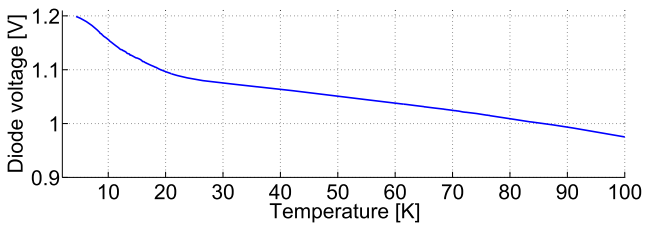

FIG. 8. FPGA diode calibration against external reference diode, both diodes biased with 10 μA. Over 3.000 measurement points were used in order to recreate the diode curve. As hysteresis of <0.5 K was present in the measurement data, the curve is averaged out between temperature decrease and increase.

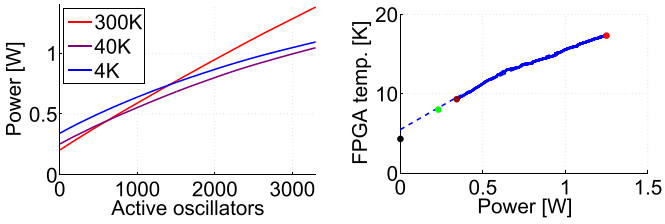

FIG. 9. (a) Power consumption of the FPGA while increasing the number of running oscillators in the FPGA fabric. (b) FPGA power consumption versus the resulting die temperature. The coloured dots indicate (left to right) powered off FPGA, idle FPGA, 0 active oscillators, and 4500 active oscillators.

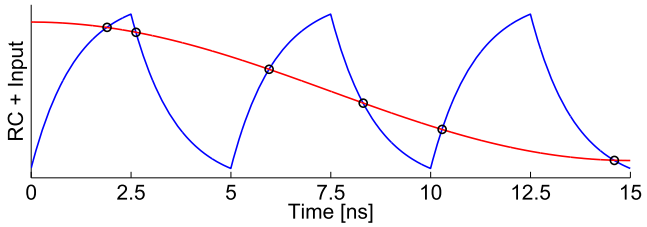

FIG. 10. Basic principle of analog-to-digital conversion in the FPGA using an *RC*-filter to create a ramp from the clock output signal. The crossings of the input and the ramp are timestamped in a TDC.

are aligned with the clock rising edge and the offsets calibrated out. Third, the *RC*-ramps are calibrated in each TDC and matched with one another. Finally, the differently phased ADCs are properly synchronized to match in the phase offset. More details on this procedure can be found in Refs. 34 and 35.

The performance of a 1.2 GSa/s ADC, created by interleaving 6 different phases of a 200 MHz clock, is summarized in Table IV and detailed in depth in Ref. 35. The FPGA is operating at a slightly elevated die temperature of 15 K, while the decoupling capacitors could not sustain the high power demand of almost 0.9 W at 4 K to reach optimal performance, i.e., store enough charge to quickly stabilize the significant current fluctuations. As the ADC is calibrated at both operating temperatures, the non linearities can be seen to be only slightly larger at cryogenic temperatures.

In Figure 11, the performance of the ADC is plotted in terms of ENOB over different signal input frequencies for both 300 K and 15 K. The ENOB is lowered by roughly 1-1.5 bit at cryogenic temperatures due to decreased decoupling stability and increased IDELAYE2 jitter. The effect can be mainly attributed to the decreased single shot resolution (or increased ADC jitter), which is increased from 1.1 LSB (1σ) at 300 K to 2.3 LSB at 15 K.[35]

Although one bit has to be sacrificed while going down towards 15 K, the performance is still in line with the requirements for the qubit control loop, which demands a high sampling rate rather than a high voltage resolution.

C. Discussion

Creating ADCs and TDCs in an FPGA is not trivial, especially at cryogenic temperatures. However, we showed their feasibility when good design practices and extensive calibration techniques are used as an integral part of the firmware. Among the components required in the control platform (as discussed in Section II) we focused on one of the most complex features, i.e., integrating a high performance ADC operating over a large temperature range.

The other components that, in our view, can be integrated inside the FPGA are digital control logic, digital-to-analog converters, temperature sensors, and oscillators.

The temperature can be monitored using the internal temperature-measuring diode after calibration with an accurate reference sensor.

GHz-oscillators, required for up-/down-mixing the baseband analog signal, can be implemented in FPGAs. Although the standard IOs of the FPGA cannot operate beyond roughly 650 MHz in the Artix 7, the general purpose transceivers (GPT) can in theory be used to generate clock signals as high as 12.5 GHz (e.g., on Xilinx Kintex 7 devices), which is in the perfect range to operate most qubits.

As noted in Section II, also DACs can be integrated in the FPGA, with the use of TDCs and the use of ultra-fast pulse-width modulation techniques, so that the (baseband) error-correcting control loop can be closed using only the FPGA.

For integration of the cryogenic FPGA in the control loop, there are still several optimizations required. The main focus of future work is the reduction of the FPGAs power consumption, by circuit optimization, operating voltage reduction, and potential replacement of the current FPGA with the one rated at lower power consumption. The use of FPGAs as part of the control loop has already been demonstrated at room temperature.[10,36] Both a reduction in error-correction decision time and the feasibility of performing more complex analysis have been achieved with the use of FPGAs as part of the measurement system.

TABLE III. Idle FPGA power consumption at different temperatures. Bias voltages for VCC_INT, VCC_AUX, and VCC_O are 1, 1.8, and 2.5 V, respectively.

Temperature (K)	VCC_INT (mA)	VCC_AUX (mA)	VCC_O (mA)	Power consumption (mW)
300	24	26	5	83
40	19	69	4	153
4	20	110	4	228

TABLE IV. Summary of calibrated ADC performance at 300 K and 15 K. The results are achieved after merging the 6 phase interleaved channels.

Temperature (K)	300	15
Sampling rate (MHz)	1.2 GSa/s	1.2 GSa/s
Input range (V)	(0.9-1.6)	(0.9-1.6)
ENOB (1 MHz) (bits)	6.0	4.5
DNL (LSB)	(−0.75 1.04)	(−0.85 1.04)
INL (LSB)	(−0.36 0.52)	(−0.68 0.77)

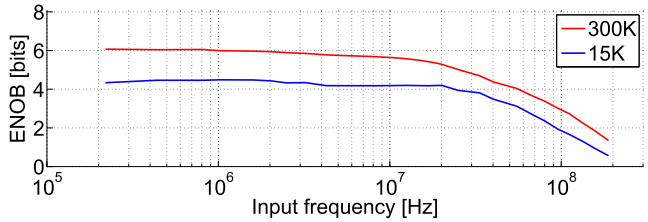

FIG. 11. Effective number of bits versus input signal frequency at room temperature and 15 K for the FPGA ADC sampling with 1.2 GSa/s. More details can be found in Ref. 35.

V. CONCLUSIONS

A cryogenic, all-digital FPGA based control platform for error-correcting loops has been proposed. The FPGA is operating over a large temperature range from 4 K up to 300 K, without significant loss in performance. Logic speeds are very stable with changes of less than 5%. Also all other major components (MMCM, PLL, BRAM, IDELAY2) are fairly stable over the complete range.

We believe, although not all control logic can be implemented in the FPGA, a large part of the required elements to control and read both physical and virtual qubits can be implemented. The FPGA is clearly ideal to implement any digital logic, as it can be reprogrammed, in real-time even at cryogenic temperatures, without the need for time-consuming and potentially hazardous cooling cycles. So far, digital logic, analog-to-digital converters, temperature sensors, and oscillators have been shown to be working correctly in cryogenic conditions, while being integrated in the FPGA.

Creating ADCs in an FPGA is not trivial, especially at cryogenic temperatures. However, we showed their feasibility when good design practices and calibration techniques are used as an integral part of the firmware, thus paving the way toward the control of realistic fault-tolerant solid state quantum information processing.

APPENDIX: ADDITIONAL INFORMATION

In this appendix some additional information on the designed PCB and measurement setup can be found.

1. PCB design choices

The PCB was designed to embody a Xilinx FPGA from the Artix 7 series. The simplified bill of materials (BoM) can be found in Table V. In particular, the FPGA from Xilinx 7 series was chosen for its industrial grade (higher standard temperature range down to −40 °C), its low power (28 nm node), and its small size. It features over 100 k logic cells (in 16 *k* slices) and up to 170 user IOs in a small package measuring 17 × 17 mm.

TABLE V. Bill of materials (simplified) of the FPGA PCB.

Component	Manufacturer	Part
FPGA	Xilinx	XC7A100T-2FTG256I
Capacitors	Kemet	C-series (ceramic (NP0/COG, X8L))
Capacitors	Kemet	T-series (tantalum)
Capacitors	Panasonic	TQC-series (polymer)
Resistors	Panasonic	ERA-series (metal film)
Connectors	Amphenol	MMCX
Connectors	Samtec	8 × 2 female connector

TABLE VI. Connections toward the FPGA PCB.

Connector	Occupied pins	Purpose
Shields	20[a]	Ground
DC	3	Voltages (VCC_INT, VCC_O, VCC_AUX)
DC	4	External temperature sensor (DT-670)
8 × 2	4	JTAG (TDI, TDO, TMS, TCK)
8 × 2	3	UART (RX, TX, CTS)
8 × 2	5	Voltages + ground
8 × 2	2	Internal temperature diode
8 × 2	2	Debug
MMCX	2	Clock (differential)
MMCX	1	ADC input signal
MMCX	1	High frequency debug

[a]16 + 4 coaxial shields.

A detailed summary of the used connections to the FPGA board is given in Table VI. For communication, both JTAG (programming) and UART were used, occupying most of the user IO pins available on the board.

For the power supplies, additional cables were added to avoid a large *IR* drop in the shielded cables. Special care has been taken to ensure proper grounding of the complete setup, by shorting the cable shield terminals both at the instrument side (room temperature) and at the PCB side (deep cryogenic temperature).

The measurement setup is depicted in Figure 12. For the power, two power supplies from Aim-TTI Instruments (EL302RD) were used, generating 1, 1.8, and 2.5 V. Programming and communication with the FPGA was done with a Digilent JTAG controller (XUP USB-JTAG) and an UART-USB dongle (FTDI UMFT234XD), respectively. The clock signal was provided differentially from an SP605 (Xilinx Spartan 6 evaluation kit) and was set to 100 MHz. Additionally, a Rohde and Schwarz HMF2550 signal generator has been used to provide the ADC test input. For accurate temperature measurements, a Keithley source meter unit

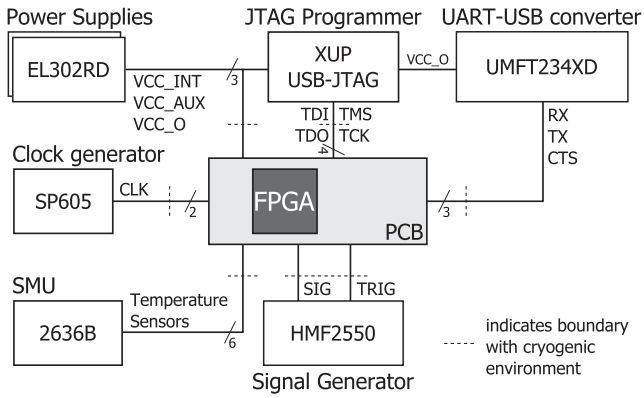

FIG. 12. Overview of the equipment used outside the cryogenic environment to control and operate the FPGA. The ground is not indicated, but is common for all equipments and the PCB.

(2636B) was added to the system. It provides a precision current bias for the FPGAs internal temperature-measuring diode and for an external reference sensor (Lake Shore Cryotronics, DT-670 silicon diode) mounted in thermal contact to the FPGA. Both diodes were biased with a current of 10 μA, and the diode voltage is read as a function of temperature.

2. Test set-up

In order to test the FPGA in deep cryogenic conditions, a setup was built which uses a dip-stick to immerse the PCB in liquid helium. A schematic cross section of the setup is shown in Figure 13. The dip-stick consists of a steel pipe (2 m), a break-out box for cables placed on the top end, and a sample holder at the low end of the pipe. The pipe limits the size of the PCB (diameter of 1.5 in.) and the number of cables. In total, 16 shielded cables (standard RG174/U coaxial wires with a 0.5 mm diameter core) are used for low frequency connections, 4 high frequency cables are connected to the MMCX, and up to 9 additional cables for the temperature sensor and power supplies. The resistance of the cables used to power the FPGA is in the order of 0.2–0.3 Ω.

As the pipe is able to move up and down through a vacuum flange, the temperature can be shifted from 4 K in the liquid phase to around 200 K in helium vapours at the top of the Dewar. As the sample is immersed in either the gas or the liquid helium, the cooling process is relatively fast and the cooling power relatively high compared to a vacuum refrigerator.

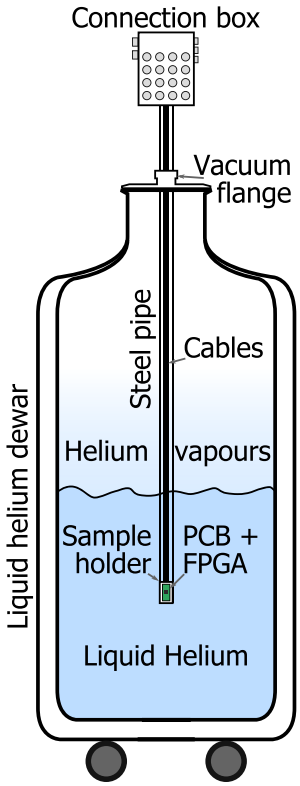

FIG. 13. Schematic depiction of our cryogenic test setup. The sample is mounted on a long steel pipe which is shifted into a helium Dewar to reach the liquid helium. The connections to the sample are made with long (standard) cables that are attached to a break-out box on the top. There are 16 shielded connections to a 8 × 2 pin header, 4 shielded connections to high frequency MMCX connectors, and up to 9 additional DC wires for a temperature sensor and the various supply voltages.

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