A Regulated Charge Pump With Small Ripple Voltage and Fast Start-Up

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***Abstract*—A regulated charge pump circuit is realized in a 3.3-V 0.13-μm CMOS technology. The charge pump exploits an automatic pumping control scheme to provide small ripple output voltage and fast start-up by decoupling output ripple and start-up time.**

The automatic pumping control scheme is composed of two schemes, an automatic pumping current control scheme and an automatic pumping frequency control scheme. The former automatically adjusts the size of pumping driver to reduce ripple voltage according to output voltage. The latter changes the pumping period by controlling a voltage-controlled oscillator (VCO). The output frequency of the VCO varies from 400 kHz to 600 kHz by controlling the input bias voltage of the VCO.

The prototype chip delivers regulated 4.5-V output voltage from a supply voltage of 3.3 V with a flying capacitor of 330 nF, while providing 30 mA of load current. The area is 0.25 mm^2 and the measured output ripple voltage is less than 33.8 mV with a 2-μF load capacitor. The power efficiency is greater than 70% at the range of load current from 1 to 30 mA. An analytical model for ripple voltage and recovery time is proposed demonstrating a reasonable agreement with SPICE simulation results.

***Index Terms*—Automatic pumping control, large load current, regulated charge pump, small ripple voltage.**

I. Introduction

In MANY semiconductor devices, such as DRAM, EEPROM, and switched-capacitor transformers, charge pumps are frequently used to provide voltage higher than a power supply because high voltage level in a charge pump is generated by transferring charge to a capacitive load, without any amplifiers or regular transformers [1]. Many charge pump approaches have focused on the design of the Dickson charge pump, such as [2]–[4], since the conventional applications have required a high voltage with only limited current drive capability. However recent applications like USB-OTG (On-The-Go) not only require a high voltage level, but also require high current drive capability [5].

According to [6], output voltage of the charge pump decreases as load current increases. The dependence prevents the charge pump from generating high voltage with high load current. To reduce the dependence, the regulated charge pump was proposed [7]. This charge pump generates constant output voltage regardless of load current by employing a clock blocking scheme blocking an input clock signal when the output voltage is higher than the required voltage. Fig. 1 shows a conceptual schematic of this charge pump. Using this scheme, constant output voltage with large load current of the charge pump can be achieved. However, large ripple voltage is incurred due to the clock blocking, especially in case of the large load current.

This paper describes a new regulated charge pump incorporating an automatic pumping control scheme to reduce ripple voltage while delivering large load current. The proposed regulated charge pump generates approximately 4.5-V output voltage and 33.8-mV ripple voltage with 30-mA load current.

In Section II, the steady state and dynamic analysis of the conventional regulated charge pump are described to develop the output ripple voltage generation processes and output voltage recovery time. In Section III, a new charge pump is proposed to reduce ripple voltage and decrease the recovery time of the output voltage. To verify the function of the proposed charge pump, the charge pump is analyzed by dynamics with state equations. Experimental results are provided and discussed in Section IV. Finally, conclusions are presented in Section V.

II. Conventional Regulated Charge Pump

In the conventional regulated charge pump, the clock blocking scheme is adopted to isolate the output voltage level from the value of a load resistor, which determines the load current. Although its average output voltage has a constant value regardless of load resistor, large output ripple voltage is generated during the pumping and blocking periods.

The operation of clock blocking is shown in Fig. 2. The output load capacitor is charged only during pumping period and discharged through the load resistor continuously. If the pumping period is much shorter than the blocking period, output ripple voltage at the load capacitor during the pumping period [4] is determined by

$$\Delta V_{\rm out} = \frac{i_{\rm pump}}{C_{\rm load} \cdot f} \tag{1}$$

where $i_{\rm pump}$ is the pumping current into the flying capacitor during the pumping and blocking periods which is equal to $i_{\rm out}$ in a steady state, $C_{\rm load}$ is the output load capacitance, and f is the switching frequency between the pumping and blocking periods.

Manuscript received December 26, 2004; revised October 4, 2005.

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Digital Object Identifier 10.1109/JSSC.2005.862340

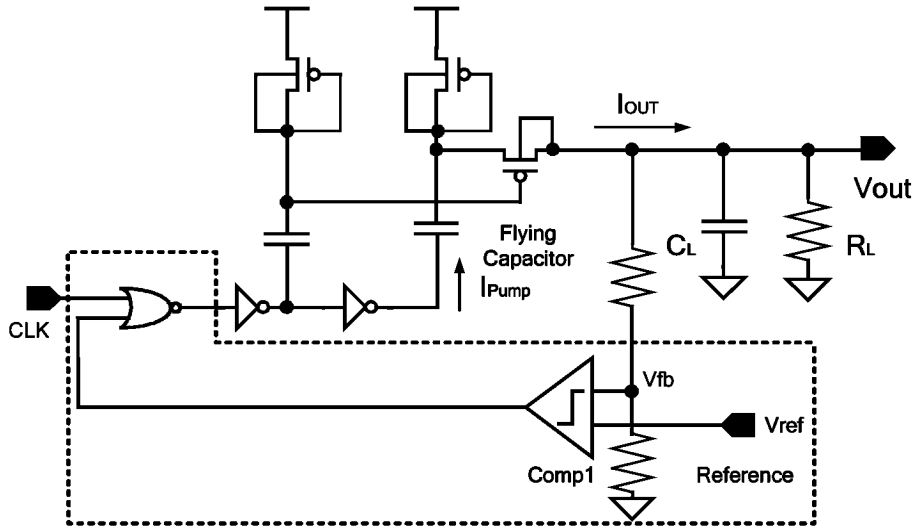

Fig. 1. Conceptual schematic of a conventional regulated charge pump.

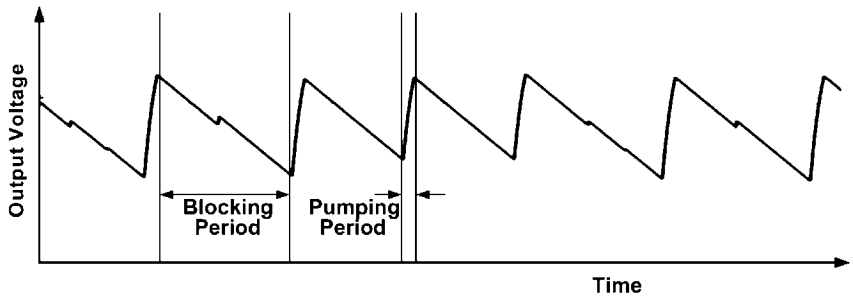

Fig. 2. Operation of a regulated charge pump.

To reduce output ripple voltage, voltage variation during the pumping and blocking periods should be minimized. During the pumping period, it is clear that either small pumping current or large output load capacitor or high switching frequency is required to achieve small ripple voltage. However, in practice, changing the load capacitor value is difficult when this value is given in a specification, and reducing the charge pumping ability may lose load current supplying capability. Therefore, in order to reduce the output ripple, control of the pumping current and switching frequency, according to the load current, is required.

During the blocking period, turning off the operation of the charge pump causes a relatively large voltage drop. Therefore, another novel scheme rather than the blocking scheme is required.

It is important to decrease the rise time for the robustness of the output voltage. If the charge pump has a fast rise time in a power-up state, fast recovery time is also shown after the output voltage drops abruptly. Using dynamic analysis of charge pump, rise time T_r [3], output voltage raises to the required voltage level, is derived as

$$T_r = \frac{\ln\left[1 - \dfrac{V_{\text{out}} - V_{\text{gain}}}{V_{\text{gain}}}\right]}{\ln \beta} \tag{2}$$

$$\beta = \frac{1}{1 + \dfrac{C_{\text{flying}}}{C_{\text{load}}}} \tag{3}$$

where V_{gain} is the maximum gained voltage at the flying capacitor, and (2) is expressed by the number of clock cycles. Large V_{gain} is essential in reducing the rise time. However, it creates large ripple voltage in a steady state, because it increases the charge at load capacitor during the pumping period. Therefore, in a dynamic state, V_{gain} during the pumping period should be maximized for fast rise time, and in a steady state, minimized for small ripple voltage.

III. Proposed Regulated Charge Pump

A. Automatic Pumping Current Control Scheme

The proposed charge pump exploits the automatic pumping current control scheme; it changes pumping current according to the magnitude of the output voltage. At the low output voltage, the proposed charge pump uses large pumping current to rapidly increase output voltage. On the other hand, at the high output voltage, it reduces boosting power by turning off some of pumping drivers. Fig. 3 shows the reduction of output ripple voltage in the automatic pumping current control scheme, compared to the clock blocking scheme. In case of the conventional regulated charge pump, the output voltage is independent of the load resistance and has large ripple voltage because it always pumps the flying capacitor with full power. However the proposed charge pump using the automatic pumping current control scheme create a small ripple voltage with output voltage independent of load resistance.

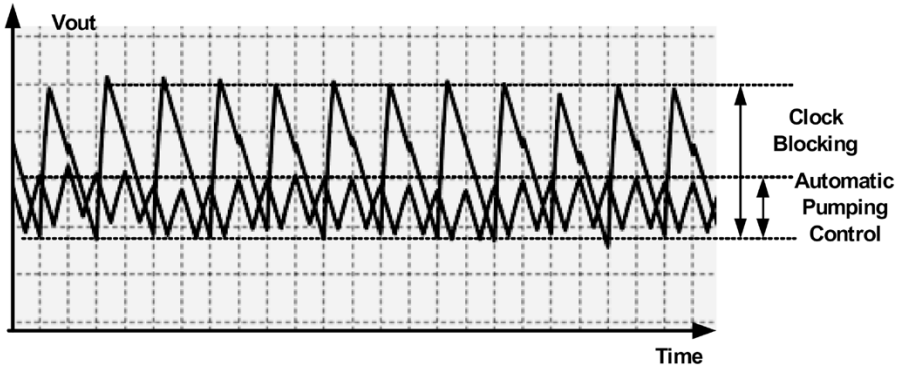

Fig. 3. Reduction of output ripple voltage in automatic pumping control.

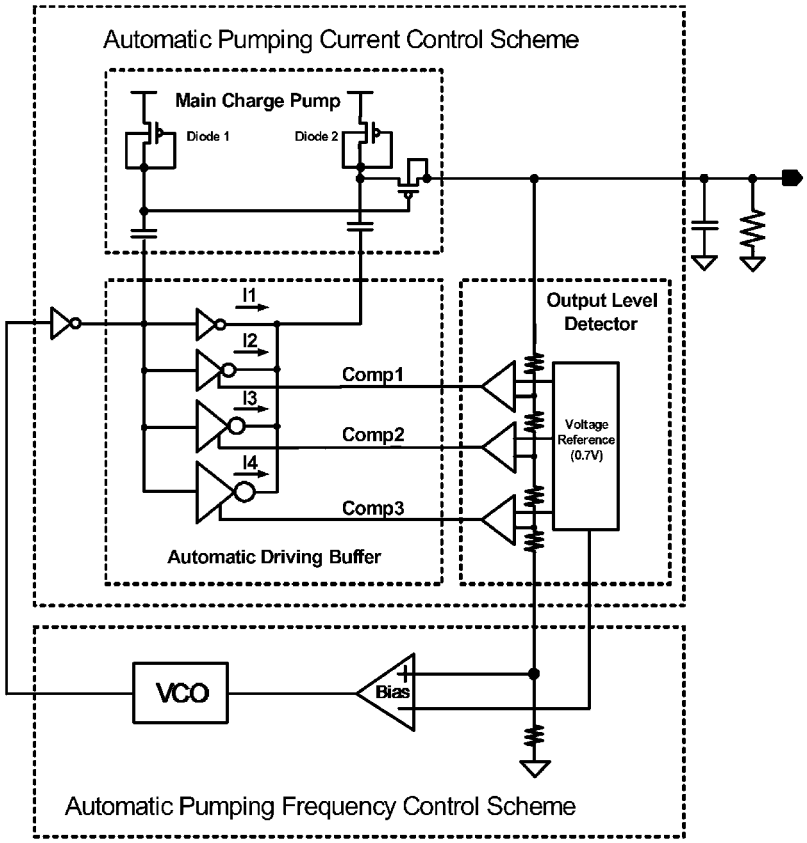

Fig. 4. Proposed charge pump.

The automatic pumping current control scheme is realized by three functional blocks; a main charge pump (MCP), an output level detector (OLD), and an automatic driver (ADR), as shown in Fig. 4. The operation of the MCP is to charge the load capacitor. The OLD senses the output voltage level and generates control signals for the ADR. By using resistor chain, scaled values of output voltage are compared to the reference voltage of 0.7 V in each comparator. The voltage reference and the comparator are shown in Fig. 5(a) and (b), respectively.

The bandgap reference voltage generator generates an output voltage of 1.2 V and the reference voltage of 0.7 V is generated using a voltage divider. It adopts a self-biased cascade structure [8] to reduce the effect of supply voltage variations and can effectively remove switching noise. The comparator has two feedback paths: the negative feedback of M1 and M2, and the positive feedback of M10 and M11 to accomplish hysteresis. It detects output voltage levels of 4.5, 4.8, and 5 V.

The ADR optimizes the pumping current by adjusting the number of buffers using the output value of the OLD, since the pumping current in (1) determines the ripple voltage. The operation of the ADR according to output voltage is shown in Fig. 6. When output voltage is low, the ADR provides full pumping current $(I_1 + I_2 + I_3 + I_4)$ to the flying capacitor and as output voltage rises, the pumping current delivered to the flying capacitor is stepwise reduced down to I_1.

B. Automatic Pumping Frequency Control Scheme

To further reduce output ripple voltage, the proposed charge pump also exploits the automatic pumping frequency control scheme that has been developed in previous works [9], [10].

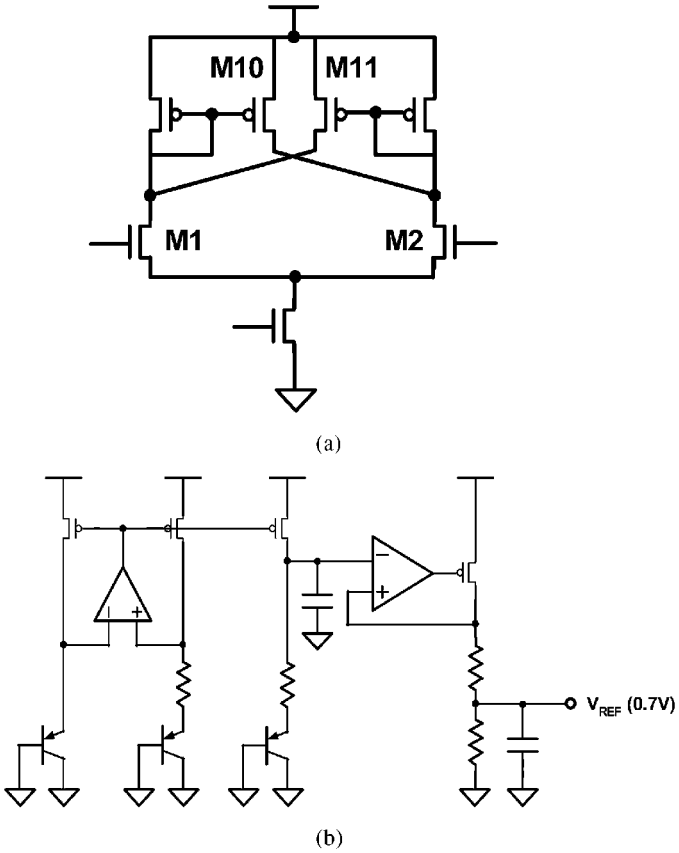

Fig. 5. (a) Comparator. (b) Voltage reference.

In (1), the switching frequency of the charge pump is related to the output ripple voltage. The switching frequency is equal to the pumping clock frequency because the proposed charge pump repeats the current pumping on every clock cycle, while the conventional charge pump with the clock blocking scheme continues to charge the load capacitor during the pumping period and stops during the blocking period. This switching frequency is larger than the pumping clock frequency. Fig. 7 shows the relationship between the output ripple voltage and the clock frequency. As (1) implies, the ripple voltage is inversely proportional to the switching frequency. The block diagram for the automatic pumping frequency control is shown in Fig. 4. A voltage-controlled oscillator (VCO) generates a clock signal, linearly determining the switching frequency. After the output voltage is detected, a bias block compares the voltage divided by resistors with the reference voltage and linearly converts that to the control voltage of the VCO. The operating clock frequency of the charge pump changes from 400 kHz to 600 kHz as output voltage rises.

C. Analysis of Proposed Charge Pump

To reduce the output ripple voltage and the recovery time after the drop in output voltage, a $V_{\rm gain}$ at each cycle is controlled according to output voltage. To analyze the proposed charge pump, the following assumptions are made:

1) The diode has constant forward bias voltage drop $(V_{\rm t})$ when the diode is on.

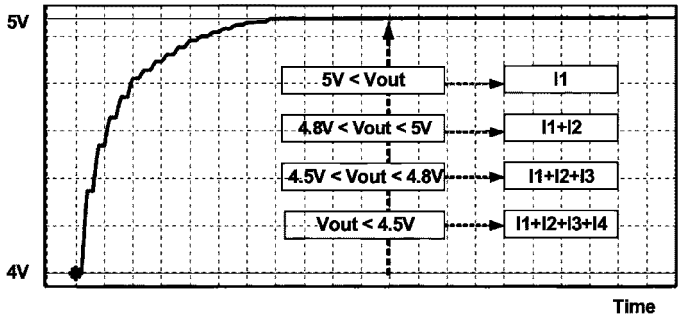

Fig. 6. Simulation result of the proposed charge pump.

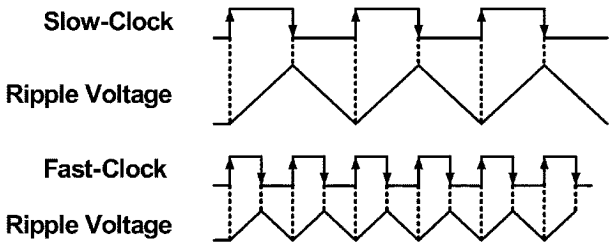

Fig. 7. Relationship between clock frequency and ripple voltage in the proposed charge pump.

2) Parasitic capacitance is negligibly small compared with the charge pump capacitance.

The pumping current $i_{\rm pump}$ of the proposed charge pump is expressed as

$$i_{\rm pump} = \sum_{j=1}^{n} i_j \quad (n = 1, 2, 3, 4) \tag{4}$$

where i_j is the pumping current delivered by each buffer in the ADR, and n is the index number of operating buffers which are operated by the output value of the OLD. The ripple voltage is obtained from (1) as

$$\Delta V_{\rm out} = \frac{\sum_{j=1}^{n} i_j}{C_{\rm load} \cdot f} = \frac{i_{\rm out}}{C_{\rm load} \cdot f}. \tag{5}$$

The pumping current is equal to that of the load resistor in a steady state. As load current increases, the output voltage level decreases, and the number of operating buffers increases.

Fig. 8 shows the dependence of the ripple voltage on the load current and the switching frequency under the condition of $V_{cc} = 3.3$ V and $C_L = 2$ μF. The output ripple voltage is proportional to the load current and inversely proportional to the pumping clock frequency.

It is important to guarantee the fast recovery of the output voltage after the output voltage drops abruptly. In order to model the recovery time, Thevenin equivalent circuit for this charge pump is derived from a large signal model in a steady state and then the time constant of output node is calculated from the output resistance and capacitance of the equivalent circuit. Fig. 9(a) shows the operation of the proposed charge pump in steady state. The currents I_p and I_n flow through $\rm P_1$ and $\rm N_1$ in the pumping period and the blocking period, respectively. If the resistances of $\rm D_1$ and $\rm SW_1$ are sufficiently smaller than the

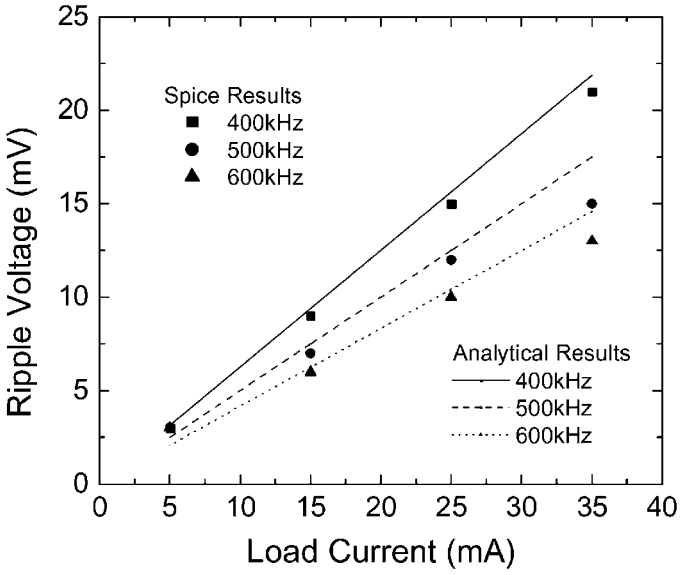

Fig. 8. Comparison of the analytical result with the SPICE simulation for the ripple voltage.

those of P_1 and N_1, V_{boost} is V_{out} or $V_{cc}-V_t$ and V_{node} changes linearly as shown in Fig. 9(b) since P_1 and N_1 operate in triode region. The current I_p and I_n can be obtained from the current equation of MOSFET in a triode region as

$$I_p\left[\mathrm{nT}, \mathrm{nT}+\frac{T}{2}\right] \approx \mu_p C_{\mathrm{ox}} \frac{W_p}{L_p}\left\{(V_{cc}-V_{thp})(V_{cc}-V_{nh}) - \frac{(V_{cc}-V_{nh})^2}{2}\right\} \tag{6}$$

$$I_n\left[nT+\frac{T}{2}, (n+1)T\right] \approx \mu_n C_{\mathrm{ox}} \frac{W_n}{L_n}\left\{(V_{cc}-V_{thn})V_{\mathrm{nl}} - \frac{V_{\mathrm{nl}}^2}{2}\right\} \tag{7}$$

where V_{nh} and V_{nl} are the averages of V_{node} in the pumping period and the blocking period, respectively.

In a steady state, the output current is equal to the currents supplied by P_1 and N_1 for half cycle time ($I_{\mathrm{out}} = I_p/2 = I_n/2$) because the V_{node} does not change according to clock cycle, and assuming $V_{cc}-V_{thp} \gg V_{cc}-V_{nh}$ and $V_{cc}-V_{thn} \gg V_{nl}$

$$V_{nl} = \frac{\mu_p}{\mu_n}\cdot\frac{W_pL_n}{L_pW_n}\cdot\frac{V_{cc}-V_{thp}}{V_{cc}-V_{thn}}(V_{cc}-V_{nh}) \tag{9}$$

$$dV_{nl} = -\frac{\mu_p}{\mu_n}\cdot\frac{W_pL_n}{L_pW_n}\cdot\frac{V_{cc}-V_{thp}}{V_{cc}-V_{thn}}dV_{nh}. \tag{10}$$

According to the charge conservation law, the total charge stored in the circuit at time $nT + T/4$ is equal to the sum of

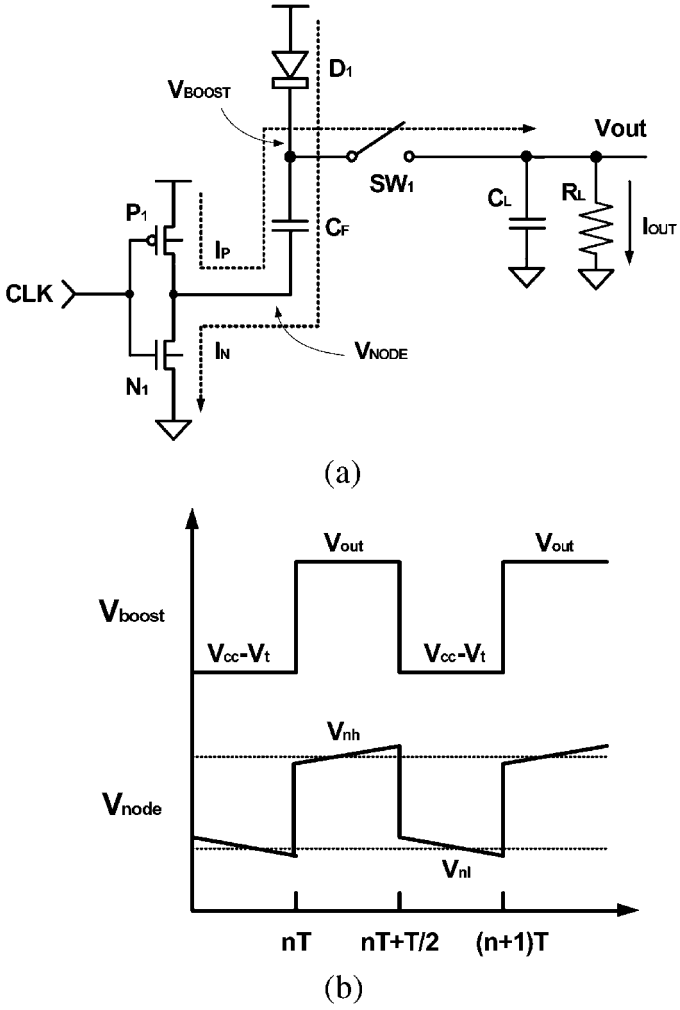

Fig. 9. (a) Operation of the proposed charge pump. (b) Timing diagram of V_{boost} and V_{node}.

the charge flowing into load resistance for $T/2$ and the charges stored in the capacitors C_f and C_1 at time $nT + T3/4$.

$$(V_{\mathrm{out}}-V_{nh})C_f + V_{\mathrm{out}}C_1 = (V_{cc}-V_t-V_{\mathrm{nl}})C_f + V_{\mathrm{out}}C_1 + I_{\mathrm{out}}\frac{T}{2} \tag{11}$$

$$dV_{\mathrm{out}} = dV_{nh} - dV_{\mathrm{nl}} \tag{12}$$

From (10) and (12)

$$dV_{\mathrm{out}} = \left(1+\frac{\mu_p}{\mu_n}\cdot\frac{W_pL_n}{L_pW_n}\cdot\frac{V_{cc}-V_{thp}}{V_{cc}-V_{thn}}\right)dV_{nh}. \tag{13}$$

By differentiating (6) and using (13)

$$dI_p \approx -\frac{\mu_p C_{\mathrm{ox}}\frac{W_p}{L_p}(V_{cc}-V_{thp})}{1+\frac{\mu_p}{\mu_n}\cdot\frac{W_pL_n}{L_pW_n}\cdot\frac{V_{cc}-V_{thp}}{V_{cc}-V_{thn}}}dV_{\mathrm{out}}. \tag{14}$$

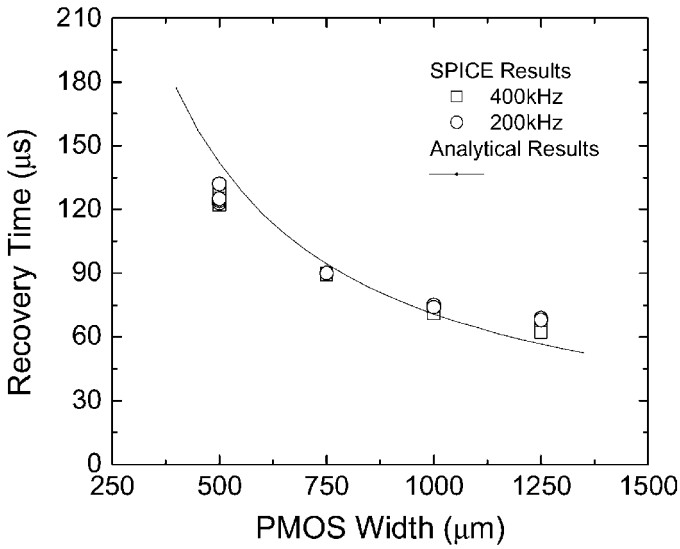

Fig. 10. Comparison of the analytical result with SPICE simulation for recovery time.

From (14), the relationship between the variations of $V_{\rm out}$ and $I_{\rm out}$ is expressed as

$$\frac{dV_{\rm out}}{dI_{\rm out}} \equiv R_{\rm rec} \approx -\frac{2\left(1+\frac{\mu_p}{\mu_n}\cdot\frac{W_pL_n}{L_pW_n}\cdot\frac{V_{cc}-V_{thp}}{V_{cc}-V_{thn}}\right)}{\mu_pC_{\rm ox}\frac{W_p}{L_p}(V_{cc}-V_{thp})}. \quad (15)$$

$R_{\rm rec}$ represents the equivalent output series resistance of the proposed charge pump and is dependent on the electrical characteristics, the dimensions of transistors and the gate voltage. The recovery time that gets back up to 63% of $\Delta V_{\rm out}$ is the time constant $tR_{\rm rec}C_L$.

Fig. 10 shows the comparison of the analytical result with the SPICE simulation for the recovery time as a function of the size of driver buffer under the condition of $\Delta V_{\rm out} = 0.4$ V $\sim$ 2.4 V and $C_L = 2$ μF. The analytical data have been in good agreement with the SPICE simulation results. Fig. 10 indicates that the recovery time does not depend on the switching frequency and $\Delta V_{\rm out}$, and is inversely proportional to the width of the pMOS (P_1). Therefore, the recovery time of the proposed charge pump compared to the conventional charge pump decreases by stepwise increasing the size of the driving buffer when the output voltage reduces below the specified voltages.

IV. Experimental Results

The approach of the proposed charge pump is focused on producing small output ripple voltage while delivering large load current. To validate the results of our schemes, the proposed charge pump was fabricated using 3.3-V 0.13-μm CMOS technology as the power supply circuit in an USB-OTG transceiver. The microphotograph is shown in Fig. 11. Its active area is 0.25 mm^2 except for a 330-nF external flying capacitor. On the bottom right side, the pumping MOS diodes are designed as large as possible to supply enough load current. The output stage of the proposed charge pump is composed of a variable load resistor and a 2-μF load capacitor mounted on a test PCB.

Fig. 11. Microphotograph of proposed charge pump.

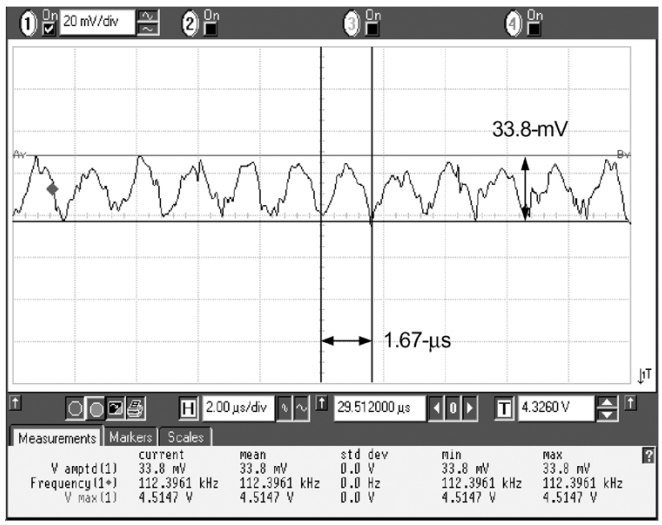

Fig. 12. Measurement results of output voltage.

Fig. 12 shows that the output ripple voltage is 33.8 mV with the automatic pumping control scheme when the load current is 30 mA and the output voltage is 4.5 V. The rise time and fall time of the output voltage are equal to each other since the pumping operation is performed on every clock cycle and the clock duty cycle is 50%. In the conventional charge pump, these times are different because the charge pump stops pumping operations until the output voltage drops lower than the required output voltage level.

Fig. 13 shows the measured output and the ripple voltage versus the load current. A set of measurements has been performed by changing the value of the variable load resistor connected to the output. As load current increases, output voltage gradually drops to 4.5 V and output ripple voltage changes from

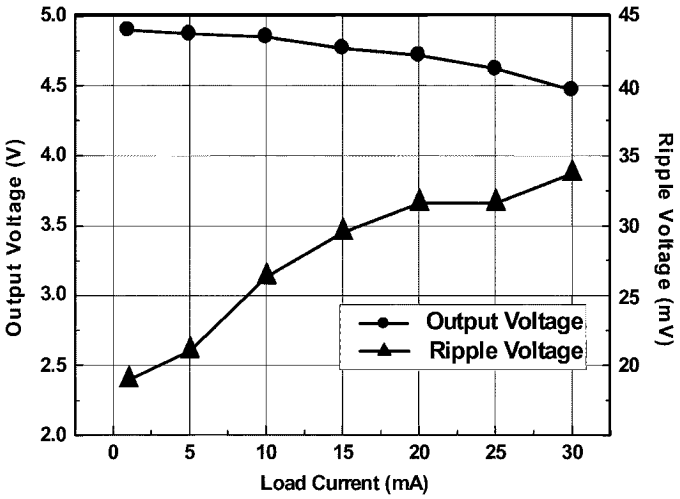

Fig. 13. Measurement results of output and ripple voltage as a function of load current.

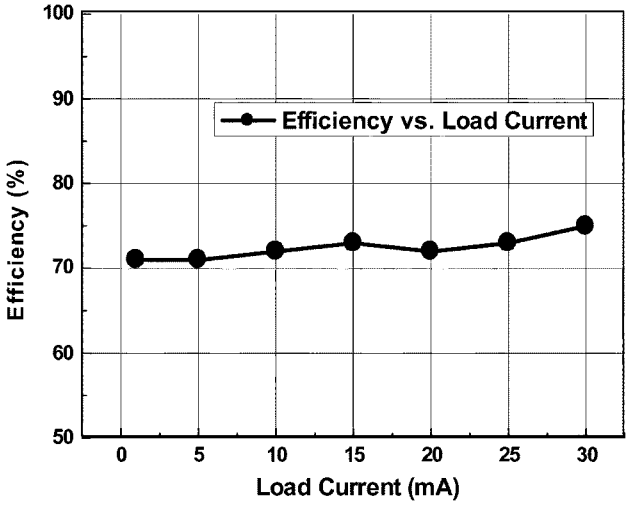

Fig. 14. Measurement results of power efficiency.

18 mV to 33.8 mV. The ripple voltage is proportional to load current. However, the difference between the measured ripple voltage and the SPICE simulation result shown in Fig. 8 increases as the load current increases because the simulation result does not include the noise caused by parasitic components. The leakage current was through the pMOS used as SW1 in Fig. 9(a). This can also increase ripple voltage.

Power efficiency of a charge pump [11] is shown as

$$\mathrm{Eff}_{\mathrm{power}} = \frac{I_{\mathrm{out}} V_{\mathrm{out}}}{I_{\mathrm{power}} V_{\mathrm{power}}} \times 100. \tag{16}$$

The corresponding result is higher than 70% regardless of load current, as shown in Fig. 14. When the load current becomes smaller, the dynamic power loss caused by switching large transistors does not change and the ratio of the power loss over the output power increases. As a result, the power efficiency degrades as load current decreases.

To verify the effect of the pumping clock frequency on the output voltage and the output ripple voltage, the VCO is turned off and an external clock is applied as a pumping clock. Fig. 15 shows that the pumping clock frequency does not influence the

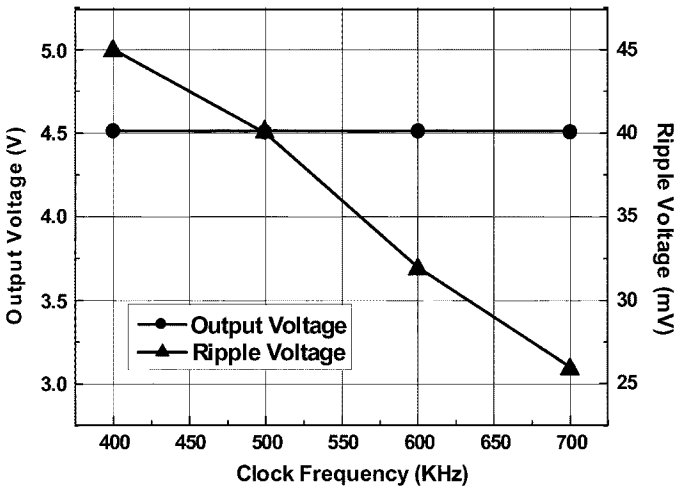

Fig. 15. Measurement results of output and ripple voltage as a function of clock frequency.

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED CHARGE PUMP

Supply Voltage	3.3-V
Pumping Frequency	400-kHz~ 600-kHz
Output Voltage	4.5-V~5-V
Ripple Voltage	33.8-mV (with 2μF load capacitor)
Efficiency	70%~75%
Area	0.25 mm^2
Technology	3.3-V 0.13-μm CMOS technology

output voltage and the output ripple voltage is inversely proportional to the pumping clock frequency at a load current of 30 mA. In a steady state, output ripple voltage shows a linear triangle wave as shown in Fig. 12. Although clock frequency is changed, output voltage increase during a positive clock phase equals to the decrease during a negative clock phase. Therefore, the output voltage is not affected by frequency change.

Table I summarizes the performance characteristics of the proposed charge pump.

V. CONCLUSION

A new regulated charge pump with low output ripple voltage and high load current drive capability is proposed enhancing tolerance of the output voltage variation. This proposed charge pump adopts the automatic pumping current control scheme and automatic pumping frequency scheme. The analysis of the charge pump is carried out to model the ripple voltage and the recovery time. The proposed charge pump is implemented using a 3.3-V 0.13-μm CMOS technology. The test chip generates 4.5-V output from a 3.3-V supply with supplying up to 30 mA of load current. Its ripple voltage is less than 33.8 mV with a 2-μF load capacitor. The power efficiency is higher than 70% at the range of load current from 1 mA to 30 mA. The proposed charge pump is used as the power supply circuit in the USB-OTG transceiver.

ACKNOWLEDGMENT

The authors would like to thank Samsung Electronics Corporation for the test chip and test PCB fabrication.

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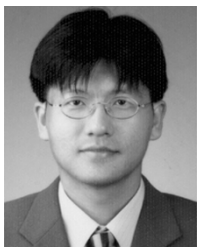
He subsequently joined the Basic Research Laboratory of Electronics and Telecommunications Research Institute (ETRI), Daejeon. Since then, he has been engaged in the research and development of MEMS switch driver and intrabody communication system.



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From 1988 to 1990, he was with Bell Communications Research, Red Bank, NJ, where he invented the two-dimensional phase-locked VCSEL array, the front-surface-emitting laser, and the high-speed lateral HBT. In 1991, he became Manager of a DRAM design group at Hyundai Electronics and designed a family of fast-1M DRAMs and synchronous DRAMs, including 256M SDRAM. From 1995 to 1997, he was a faculty member with Kangwon National University. In 1998, he joined the faculty of the Department of Electrical Engineering at KAIST, and led a project team on RAM Processors (RAMP). In 2001, he founded a national research center, System Integration and IP Authoring Research Center (SIPAC), funded by Korean government to promote worldwide IP authoring and its SOC application. Currently, he serves as the Project Manager for IT SoC and Post-PC in Korea Ministry of Information and Communication. His current interests are SOC design, IP authoring, high-speed and low-power memory circuits and architectures, design of embedded memory logic, optoelectronic integrated circuits, and novel devices and circuits. He is the author of the books *DRAM Design* (Seoul, Korea: Hongleung, 1996; in Korean) and *High Performance DRAM* (Seoul, Korea: Sigma, 1999; in Korean).

Dr. Yoo received the Electronic Industrial Association of Korea Award for his contribution to DRAM technology in 1994 and the Korea Semiconductor Industry Association Award in 2002.