A Review of Carbon Nanotube Ensembles as Flexible Electronics and Advanced Packaging Materials

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The exceptional electronic, thermal, mechanical, and optical characteristics of carbon nanotubes offer significant improvement in diverse applications such as flexible electronics, energy conversion, and thermal management. We present an overview of recent research on the fabrication, characterization and modeling of carbon nanotube (CNT) networks or ensembles for three emerging applications: thin-film transistors for flexible electronics, interface materials for thermal management and transparent electrodes for organic photovoltaics or light emitting diodes. Results from experimental measurements and numerical simulations to determine the electrical and thermal transport properties and characteristics of carbon nanotube networks and arrays used in the above applications are presented. The roles heterogeneous networks of semiconducting and metallic CNTs play in defining electrical, thermal, and optical characteristics of CNT ensembles are presented. We conclude with discussions on future research directions for electronics and packaging materials based on CNT ensembles. [DOI: 10.1115/1.4004220]

1 Introduction

CNTs have quasi 1D structure with unique electrical, optical, mechanical, and thermal properties which make them very attractive for a wide range of applications [1]. The thermal conductivity of a single-wall nanotube is measured as high as 3500 W/mK [2,3], their electron mobility can be up to 10,000 $cm^2\ Vs^{-1}$ [4] at room temperature and their Young's moduli are in the range of 1–2 TPa [5]. These remarkable properties of CNTs have motivated an extensive study for their possible use in diverse applications of electronic devices, avionic structures, energy conversion devices, thermal interface materials, interconnects, chemical/biological sensors, solar cells, and hydrogen storage devices [1,6–17]. Many of these applications require fabrication of thin-films or composites using a large number of nanotubes in random networks, mats or parallel arrays; precise alignment of CNTs is not a stringent requirement. These structures are relatively inexpensive and compatible with large scale manufacturing [10].

Thin-film transistors (TFTs) on flexible substrates have been investigated extensively for diverse applications such as displays [18], e-paper, e-clothing, and pressure-sensitive skin [14], large area chemical and biological sensors [6], flexible and shape-conformable antennae, and radar [14]. Thin-film transistors based on CNT networks (CNTN-TFTs) are being explored to substantially increase the performance of flexible electronics to address medium-to-high performance applications in the 10 MHz to 1 GHz range [1,14]. High mobility, substrate-neutrality, and low-temperature/low-cost processing make CNTN-TFTs very promising for these flexible-electronic applications. The network of CNTs forms the channel region of the transistor and they are amenable to mass manufacture. Various groups fabricated these TFTs for macroelectronics and chemical sensing applications [1] and have begun to explore their performance. Snow et al. [15,16] reported the mobility and conductance properties of CNT networks and explored the interfacial properties of CNTs in chemical sensing transistor. Zhou et al. demonstrated fabrication of p-type and n-type transistors [9], which could be used as building blocks for complex complementary circuits. Cao et al. [1] reported fabrication of an integrated digital circuit composed of up to nearly 100 transistors on plastic substrates using a random network of CNTs. Recently, a number of groups have focused on developing TFTs with *well-aligned* and *or partially aligned* nanotubes for very high performance applications [11,12] using transfer printing; mobilities of 1000 $cm^2\ Vs^{-1}$, comparable to single-crystal silicon are achievable using this technology [1]. Other experimental reports on CNTN-TFTs fabrication for diverse applications can be found in Ref. [1].

Ensembles of CNTs are also being developed as thermal interface materials (TIM) for advance packaging concepts. The thermal management problem near a chip or electronic device can be very severe because of nonuniform heating and the need to maintain the hottest spot on the chip below a certain design point. Such nonuniform heating has been shown to multiply the magnitude of interface resistance near the chip by a factor greater than one, which increases with the degree of nonuniformity in the heat generation, when calculating the thermal resistance of the total package (i.e., the junction to ambient resistance) [19]. This "hot spot" effect has become more severe over the past few decades because of substantial increase in the power density of electronic packages, and as a result thermal interface resistance can now comprise a significant portion of the total thermal resistance in high-power packages (more than 50% in some cases) [19]. To mitigate thermal management challenges that arise from such increase in contact resistance, considerable attention has been focused on developing advanced TIMs that utilize the extraordinarily high axial thermal conductivity of CNTs [20,21]. Early studies focused on dispersing CNTs in a compliant polymer matrix to enhance the effective thermal conductivity of the composite structures [22]. Yet, only modest improvements in thermal performance were achieved because enhancement of thermal conductivity in such structures is hindered by mechanical stress at CNT-matrix boundaries that reduces the speed at which phonons propagate in the CNTs (i.e., the surrounding elastic medium alters phonon dispersion and reduces the intrinsic thermal conductivity in CNTs) [23]. Recently, significant attention has shifted to vertically oriented CNT arrays as promising TIM structures that have been demonstrated to produce contact resistances that compare favorably to state-of-the-art materials [24]. Such configurations possess a

Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the JOURNAL OF ELECTRONIC PACKAGING. Manuscript received October 23, 2009; final manuscript received May 1, 2011; published online June 17, 2011. Assoc. Editor: Cemal Basaran.

synergistic combination of high mechanical compliance and high effective thermal conductivity—in the range of 10–200 W/mK [25–27]. The conformability feature is particularly advantageous in addressing mismatches in coefficients of thermal expansion that can cause TIM delamination and device failure. Also, in contrast to polymer-CNT composites, CNT array interfaces are dry and chemically stable in air from cryogenic to high temperatures (~450 °C), making them suitable for extreme-environment applications [28].

In addition to development for CNTN-TFT applications, semi-transparent thin-film networks of single-wall CNTs (SWNTs) are also being developed to provide an alternative to transparent conducting oxides (TCO) in electronic devices such as organic photovoltaics and organic light emitting diodes (OLED) [29,30]. Most of the efforts on developing SWNT networks have generally consisted of a heterogeneous mixture of nanotubes with metallic and semiconducting characteristics with ratios of metallic/semiconducting tubes being of order 1:2. Heterogeneous mixtures yield transparent electrodes with optoelectronic properties comparable to indium tin oxide (ITO) deposited on plastic substrates [31]; however, the sheet resistance and transmittance of these SWNT films have yet to compete favorably with TCOs on glass substrates [32]. In general, ITO on glass substrates have obtained sheet resistances less than 20 Ω-sq^{-1} with transparencies greater than 85% at 550 nm. Heterogenous mixtures of CNTs have obtained sheet resistance greater than 150 Ω-sq^{-1} at similar transparency values. The ease of low-temperature processing of SWNTs as thin-films, and the potential of improved compatibility with other electronic organic thin-film materials motivates research to further improve their thin-film optical and electronic properties. Such efforts include the use of monodispersed SWNT films consisting of either semiconducting or metallic behavior. Progress in the efficient separation of SWNTs by electronic type now allows for such an approach to be taken [33,34]. Recent efforts have shown promise in that sheet resistances on the order of 60 Ω-sq^{-1} have been obtained for doped CNT electrodes at transparencies greater than 70%.

In this paper, we present an overview of recent research on the fabrication, characterization and modeling of thin-films, or composites based on CNT networks. A wide range of applications in electronic and optoelectronic devices, and thermal management have been explored using 2D and 3D networks or arrays of CNTs. A detailed review of every application proposed in these fields is out of scope of the present paper, so we have selected three application areas—thin-film transistors, thermal interface materials, and transparent electrodes—where we feel that especially promising research advances have been made recently. We first present a recent development [10,35–44] in the fabrication of CNTN-TFTs which has addressed some major challenges for this class of TFTs. A numerical modeling approach for analyzing the conducting properties of CNT thin-films made of a percolating network of CNTs is presented. Predictions of the electrical characteristics of CNTN-TFTs as a function of device parameters are presented and their behavior is explained by invoking the physics of heterogeneous finite-sized networks of metallic and semiconducting tubes. We present modeling approaches for predicting the performance of organic TFTs with CNT dispersions where charge transport in both semiconducting organic matrix and CNT-network is important. Then, we turn our attention to CNT arrays as thermal interface materials; a model that describes heat conduction through CNT array thermal interface materials is presented first in [45]. We discuss CNT array interface structures that have achieved the most promising results to date and present measurements of their total resistances as a function of interface pressure [46–51]. A transient photoacoustic technique [47] is used to measure component resistances that sum to produce the total resistance of the CNT array interface, and critical bottlenecks to heat conduction are identified. Finally, we discuss the use of CNT films as transparent electrode alternatives for organic electronic devices. Here, the impact of processing and doping of CNT films will be discussed. Integration issues with devices will be discussed. Recommendations for future research in all three focus areas—thin-film transistors, thermal interface materials, and transparent electrodes—are presented at the end of the respective sections.

2 CNT Network Based Thin-Film Transistors

In CNTN-TFTs, a sub-monolayer to a few layers of 2D ensembles of nanotubes is used as channel region between the source and drain electrodes of the thin-film transistor (Fig. 1). Different fabrication techniques have been used to make a thin layer of CNTs which have different degree of control on the density, orientation, and length distribution of CNTs [1]. Solution deposition methods such as vaccum-filtration and controlled flocculation are attractive methods for a large area synthesis of CNT-thin-films on wide variety of substrates [52,53]. External electric or magnetic field and mechanical shear is used to align CNTs for fabrication of devices which need aligned arrays of CNTs on substrates to achieve high performance [54]. Chemical vapour deposition techniques can be used to achieve better control of purity, morphology, and alignment of CNTs in their thin-films [55].

The major research in the area of CNTN-TFTs is motivated by achieving high performance, reducing nonuniformity in the device performance, and developing processing conditions for large scale integration. High performance of these devices require high electron mobility, high on-current (I_{on}), and high on-off current ratio. In a typical CNT network one third of the tubes are of metallic nature and the two third of the tubes are semiconducting nature. Metallic CNTs are problematic as they can form a percolating network from the source to drain of a TFT, short the device and limit on-off current ratios [39]. One of the most challenging tasks in achieving high performance of CNTN-TFTs is the removal of metallic CNTs from a CNT network. Different techniques have been applied to purify the CNT networks from metallic contamination such as electric burning of metallic tubes [9], density-gradient centrifugation [56], and surface sorting [57,58]. Zhou et al. [9] and Seidel et al. [59] have performed electric breakdown to burn metallic CNTs from CNTN-TFTs and successfully achieved on-off ratio of the order of 1000. However, such breakdown also removes some semiconducting CNT pathways from source to drain leading to significant decrease in the on-current of device. In addition, this method is not scalable for large scale commercial production. A gas-phase plasma hydrocarbonation reaction technique has been used to selectively etch and gasify metallic nanotubes and obtain pure semiconducting nanotubes [60]. Another process that separates single-walled carbon nanotubes (SWNTs) by diameter, band gap, and electronic type using centrifugation of compositions of SWNTs with surface active components in density-gradient media is reported in Ref. [56]. These techniques also create defects in the remaining CNT networks and add impurities which degrade the overall performance of the TFTs. A self-sorting method to separate semiconducting or metallic CNTs during the solution deposition of CNTs on substrate is proposed by LeMieux

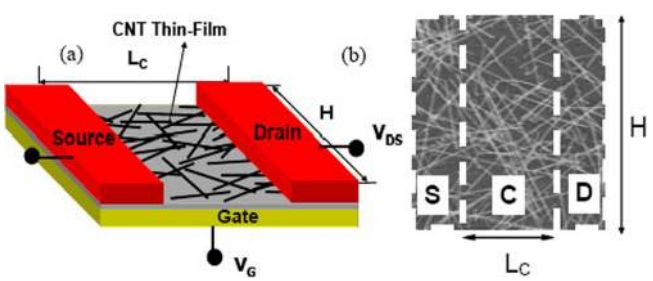

Fig. 1 Schematic of (*a*) nanotube network thin-film transistor showing source, drain, gate, and channel region. (*b*) Channel region of thin-film transistor showing source (S), drain (D), and channel (C). The channel region is composed of a network of CNTs, Geometric parameters are also shown. L_C is the length of the channel and *H* is the width of the transistor [36].

et al. [57]. In this sorting method, the SiO_2 substrate is functionalized by organic groups such as amines and the high molecular interaction of semiconducting CNTs with these organic functional groups is exploited to separate and deposit semiconducting CNTs on the substrate. On-off current ratios as high as 900,000 were achieved using this method indicating that the CNT network is composed primarily of semiconducting CNTs [57]. However, a large variation in the on-off ratio is observed indicating nonuniformity in the CNT film on the substrate.

A promising method to break metallic pathways from the source to drain electrodes of a CNTN-TFT is a striping technique wherein the random network of CNTs is stripped into stripes along the width of the TFT [10]. The striping method is based on the relocation of the percolation threshold of the CNT network; the device-width and density of CNT network in the device need to be well chosen such that metallic CNTs do not percolate through the device. Following this method, CNTN-TFTs have been fabricated with on-off ratio greater than 1000 and degradation in the on-current by a factor less than two [10]. This method seems promising for large scale fabrication of integrated circuits using CNTN-TFTs. Cao et al. [10] fabricated small-scale integrated circuits using 100s of such CNTN-TFTs on a plastic substrate with on–off current ratio as high as 100,000 and switching speed in kilohertz range. Kim et al. [61] used similar striping technique to fabricate a small pixel circuit using CNTN-TFTs for transparent electronics applications with on–off ratio greater than 1000 and mobility in the range of 16–22 $cm^2\ Vs^{-1}$. They have demonstrated fabrication of very uniform networks of CNT films on the quartz substrate using evaporated thin-film Fe catalysts on the substrate leading to minimal variation in the performance from one device to the other. Such uniformity in CNT films is difficult to achieve using solution based deposition techniques. The electron mobility of a single CNT can be as high as 10,000 $cm^2\ Vs^{-1}$ at room temperature, while the mobility of thin-films of random networks of CNTs is orders of magnitude lower than the individual CNTs ($\sim$10–100 $cm^2\ Vs^{-1}$) due to the multiple CNT–CNT contacts in the network. Operating frequency in the range of gigahertz or higher is desired for some flexible electronics applications such as RF devices for military communication electronics. TFTs based on a random network of CNTs may not have such high frequency of operation. TFTs based on the perfectly aligned, parallel array of CNTs have been fabricated for such applications with power gain frequencies in the range of 10 GHz [62].

In-plane electrical transport dominates in 2D thin-films of CNTs which poses a very specific and interesting problem of understanding the transport and predicting the device performance of CNTN-TFTs. There are a large number of unknowns regarding the ultimate performance limits of these TFTs. The typical length of these devices is in the range of 1–100 μm. At these scales, the nanotube length may compete with the finite size of the device and bulk behavior of random 2D network does not occur, so bulk properties of thin-films may not be directly used to predict the performance of these devices [36]. Strong electrical, thermal, and optical interactions between the tubes and the substrates affect device performance. A detailed investigation is required to understand the fundamental physics that govern device operation and scaling as a function of tube orientation, tube density, ratio of metallic to semiconducting tubes, and tube-substrate interaction [37,39]. Computational models have been developed to explore the transport properties of heterogeneous percolating network of CNTs and to predict the device characteristics of transistors made from these CNT networks. Good agreement between numerical model predictions and observations from different experiments has been demonstrated [37,39,40]. We next present a brief description of the transport models developed in last few years to understand the conductive and current-voltage characteristics of the CNTN-TFTs.

A schematic of a nanotube bundle transistor is shown in Fig. 1. A typical transistor is a four terminal device in which the four terminals are the source (S), drain (D), gate (G), and substrate (see Fig. 1). A fixed voltage bias, V_{DS}, is applied across the channel from drain to source to drive the mobile charges in the channel region, while the transistor is turned on and off by changing the gate voltage, V_{GS}. The corresponding current is denoted by I_{DS}. An important parameter to assess device performance is the on–off ratio (R) which is the ratio of the current flowing in the device in the on-state, I_{ON}, to the current in device in the off-state, I_{OFF}. Kumar et al. [37,39] performed analysis of the electrical performance of CNTN-TFTs in the linear regime, a regime where V_{DS} is low and current (I_{DS}) through the device is linearly proportional to V_{DS}. A extension of this problem has been reported by Ref. [40] that generalizes this problem to high-bias regime ($\sim$high V_{DS}) and provides proper scaling laws to predict the performance of the transistors. For an insulating substrate, only transport in the percolating network of tubes has been considered and the effective conductance of the pure network is computed, Fig. 2(*a*). If the substrate is sufficiently conducting as for CNTs network dispersed in organic substrate, transport in both substrate and tube network has been considered for computing the effective conductive properties, incorporating the effect of tube-to-substrate interaction [37].

If the channel of TFTs $L_C \gg \lambda$, the mean free path of electrons, a drift-diffusion model for carrier transport can be employed [44]. In the linear regime, which occurs for low source-drain voltage V_{DS}, the current density along the tube can be given by $J = \sigma d\Phi/ds$. Here, σ is the electrical conductivity and Φ is the potential, and is only a function of the source-drain voltage V_{DS}. Using the current continuity equation $dJ/ds = 0$ and accounting for charge transfer to intersecting tubes as well as to the substrate [36], the dimensionless potential distribution ϕ_i along tube i, as well the three-dimensional potential field in the substrate can be given by

$$\frac{d^2\phi_i}{ds^{*2}} + \sum_{\text{intersecting tubes j}} c_{ij}(\phi_j - \phi_i) + d_{is}(\phi_s - \phi_i) = 0 \qquad (1a)$$

$$\nabla^{*2}\phi_s + \sum_{i=1}^{N_{tubes}} d_{is}\beta_v \frac{\sigma_t}{\sigma_s}(\phi_i - \phi_s) = 0 \qquad (1b)$$

Here, c_{ij} is the dimensionless charge-transfer coefficient between tubes i and j at their intersection point. The term d_{is} is the dimensionless charge-transfer coefficient between tubes and the substrate, which is active only for nanotubes in conducting substrates. The

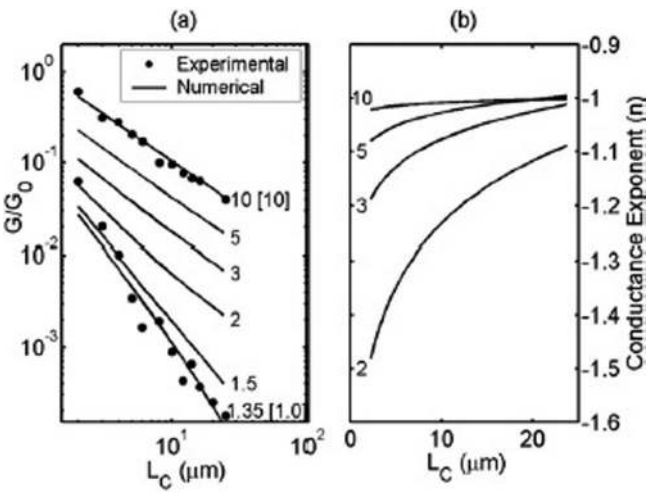

Fig. 2 (*a*) Computed conductance dependence on channel length for different densities (ρ) in the strong coupling limit ($c_{ij} = 50$) compared with experimental results from Ref. [15]. For $\rho = 10.0\ \mu m^{-2}$, $G_o = 1.0$ (simulation), $G_o = 1.0$ (experiment). For $\rho = 1.35\ \mu m^{-2}$, $G_o = 1.0$ (simulation), $G_o = 2.50$ (experiment). The number after each curve corresponds to the value of ρ used in the simulation. The number in [ ] corresponds to ρ in experiments from Ref. [15]. (*b*) Dependence of conductance exponent (n) on channel length for different densities (ρ) based on (*a*) [44].

σ_t/σ_s is electrical conductivity ratio and β_v is the geometric parameter. The nondimensional equations for the tubes and substrate can be discretized using the finite volume method and a system of linearly coupled equations can be solved for the tube segment potential ϕ_i and the substrate potential ϕ_s. Computed potentials can be further used to compute the current though the CNT segments, substrate and the entire device using the current continuity equation. To account for randomness in the CNT network, results must be computed by taking an average over a large number of random realizations of the network. We next present some computational results based on the transport model describe above in order to demonstrate the importance and robustness of these models for analyzing the characteristics and performance of CNTN-TFTs. The conductive properties of the 2D CNT network and the effect of metallic-semiconducting mixture in CNT network is presented first followed by a brief discussion of the modeling results for a CNT doped organic semiconductor based TFT.

2.1 Conductive Properties of CNT Network. The conductive properties of the network are strongly dependent on the density of the tubes in the network. A conducting path between source and drain may not exist at very low tube densities. If such tube network is used as the channel region of the transistor, no current could pass through the transistor. As the density of tubes increases, a critical density ρ_{th}, known as the percolation threshold, is reached, at which a complete pathway between source and drain is formed. The percolation threshold for the network can be given by $\rho_{\text{th}} = 4.23^2/\pi L_t^2$, which can be obtained from numerical simulations [63]. There is great interest in exploring the transport behavior of the network at densities close to the threshold, which is dependent on the dimensionality and the aspect ratio of the tubes. Close to the percolation threshold, the network conductance, G, exhibits a power-law relation, i.e. $G \sim (\rho - \rho_{\text{th}})^m$, where m is the percolation exponent [64].

Kumar et al. [44] estimated the electrical conductance (G) of a planar network of CNTs as a function of channel length (L_C) using the drift diffusion theory for tube densities (ρ) in the range 1–10 μm^{-2} and channel lengths varying from 1 to 25 μm (see Fig. 2). The average length (L_t) of the tubes are in the range from 1 to 3 μm and width H of the device is 90 μm; these dimensions and tube lengths are chosen to match the experimental observations in Ref. [15]. For long channels ($L_C > L_t$) there are no tubes directly bridging the source and drain, and current can flow only because of the presence of the network. If the tube density is greater than the percolation threshold ρ_{th}, a continuous path for carrier transport exists from source to drain, and G is seen to be nonzero even for $L_C/L_t > 1$. The values of nondimensional charge transfer coefficients are $c_{ij} = 50$ and $d_{is} = 0$ which represent good contact conductance between CNTs, but negligible charge transport between CNTs and substrate as substrate is nonconducting. It has been observed that the conductance exponent, n, defined as $G \sim (L_C)^n$, is close to -1.0 for the high densities ($\rho = 10$ μm^{-2}), indicating ohmic conduction, in good agreement with experimental observations in Ref. [15]. The exponent increases to -1.80 at lower densities ($\rho = 1.35$ μm^{-2}), indicating a nonlinear dependence of the conductance on channel length. The asymptotic limit of the conductance exponent for infinite samples with perfect tube/tube contact has been found to be -1.97, which is close to the computed exponent [65,66]. Computations are very sensitive to variations in computational parameters at densities close to the ρ_{th}, which explain the observed difference between the computed conductance exponent and the theoretical exponent. The observed nonlinear behavior for low density is expected because the density value is close to the ρ_{th}. For large densities (>3.0 μm^{-2}), the exponent approaches the ohmic limit, -1.0, with increasing channel length (see Fig. 2(*b*)). Larger exponents, corresponding to nonohmic transport, are observed for the shorter channel lengths. This is consistent with experimental observations, where conductance is seen to scale more rapidly with channel length for small L_C [15].

The conductance exponents discussed in Ref. [44] corresponds to the linear regime of operation where current is directly proportional to applied bias. Pimparkar et al. [40] generalizes this problem to high-bias regime (~high V_{DS}) by solving both the Poisson equations and drift diffusion equation consistently. Their analysis shows that the conductance exponent term in the high bias regime is same as in linear regime.

2.2 Effect of Metallic-Semiconductive CNTs on Device. The electrical performance of CNT networks is strongly influenced by the fact that approximately one-third of the CNTs grown by typical processing techniques exhibit metallic behavior and approximately two-third exhibit semiconducting behavior [39]. This heterogeneity controls the on–off ratio R of typical CNT-network based devices. R has been shown [39] to be a unique and predictable function of L_C, L_t, N_{IT}, f_M, and ρ. Here, N_{IT} is the density of interface traps and f_M is the ratio of the number of metallic tubes to semiconducting tubes in the tube-network. In the conventional transistors, N_{IT} is the trapped charge at the interface of the channel and the insulating dielectric SiO_2, which separates the gate from the channel.

Kumar et al. [39] computed the Gate characteristics (I_{DS}–V_{GS}) and the on–off ratio R at low V_{DS} as a function of tube density ($\rho = 1$–5 μm^{-2}) with device parameters ($L_C = 10$ μm, $L_t = 2$ μm, $H = 35$ μm, and $f_M = 33\%$) corresponding to the experiments in Ref. [15] (see Fig. 3). Here, I_{DS} is drain to source current and V_{GS} is the gate voltage. Their numerical model provides a unique way to find the tube density of typical CNT thin-films by comparing the computed and experimental R and Gate characteristics [39]. This method promises far more accurate estimation of tube density than methods currently in use, such as atomic force microscopy, and scanning electron microscopy [15]. Gate characteristics, represented by I_{DS}–V_{GS} curves, has been computed by taking an average over 50 random realizations of the network. Computations for $\rho = 1$ μm^{-2} agree very well with experiments in Ref. [15] for charge transfer coefficients $c_{ij} = 50$ and $d_{is} = 0$ (see Fig. 3). Increasing ρ increases the number of percolating metallic paths, increasing the on-current I_{ON}, but reducing R, as in Ref. [15]. Snow et al. speculate that $\rho > 3$ μm^{-2} for devices with low on–off ratio (top three solid lines in Fig. 3). The simulations establish that they correspond to exact densities of $\rho = 3.0$, 3.5, and 4.0, respectively. Thus, tube density ρ may be deduced from a simple electrical measurement of the on/off current ratio (see Fig. 3) obviating the need for inaccurate and time-consuming analysis of AFM images, as is currently done. The same methodology can be used to interpret both long channel [15] and short channel data

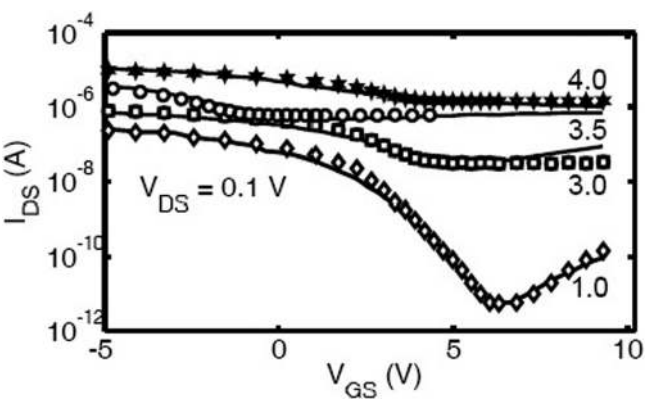

Fig. 3 Computed I_{DS}–V_{GS} at $V_{DS} = 0.1$ V for different densities is compared with experimental results from Ref. [15] before the electrical breakdown of metallic tubes. Solid lines correspond to experimental results from Ref. [15] and markers correspond to computational results. The number after each curve corresponds to tube density ρ. The curve $\rho = 3.5$ μm^{-2} is shifted on the *x*-axis to account for charge trapping [39].

[9] which demonstrates the predictive power of the numerical framework.

Topinka et al. [67] considered the effect of Schottky barrier between metallic tubes and semiconducting tubes in their numerical simulation to analyze the conductance properties of the CNT network. Based on this study, they presented an electronic phase diagram of different types of CNT transistors as a function of the density of the tubes and ratio of metallic to semiconducting tubes [67]. The performance of device in the high bias regime ($\sim V_{DS}$) is performed by Pimparkar et al. using a heterogeneous network of semiconducting and metallic tubes [40,42,43]. Their analysis provides scaling laws to predict the performance of transistors with arbitrary geometrical parameters and biasing conditions, which can be described as a universal formula of current through the device. They also performed a study to investigate the effect of degree of alignment on the device performance and observed that the performance can be maximized for a configuration of the tube network, which lies between a completely random network and a perfectly aligned array [43]. Cao et al. [10] performed device and circuit level simulations to analyze the characteristics of the integrated circuits (ICs) made from CNTN-TFTs. Their analysis shows that the behavior of ICs can be described using standard models for the circuit simulation such as SPICE (simulation program for integrated circuits emphasis) [10].

2.3 CNT-Organic Thin-Films Devices. A novel approach involving modifying the transconductance ($g_m \sim dI_{DS}/dV_{GS}$) of an organic host using a sub-percolating dispersion of CNTs has been proposed in Ref. [68]. A 60-fold decrease in effective channel length, L_{eff}, is observed that results in a similar increase in g_m with a negligible change in on–off ratio [68]. In this technique, the majority of the current paths are formed by the network of CNTs, but short switchable semiconducting links through organic substrate are required to complete the channel path from source to drain [68]. Here, semiconducting organics and CNT-network both play an important role in determining the performance of these devices. The charge transport in the CNT network, in organic and the charge exchange between the CNT network and organic substrate must be considered (see Eqs. (1*a*) and (1*b*)) for modeling transport in these organic TFTs with CNTs dispersion [37].

Kumar et al. [37] simulated for the charge transport in organic TFTs with CNT dispersion using the device parameters $L_C = 20$ μm, $L_t = 1$ μm, and $V_{DS} = -10$ V which are chosen to match the experiments in Ref. [68]. Charge transfer coefficients $c_{ij} = 10^{-4}$ and $d_{is} = 10^{-4}$ are assumed and correspond to poor contact conductance between tube-tube and tube-substrate (see Eq. (1)). The numerical results agree well with experiments over the entire range of tube densities $\rho = 1.5$–17 μm^{-2} (see Fig. 4). An anomalous jump in the I_{DS}–V_{GS} curve for 0.5% volume fraction of CNTs (labeled "shift" in Fig. 4) is observed in Ref. [68] which was not properly understood. The computed I_{DS}–V_{GS} characteristics of this organic TFT device in Ref. [68] with a realistic heterogeneous network of semiconducting-metallic tubes (1:2 ratio) show that this anomalous shift in the I_{DS}–V_{GS} curve is a consequence of the formation of a sub-percolating network of *semiconducting* CNTs in the organic matrix. At 0.2% CNT volume fraction, the semiconducting tubes do not have sufficient density to form a percolating network in and of themselves; metallic CNTs are necessary to achieve percolation. However, when the volume fraction is increased to 0.5%, semiconducting tubes can form a percolating network by themselves, and shift the I_{DS}–V_{GS} curve as shown (see Fig. 4). This confirms that semiconducting CNTs are active elements of this organic TFT device, a feature which was not previously understood [37].

Demonstration of small integrated circuits using high performance CNTN-TFTs and development of computational models that can reasonably explain the characteristics of these devices and predict their performance for a range of crucial parameters suggests that these devices may find their way in many flexible electronics applications [58]. Some challenges still need to be addressed in order to adopt these devices for commercial flexible electronics. Well controlled and scalable methods for filtering metallic tubes from CNT networks needs to be developed, and such methods need not degrade the performance of devices. If metallic and semiconducting tubes are still present in the channel region of the device such as devices fabricated by stripping technique, the interaction of metallic (M) and semiconducting (S) tubes and the effects of S–S, S–M, and M–M junctions need to be well understood as they can significantly affect the device performance. In commercial applications such as liquid crystal displays (LCDs), CNT-devices may be covered or encapsulated by glass, plastic or polymers inside an electronic package. Most of these applications do not require cooling under normal operating conditions because of the use of low-frequency processors (~kilohertz). Increasingly though, the interest is in pushing TFT frequencies into the 1–100 MHz range, and in expanding the range of possible applications [69]. Self-heating is expected to become a severe problem in the high frequency range, especially if no active cooling is used in order to maintain flexibility. The affect of self-heating need to be well explored in order to make necessary design changes in CNTN-TFTs and their circuits such that device temperatures can be maintained below threshold values for enhanced performance and reliability.

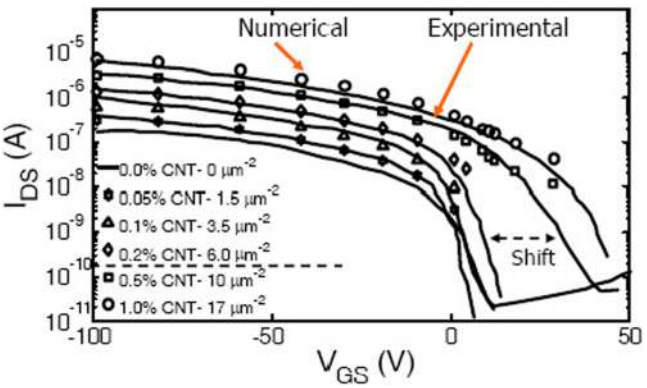

Fig. 4 Computed I_{DS}–V_{GS} at $V_{DS} = -10$ V for different CNT-densities ($\rho \sim 1$–17 μm^{-2}) is compared with experimental results in Ref. [68]. The vol. % of CNT dispersions used in the experiments and the corresponding network density (ρ (μm^{-2})) used in the computations are shown. $L_t = 1$ μm, $L_C = 20$ μm, and $H = 200$ μm. The shift in the I_{DS}–V_{GS} curves due to the initiation of semiconducting CNT percolation for CNT vol. % >0.2% is shown by the dashed arrow [37].

We turn our attention to CNT array interface structures used for thermal management in the Sec. 3. CNT arrays are promising candidates for low resistance thermal interface materials in electronic packaging applications. We present the different component resistances that sum to produce the total resistance of the CNT array interface, discuss the effect of interface pressure and contact resistances and identify the critical bottlenecks to heat conduction in such structures.

3 CNTs Arrays as Thermal Interface Materials

The combination of high thermal conductivity and high mechanical compliance are difficult to achieve with most materials; yet, such characteristics are desired for high-performance thermal interface materials where the intrinsic resistance of the material should be low and the contact area in the interface should be high. These characteristics can be achieved to varying degrees by tuning the properties of CNT ensembles. Random networks of CNTs have been shown to improve thermal interface resistance [22]. However, as discussed in detail below, several groups have shown that more significant improvements can be achieved by aligning CNTs in arrays, along the direction of heat flow. This approach

minimizes the effects of intertube interface resistance and void space on the effective thermal conductivity of the ensemble. The thermal conductivity of CNT arrays is usually 1–2 orders of magnitude higher than the thermal conductivity of traditional TIMs [25–27], yet these values are still an order of magnitude less than the values for individual tubes [2,3]. The effective thermal conductivity of vertical arrays of CNTs can be improved by increasing the number density of CNTs in the array. However, increased CNT number density stiffens the array [45], thus, a compromised between high thermal conductivity and mechanical compliance must be reached. As shown in detail below, the resistance at CNT-substrate contacts comprises the majority of the total interface resistance in most applications of vertically oriented CNT arrays because the relatively high thermal conductivity of the CNT arrays produces negligible resistance for moderate array heights [45]. Reducing CNT-substrate resistances and optimizing the thermal conductivity, height, and mechanical compliance of CNT arrays for specific applications will be required for CNT array TIMs to gain wide use as electronic packaging materials.

The most actively studied CNT array interface structure is the "one-sided" CNT array interface that consists of CNTs directly grown on one substrate with CNT free ends in contact with an opposing substrate (see Fig. 5). This structure has produced some of the lowest resistances measured for CNT TIMs to date. The numerous CNT contacts at both substrates form parallel heat flow paths within the framework of the thermal resistance network illustrated in Fig. 5. This network shows thermal resistances resolved at the individual nanotube level for true CNT-substrate interfaces, both at the growth substrate (with a nanotube number density of N, in contacts/area) and at the opposing interface (with a contacting nanotube number density of n). The resistance at each local CNT-substrate contact can be modeled as two resistances in series [45]: (1) a classical substrate constriction resistance (R_{cs}) and (2) a resistance (R_b) that results from the ballistic nature of phonon transport through contacts much smaller than the phonon mean free path in the materials ($\sim$100 nm). The ballistic resistance (R_b) is usually orders of magnitude larger than R_{cs} for CNT-substrate contacts, which are typically $\sim$10 nm.

The remaining resistance (R''_{array}) is from heat conduction through the CNT array. This *effective* resistance is defined for the entire array (including void spaces) to simplify the modeling effort. Moreover, this quantity has been measured in prior work for representative samples and that can be used to interpret experimental results that only measure overall thermal interface resistance. When array height is less than 50 μm, R''_{array} is usually negligible in comparison to the resistances at the CNT-substrate contacts [45].

Given knowledge of the contact number densities at the growth substrate (N) and the opposing substrate (n), an overall or total interface resistance can be calculated. The former density (N) can be estimated from scanning electron micrographs of synthesized arrays, and the latter density (n) can be estimated using a recent model that predicts real contact area in CNT array interfaces as a function of applied pressure and important array characteristics such as porosity and CNT diameter [45]. The model reveals that fabricating arrays with low effective compressive modulus is critical for establishing large interfacial contact and minimizing total thermal resistance. A detailed development of the CNT array TIM resistor network model is presented elsewhere [45]. Applying the model to one-sided CNT array interfaces with a surface density of 10^8 CNTs/mm^2 and CNT diameters of 20 nm, suggest that total resistances of $\sim$0.1 mm^2 K/W represent *limiting values* that could be achieved if the CNTs are completely and perfectly contacted and have well-matched acoustic impedances at all CNT-substrate interfaces.

3.1 CNT TIM Structures. The three CNT array TIMs shown in Fig. 6 have exhibited some of the most promising thermal performance characteristics to date. The first is the one-sided interface structure discussed above. The second configuration, i.e., the "two-sided" configuration, consists of CNT arrays adhered to surfaces on both sides of the interface and brought together in Velcro^{TM}-like contact (in this configuration CNTs mechanically entangle and are attracted to each other by van der Waals forces). The third structure comprises vertically oriented CNT arrays directly and simultaneously synthesized on both sides of thin foil substrates that are inserted into an interface. The CNT-coated foil structures are particularly attractive in that they serve as a method for applying CNT arrays to interfaces between heat sinks and electronic devices that would experience damage from exposure to the high temperatures normally required for high-quality CNT

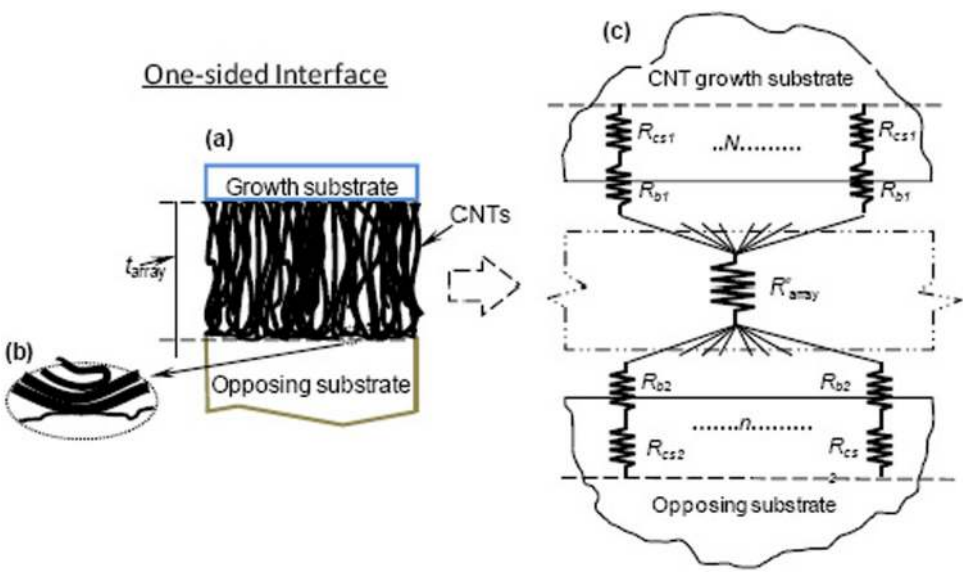

Fig. 5 (*a*) Schematic (not to scale) of an interface with the addition of a vertically oriented CNT array of thickness t_{array} [24]. (*b*) Buckled CNT contacting an opposing surface with its wall. As shown some CNTs do not make direct contact with the opposing surface. (*c*) Resistance schematic of a one-sided CNT array interface between two substrates, showing constriction resistances (R_{csi}), phonon ballistic resistances (R_{bi}), and the effective resistance of the CNT array (R''_{array}).

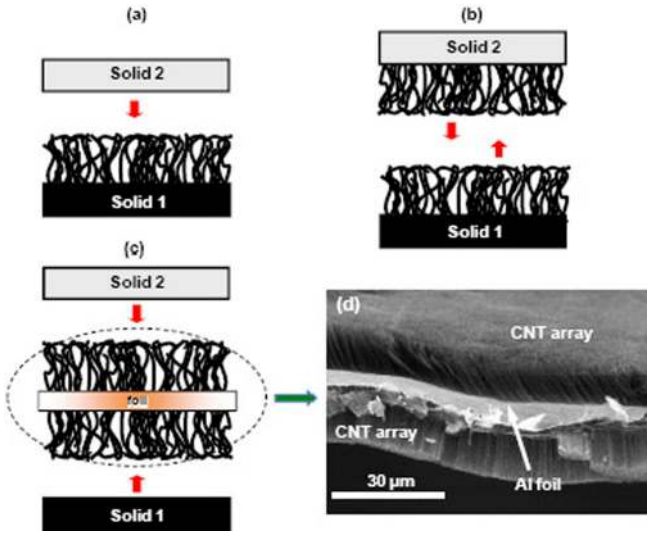

Fig. 6 CNT array interface structures. (*a*) An example one-sided interface. (*b*) An example two-sided interface. (*c*) An example CNT-coated foil interface. (*d*) CNT arrays on both sides of 25 μm-thick Al foil [24].

growth (>700 °C). Using the CVD processes that are ubiquitous in the electronics industry, the CNT array TIMs in Fig. 6 have been grown on various substrates such as silicon, silicon carbide, copper, and aluminium that are important for thermal management in electronics, MEMS and NEMS applications [24].

3.2 Thermal Resistances of CNT Interfaces. Xu and Fisher reported some of the earliest results in applying CNT arrays as thermal interfaces, with interface resistances less than 20 mm^2 K/W for dry one-sided structures [49] and less than 7 mm^2 K/W for CNTs directly synthesized on Si and then enhanced with a phase-change polymer [50]. Since then, several others have explored using CNTs (and carbon nanofibers (CNFs)) to improve contact thermal conductance [47,48,51,70–82]. Ngo et al. [76] used electrodeposited Cu as a gap filler to enhance the stability and thermal conductance of CNF arrays and reported a thermal resistance of 25 mm^2 K/W under a pressure of 414 kPa for Si–Cu interfaces enhanced with such structures. At moderate contact pressures thermal resistances of approximately 12 mm^2 K/W were measured by Xu et al. [51] for a Si–CNT–Ni interface, and by Tong et al. [79] for a Si–CNT–glass interface; these values are very close to the result presented in Ref. [25]. Amama et al. [70] measured thermal resistance values of approximately 8 mm^2 K/W at a pressure 350 kPa for Si–CNT–Ag interfaces, and Cola et al. [47] measured the resistances of a two-sided interface to be near 4 mm^2 K/W at moderate contact pressures. Zhang et al. [82] recently applied CNT arrays with optimized synthesis conditions to enhance the brightness and efficiency of light-emitting diodes and achieved resistances as low as 7 mm^2 K/W for a Si–CNT–Al interface at a contact pressure of 150 kPa. Resistances as low as 7 mm^2 K/W were also measure by Cola et al. [46] for a one-sided Si–CNT–Ag interface.

Figure 7 summarizes the performance of one-sided, two-sided, and CNT-coated foil interfaces as a function of pressure [46–51]. For these configurations, the pressure dependence is weak in the measured range because the CNTs are compressed near their maximum extent within the measurement range [45]. Resistances as low as 8 mm^2 K/W were produced with the CNT-coated foil TIMs [48]. The CNT-coated foils enhance real contact area significantly, which results in low contact resistance, because deformation of the thin foil substrate "assists" CNT displacement to match the topology of the matting surfaces.

A few groups have measured thermal resistances of CNT array TIMs using transient techniques that allow the true CNT-substrate resistances and the resistance of the CNT array to be independently resolved [47,77,79]. Such measurements confirm that the resistances at CNT-substrate contacts are much larger than the intrinsic resistance of the CNT array, and that the resistance at the interface between CNT free ends and an opposing substrate is considerably larger than the resistance at the CNT-growth substrate interface—the true contact area established by weakly bonded van der Waals forces between CNT free ends and the opposing substrate is considerably less than the contact area at well anchored CNT roots. Figure 8 illustrates a one-sided interface with local resistances at true CNT-substrate contacts highlighted. The resistance between CNT free ends and the opposing substrate is clearly the largest resistance in the network. The thermal resistances at the CNT free ends also comprise the largest percent of total resistance in the two-sided and CNT-coated foil configurations [47,48].

Techniques to improve CNT-substrate bonding and contact area, especially at contacts to free CNT ends have been explored recently by a few groups. Bonding free ends by reflowing thin indium layers [79], using gold coatings on CNTs and substrates for gold-gold thermo-compression bonding [83], or combining CNT arrays with traditional TIMs that wet the interface well (e.g., phase change materials) [50,84], produced thermal resistances that were an order of magnitude lower than the resistances of one-sided interfaces in dry contact (on the order of 1 mm^2 K/W). Each method reduced interface resistance by presumably connecting more CNTs and establishing more contact area at the interface to free CNT ends. While these techniques have shown much promise, continued research is required in this direction to develop more reliable and scalable methods, and to reduce thermal resistance further. Hamdan et al. [85] recently combined a patterning technique with gold–gold thermo–compression bonding and measured a low total resistance of approximately 4 mm^2 K/W.

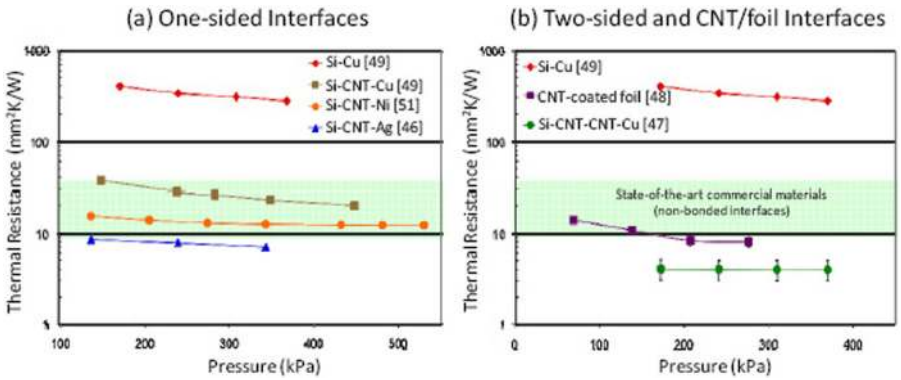

Fig. 7 Room-temperature thermal resistances as a function of pressure. (*a*) One-sided CNT array interfaces. (*b*) Two-sided CNT array interfaces and CNT-coated foil interfaces.

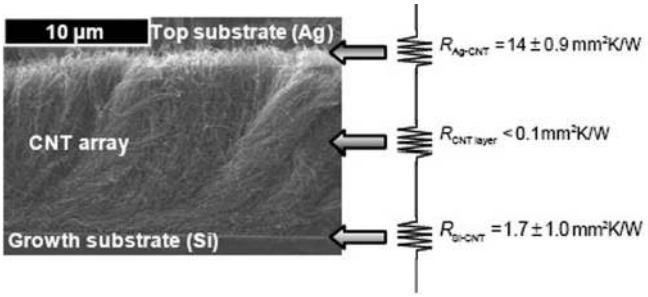

Fig. 8 True contact resistances for a one-sided Si-CNT-Ag interface at 0.241 MPa measured at room temperature using a photoacoustic technique [47]

Patterning the CNT array into periodically spaced pillars, as was done in Ref. [85], reduces the CNT number density in the array, which likely increases the mechanical compliance of the array, allowing more contact area to be established at the interface to free CNT ends during thermo–compression bonding. Future studies should continue to focus on techniques to reduce thermal resistance of CNT arrays via an increase in the mechanical compliance of the arrays. Some preliminary data on thermal and mechanical cycling of CNT array TIMs in a burn-in application have been reported [86], and these results demonstrated no change in performance of CNT array TIMs after 1000 thermo-mechanical cycles. The CNT arrays were also shown to be well adhered to the substrate before and after cycling. Much work is still needed to fully understand the performance characteristics of CNT array TIMs during thermal cycling of real devices.

In the Sec. 4, we discuss how thin-films of CNTs can be used as transparent electrodes for electronic devices. The different methods for the manufacturing of these electrodes, the impact of processing and doping of CNT films on their conductance and transparency properties and the integration issues of these electrodes with devices are discussed.

4 Transparent CNT Electrodes for Electronics

High conductivity transparent electrodes are critical to the performance of a wide range of solar photovoltaic, display, and optoelectronic applications. Typically, indium tin oxide is the most commonly used material due to its excellent transparency in the visible range and low sheet resistance which can reach levels on the order of 10 Ω-sq^{-1}. While such properties make the use of indium tin oxide (ITO) nearly ubiquitous in devices needing transparent electrodes, there are still several limitations to this technology. First, ITO is a brittle material with limited strain to failure. Thus, applications which require transparent electrodes in flexible electronics are limited in their deformation due to the strain limitations in ITO. Second, the surface of ITO is not chemically stable. A number of cleaning methods have been used to increase the conductivity of the ITO and chemical methods have been used to try and stabilize its work function. Nonetheless, there is an impetus to find replacements for ITO for use in electronics, especially those involving flexural deformation.

Carbon nanotube networks are one of the materials currently under development to replace ITO and other transparent conductive oxides in flexible-electronic applications. Electrodes comprised of SWNTs are an appealing choice as a surrogate for ITO in organic electronics because of the extraordinary electrical and mechanical properties these 1D structures possess. Exploiting the metallic behavior of SWNTs is desired because individual SWNTs can support electrical current densities exceeding 10^9 A-cm^{-2} [87] while SWNT ropes and bundles of individual SWNTs have demonstrated axial conductivity values as high as 10,000–30,000 S-cm^{-1} [88]. In addition to significant electronic potential, SWNT electrodes have been shown to exhibit sustained electrical performance under extreme bending conditions [89]. The higher

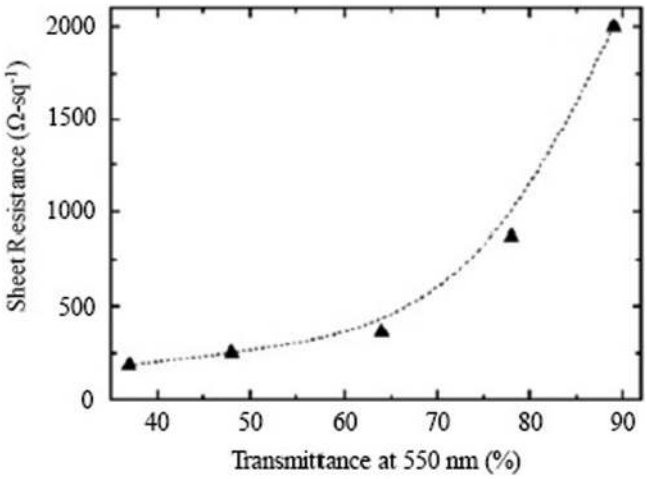

Fig. 9 Correlation between transparency and R_{sh}. Film transparency represented by transmittance at 520 nm. Taken from Ref. [109].

work function of SWNTs (ca. 5.0 eV) [90] in comparison with ITO (ca. 4.3–4.7 eV) may provide a more optimal hole injection into typical OLED hole transport layers due to the reduced energy barrier arising from the difference of the organic HOMO level and the positive electrode work function [91]. Additionally, a larger selection of organic materials compatible with the high work function of SWNTs may also be available. Moreover, SWNT films can be processed at room temperature under ambient conditions, which increases the range of substrate compatibility.

While these properties have led researchers to develop transparent conductors based on carbon nanotubes, it must be realized that CNTs are very strong optical absorbers. While thick or dense films show lower sheet resistance, they also result in highly absorbing films in the optical regime (Fig. 9). In addition, the electrical junctions between tube contacts can results in additional resistance beyond that seen in the intrinsic resistance of the CNTs. Thus, the many junctions required by relatively short CNTs (e.g., >1 μm) can add significantly to the overall film resistance. For these reasons, it is highly desired to have long CNTs which are single-walled (reduce optical absorption) with low contact resistance between the CNTs. Research has shown great improvements in CNT electrode performance with type sorted CNTs where the tubes are >95% metallic or semiconducting. Such films limit Schottky barrier resistance at the tube junctions resulting in improved sheet resistance [92].

4.1 Manufacturing of SWNT Electrodes. The most common method for making SWNT electrodes is the use of vacuum filtration (Fig. 10) [93,94] This method provides consistency in

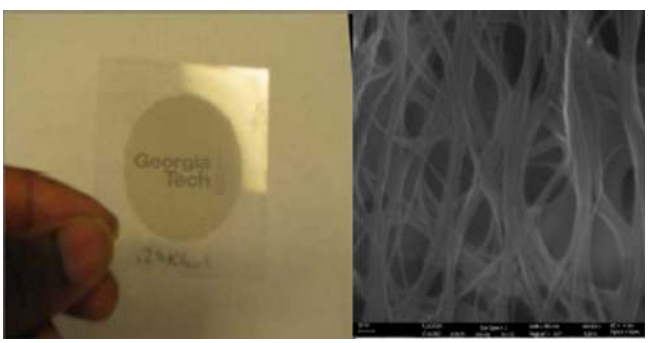

Fig. 10 Picture show vacuum filtered CNT electrode on a PET substrate (left) and an SEM image showing the details of the CNT network (right)

uniformity of the electrode due to the variable change in conductance of the membrane filter with CNT thickness, but lacks in the potential for scalable processing. Two primary methods exist for transferring the filtered SWNT film from the vacuum filter to the desired substrates: via an elastomeric PDMS stamp [95] or through chemical exposure of the filter and film such that the filter paper dissolves away [93]. Aguirre et al. [96] used this method to fabricate a SWNT film with a R_{sh} of 250 Ω-sq^{-1} and 80% transmittance at 520 nm. The rms surface roughness of the film was 12 nm. Wu et al. [93] were able to produce a SWNT film with a R_{sh} of 30 Ω-sq^{-1} and transmittance greater than 70% over the visible spectrum. The R_{sh} and corresponding transmittance of this film represent the best reported optoelectronic properties of SWNT films in the literature.

Mayer rod and spray coating are another popular and scalable approach to producing large area SWNT electrodes [94]. In this simple approach, SWNT solutions are directly coated or sprayed onto substrates via a wire wound rod, air brush pistol or ultrasonic spray tool. The substrate is kept hot during the process (~100 °C) to accelerate drying of the fine solution droplets on the surface [97]. While the airbrush technique provides a simple and quick method to tune film thickness, significant heterogeneity on the nanometer scale can exist [97]. Geng et al. [98] demonstrated that low R_{sh} films could be produced using spray deposition. By producing films with R_{sh} of 160 Ω-sq^{-1} and transmittance of 80% at 550 nm, An acid treatment process was subsequently used to remove residual surfactant and further decrease R_{sh} by a factor of ~2.5 to a final value of 70 Ω-sq^{-1}.

The successful deposition of SWNT films by spray coating with high surface uniformity and low surface roughness was recently achieved by Tenent et al. [99]. They attributed the improved surface properties to two major advances: (1) aqueous SWNT solutions were dispersed using a polymeric derivative of cellulose (sodium carboxymethyl cellulose (CMC)) and (2) ultrasonic spraying of the solution onto the substrate. While other spray techniques utilize SDS to disperse SWNTs [97], CMC was found to disperse 20 times the amounts of SWNTs into water than possible with SDS. Due to the strong binding between CMC and the SWNTs, individual nanotubes were isolated and suspended with more gentle sonication and centrifugation than typically required for SDS. Their data suggested that approximately 95% of the SWNTs in the CMC based dispersion were individual in nature versus aggregated bundles. The rms roughness of sprayed films was 3 nm over a 10×10 μm area. This surface roughness is much lower than that obtained using typical vacuum filtration methods and results in improvements in device yields when integrated with organic electronics. After removal of the CMC polymer via overnight exposure to 16 M HNO_3, low R_{sh} values of 150 Ω-sq^{-1} with 78% transmittance at 550 nm were obtained for sprayed SWNT films. This work represents an easily scalable SWNT film deposition technique, as the authors demonstrated the first optically homogenous 6×6 in. SWNT film on glass.

4.2 Impact of Post Processing on SWNT Electrodes. To enhance the conductivity of SWNT films while retaining high transmittance, Zhang et al. [29] carried out chemical doping using thionyl chloride ($SOCl_2$). After $SOCl_2$ treatment, R_{sh} decreased by a factor of 2.4–160 Ω-sq^{-1} with a transmittance of 87% at 550 nm. The SWNTs used in the films studied by Zhang et al. contained high levels (4–6 at. %) of carboxylic acid groups covalently bonded to the SWNT sidewalls and ends. Upon immersion in $SOCl_2$, the carboxylic acids were converted to more electronegative acyl chloride groups [100–102] which further p-doped the CNTs. Via immersion in 12 M HNO_3 for 60 min, Geng et al. [103] increased the conductivity of transparent SWNT films by a factor of 2.5. Additional work has shown that the use of a combination of nitric acid and thionyl chloride can lead to increased doping of CNTs as seen in Fig. 11. While it has been noted that

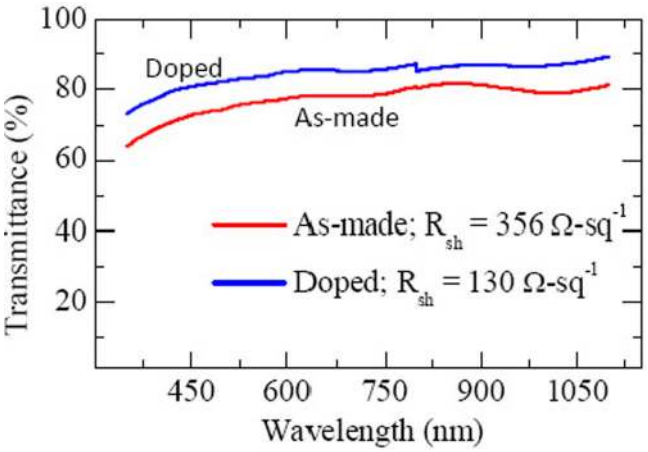

Fig. 11 Data showing the transmittance versus wavelength for doped and undoped SWNT electrodes. Doping was performed with thionyl chloride and nitric acid.

SWNT electrode doping is not stable in air, Jackson et al. introduced a capping technique using PEDOT:PSS to create doped CNT electrodes with long term air and thermal stability [100].

While doped heterogenous CNT networks generally yield sheet resistances greater than 100 Ω-sq^{-1} with transmittances greater than 75%, recent advancements have been made in the use of SWNTs of homogenous electrical type. Type sorted CNTs using centrifugation have now become commercially available. Using vacuum filtration methods and combined thionyl chloride and nitric acid doping, sheet resistances as low as 60 Ω-sq^{-1} have been obtained for semiconducting CNTs and 76 Ω-sq^{-1} for metallic CNTs at 70% transmittance [104]. The use of type sorted CNTs helps to eliminate some of the Schottky barriers which exist in mixed nanotube films. Such films also allow for tuning of electrical properties through controlling Fermi level shifts by doping as well as the density of carriers in the tubes by tube diameter which controls the density of states. While these films show excellent sheet resistance values, integration issues still remain with devices. In general, the sheet resistance remains too large for large area devices such as photovoltaics and large area OLEDs. Thus, the use of metallic grids with CNT electrodes will become necessary for device integration to reduce resistive losses.

While continued research has shown the ability to process low sheet resistance carbon nanotube electrodes, additional work is still needed. It is well known that the sheet resistance depends on CNT length, the resistance between the CNT bundles in the array and packing density. To address some of these issues, researchers are investigating the use of double wall CNTs which are less prone to breakage during sonication and dispersion steps, resulting in longer CNTs which enhance the electrical conductance [105]. Additional research has promoted methods to ensure complete removal of surfactants from CNT interfaces to reduce tube-to-tube electrical contact resistance. While washing with water and the use of nitric acid has been shown to remove surfactants like SDS, more aggressive steps such as thermal annealing must be used to remove surfactants such as sodium cholate. Alternate doping methods which may result in improved stability are being pursued based on the incorporation of metal nanoparticles such as Fe, Pd, Au, Co, and Ni via electrochemical deposition or noncovalent bonding from thiolated solutions [94,106]. Finally, since the CNT network is filled with voids, additional method to bridge these nonconductive areas with conducting materials is being sought [107,108]. One such method involves the creation of CNT-Graphene composites. Preliminary studies have shown such materials to be very effective when combined with single or bilayer graphene sheets which improve sheet resistance while only absorbing 1%–1.5% optical transmission in the visible range. Additional work on CNT composite electrodes has the potential to bring

about revolutionary changes in the electrical performance of CNT based electrodes.

5 Conclusions

In summary, developed computational models for the electrical transport in CNTN-TFFs has good capability to predict the device characteristics for different geometrical parameters and biasing conditions. The model has been validated against experimental data for a wide range of CNT network densities consisting of both metallic and semiconducting tubes and in the presence or absence of a conducting substrate such as semiconducting organic matrix. Reasonable matches with experimental data have established the general validity and robustness of the model. Nevertheless, a number of important issues remain to be addressed. The model employs electrical contact parameters c_{ij} and d_{is}, which are dependent on experimental conditions. These must be determined either from careful experiments or from atomistic simulations of tube-tube and tube-substrate contact. CNTN-TFTs have been targeted for high frequency applications where power dissipation in device can be high and self-heating can have consequences for the thermo-mechanical reliability of flexible substrates. It is therefore necessary to understand the interaction of electrical and thermal transport in determining device performance and reliability. Regarding the fabrication of CNTN-TFTs, the processing techniques must be improved to grow electronically homogeneous CNTs with a good control on the length and diameter and advanced methods must be developed for precise control of density of CNTs in their networks.

In the context of thermal management applications, three CNT array TIM configurations have been developed to the point where they produce resistances that compare favorably to the best TIMs currently in use. So far, the lowest resistances produced by CNT array TIMs are on the order of 1 mm^2 K/W. Further improvements can be achieved by optimizing the compliance of CNT arrays to maximize the real contact area in the interface. Experimental data and theoretical predictions reveal that the resistances at CNT-substrate contacts severely limit the potential of CNT array TIMs. Improvements in bonding and thermal transport at these contacts can lead to substantial reductions in resistance, approaching estimated theoretical limits of $\sim$0.1 mm^2 K/W. For applications as replacement of transparent conductive electrodes, CNT films have shown promise in light of the recent improvements in sheet resistance. In addition, mechanical robustness makes these films excellent candidates for use in flexible devices where the mechanical integrity of transparent conductive oxides is a limitation. While sheet resistances as low as 60 Ω-sq^{-1} have been obtained, it is still necessary to work on manufacturing methods to continue to reduce surface roughness and to address the integration of metallic grids in order to improve yield and allow integration with large scale devices.

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