



A Review of High Frequency Power Converters and Related Technologies

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A Review of High Frequency Power Converters and Related Technologies

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A Review of High Frequency Power Converters and Related Technologies

Abstract—Development of power electronic converters tend to achieve high efficiency and at the same time high power density in many industrial applications. In recent years, with emerging third-generation semiconductor materials i.e. Silicon Carbide (SiC) and Gallium Nitride (GaN), the switching frequency of several MHz has become a widely studied frequency band, therefore traditional technology can no longer meet the demand, and many new challenges appear. This paper presents a comprehensive review of high frequency (HF) converters, the essential challenges are analyzed such as topology selection, soft-switching technologies, resonant gate drivers, magnetic components design and optimization.

Index Terms— High frequency, converter, soft-switching resonant gate driver, magnetic components

I. INTRODUCTION

In the past several decades, the power conversion technology achieved fast development, and the characteristics of high efficiency and high power density are extremely expected in many fields, such as light emitting diode (LED) drivers, electric vehicles, and consumer electronics, especially in the frequency of several MHz [1-3]. Passive elements i.e. inductor and capacitors mainly decide the volume, weight and cost of power electronic converters, which scales with switching frequency, therefore increase in switching frequency will lead to converter miniaturization and cost reduction [4-6]. However, the increment of switching frequency also brings new challenges, the switching loss and magnetic loss are proportional to the switching frequency and this limits the system efficiency at high operating frequency. At the same time, many standards have put forward more stringent requirements to system efficiency. In order to solve the contradiction between efficiency and operating frequency, improvements can be made in topology, drive circuit and magnetic components these three main aspects. Besides, power switching devices based on wide-bandgap (WBG) devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) with both lower output capacitance and ON resistance (R_{ds_on}) comparing to their Si counterparts are widely applied to power converter design in recent years [7-8]. The commercialization of WBG devices promotes the development of HF converters. SiC and GaN are both WBG devices, but their material properties, device architectures are different and therefore, the output power, voltage level, performance capabilities are different. From an electrical point of view, in the low-to-medium voltage range (below 1200V), the switching losses of GaN are about three times less than SiC at 650V. Regarding operating frequency, most silicon-based designs today work at 60–300kHz. If the switching frequency goes 500kHz or higher, this can only be accomplished with GaN. SiC

is generally designed for working voltages of 650V, 1200V and higher. Because of the maximum junction temperature of SiC, SiC always works in hot and hostile environments.

Fig. 1 is power versus frequency diagram of different devices [9]. Compared with the WBG devices, the switching speed, forward voltage drop, and voltage blocking capability of Si devices are all weaker. Therefore, application of WBG devices can improve the performance of HF converters. To be more specific, SiC technology is finding application in higher-power products and GaN is moving towards HF.

GaN, as one of the representatives of the WBG devices, has a high market share in HF applications, promoting further development of the semiconductor field. Fig. 2 shows 2019-2025 GaN radio frequency market forecast by application [10]. As the figure shows, the whole market is rising at a compound annual growth rate (CAGR) of 12% from \$740 million to more than \$2 billion by 2025. Telecom infrastructure, military applications and SATCOM are the main applications. Many large companies and research institutions have done much research on GaN and relevant products are commercial.

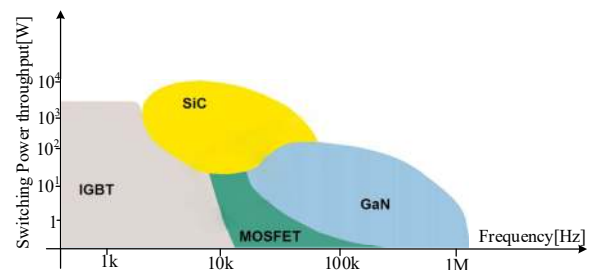


Fig. 1. Power versus frequency diagram of different devices.

2019-2025 packaged GaN RF device market forecast— split by application

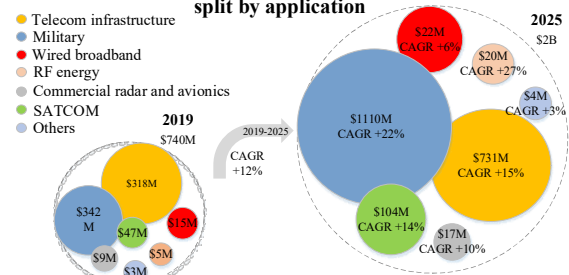


Fig. 2. 2019-2025 GaN radio frequency market forecast by application.

Based on the above analysis, the development of the WBG devices has promoted the frequency of power electronic converters. In addition to devices, switching loss can be reduced in terms of topology selection. For the sake of system efficiency, soft switching characteristic is a critical property for HF converters in which even though conduction losses might

accordingly increase. Resonance topologies such as LLC and Class-E have gained much attention [11-14], and for other non-resonance topologies, quasi-resonance technology, active-clamp and zero-voltage-switching (ZVT) may be alternatives [15-17]. On the other hand, the loss of traditional gate driver increases with the increment of switching frequency, and the system efficiency will be significantly reduced. Besides, the effective driving current provided by the hard driving circuit is small, which causes long switching time, and it is difficult to meet the demand of high-frequency power converters. Therefore, the resonant gate driver is widely used in HF applications.

The other challenge is the losses of inductors and transformers. Nevertheless, weight and volume of magnetic elements will decrease correspondingly with high switching frequency, the core loss and winding loss will also increase rapidly. Moreover, for soft-switching operation, magnetic components stress is much higher due to resonant voltage and current, and in fact, some losses are shifted from semiconductors to magnetics. Recent years, for low power applications (below 5 kW), planar magnetics with low profile are more and more widely adopted in high-frequency converters to reduce the height and volume of converters [18-20]. The planar magnetic component can effectively increase the heat dissipation area and its volume is only 20% of that of the conventional winding magnetic component under the same power. Nevertheless, their performance suffers from large planar winding capacitance in HF and high voltage (above 200V) applications.

This paper mainly focuses on the key problems in HF converters. In Section II, the common topologies of HF converters are divided as resonant converters and non-resonant converters. Then Section III presents conventional gate drivers, resonant gate drivers and current source drivers. Section IV studies loss reduction magnetic components and their optimization approaches. Section V discusses and prospects the trend of HF converters as well as the associated challenges. Finally, Section VI gives conclusions.

II. TOPOLOGY OF HIGH FREQUENCY CONVERTERS

In order to solve the high switching losses caused by the increment of switching frequency, soft-switching topologies, zero-voltage, zero-current or both, are needed. Fig.3 shows the classification of soft-switching converters. In general, the soft switching converters can be divided based on their operating principles, into two main types: resonant converters and non-resonant converters. According to the number of resonant elements, the resonant converters can be divided into two-elements, three-elements and multi-elements. Non-resonant converters can be divided into quasi-resonant converters, active-clamp converters, ZVT converters and so on, depending on different technologies. In this section, different HF converter topologies are reviewed.

A. Resonant Converters

Resonant converters, which are split as series resonant, parallel resonant and series-parallel resonance converters, are preferred in HF applications. Among them, the series-parallel resonance circuit (SPRC, also called LLC) as shown in Fig. 4

has well balanced resonant networks and thereby obtains advantages of both series resonant and parallel resonant topologies. The most attractive characteristic of the LLC resonant converter is that all the devices can achieve zero voltage switching (ZVS) over the entire load range, and the secondary-side synchronous rectification (SR) switches can also achieve zero current switching (ZCS) when the converter operates at or below the resonance. Though design and control process of LLC are quite mature, appear new challenges, when applied to HF applications and combined with devices based on WBG. For instance, in HF applications, the value of passive components i.e. inductors and capacitors decrease significantly, therefore, the parasitic parameters such as leakage inductance of HF transformers and stray capacitance can no longer be ignored. Therefore, the design of passive components becomes very crucial. At the same time, the characteristics of the driving circuit directly affect the performance of switch, as SiC and GaN switching with high dv/dt and/or di/dt are sensitive to parasitic parameters in the circuit. The design of driving circuit and printed circuit board (PCB) layout are also important issues to be solved.

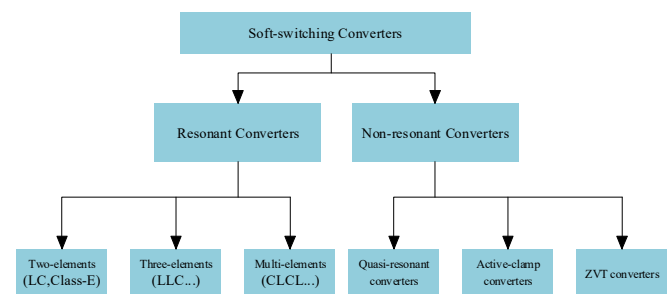


Fig.3. Classification of soft-switching converters.

Paper [21] first presented the benefits of GaN devices in a 300-W, 1-MHz LLC resonant converter by quantitative analysis, comparing with Si-based converter, 24.8% loss reduction was achieved, and the full-load efficiency was up to 96.6%. However, in the high switching frequency condition, ZVS failure cannot be predicted accurately by only considering traditional constraints. To solve this problem, paper [22] investigated the failure mode of LLC in detail and an accurate ZVS boundary is proposed for HF design, and the proposed theory was verified on a 1 MHz, 1500W LLC prototype. At the same time, in HF applications, the power stage design must take secondary leakage inductance into account because it can affect the voltage gain. Paper [23] proposed a modified LLC resonant converter model that incorporates the secondary leakage inductance for more accurate operation. The team of Prof. Fred C. Lee in Virginia Tech also do a lot of research in HF LLC and represents the current advanced level [24-25]. The power density of the 1MHz kW level LLC converter is up to 900W/in³. (~55W/cm³)

However, there are some inevitable disadvantages of LLC converter. For example, LLC converters are always designed working around the resonant frequency for higher system efficiency, and in this case, the voltage gain of the resonant tank

is about 1. Therefore, in order to achieve step-down function, the transformer **turn ratio** should be high enough to achieve desired voltage ratio between input and output voltages. Besides, LLC converters usually suffer a wide frequency variation range when adjusting the system voltage gain, which is not conducive to parameter design.

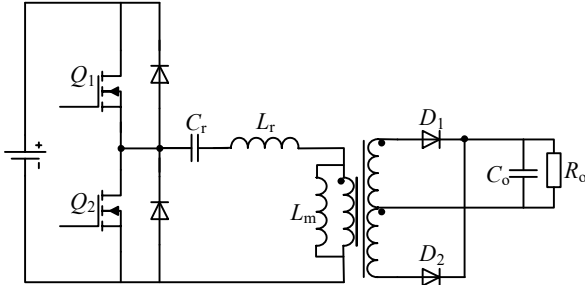


Fig.4. The circuit of LLC converter.

Wang *et al.* proposed a CLCL resonant topology which is also suit for **HF** applications with satisfactory soft switching characteristic [26]. The typical circuit is shown in Fig.5, and with a resistive impedance of resonant tank, the switches can turn on in ZVS condition and turn off in ZCS condition at full load operating condition. Moreover, the diodes can also achieve ZCS turn-off. With the application of GaN switch and optimized planar magnetic components, the efficiency of a 1-MHz 20W prototype is up to 90.9%. This topology is also suitable for high power applications [27].

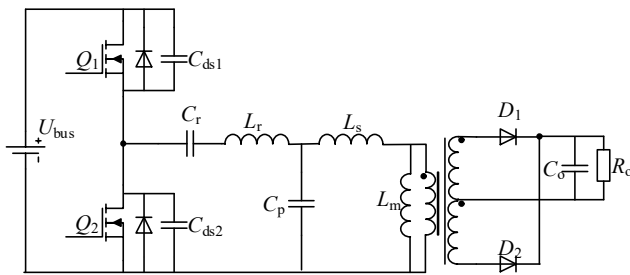


Fig.5. The circuit of CLCL converter.

Class E converter as shown in Fig.6 is another approach of resonant conversion. This kind of converter is simple and efficient at high-frequency operation with only one active power switch [28-30]. Although it shows great potential in **HF** DC/DC converter, it also increases the voltage stress over the switch, greatly limiting its application. Moreover, its ZVS performance is sensitive to the load condition and additional compensation network must be designed to alleviate this sensitivity.

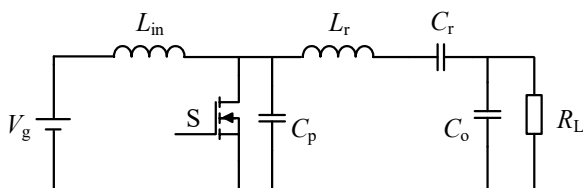


Fig.6. The circuit of Class E converter.

B. Non-resonant Converters

For those converters without soft switching characteristic innately, in order to be applied in **HF**, some measures need to be taken, therefore quasi-resonant converters are proposed. One simple solution is to add an auxiliary LC resonant circuit to shape the current and voltage of main switches during turn-ON or turn-OFF transition. The passive resonant elements are connected in series or in parallel with the main switches. In paper [31], a 1MHz modified **single ended primary inductor converter (SEPIC) converter** with ZVS characteristic and high voltage gain is proposed, as shown in Fig.7. An additional capacitor C_Q is in parallel with the switch and the current of inductor L_2 is designed to be reversed to form the LC resonant cell, therefore, ZVS is achieved, which makes the converter can be used under **HF**. The efficiency is 90.91% at full load 36W. Similar methods are applied in paper [32-35].

Some resonant cell can also be added in converters to realize soft switching. Paper [36] proposed an input current fed (ICF) cell and an output current sink (OCS) cell, as shown in Fig.8. With these two cells, ZVS on and quasi ZCS off for switch are both achieved, which can be extended to push-pull, full bridge, half bridge, and other dual end topologies. For high power level applications, these two cells can also be combined in parallel and series connection.

Besides the aforementioned methods, active-clamp is another technique to realize ZVS and high efficiency operation, which is adopted in isolated Flyback or forward converters [37-40]. Compared with traditional single-ended reset techniques, the active clamp technique cannot only absorb leakage energy but also have the advantages of lower voltage stress on the main switch, soft switching characteristic, reducing electromagnetic interference (EMI) and duty cycle operation above 50%. It can also be used in non-isolated dc-dc converters, such as Buck and Boost [41-42]. Paper [43-44] proposed several active-clamp converters, but the unclamped voltage spike on output rectifier is inevitable. In this circumstance, high voltage rating device is needed and the efficiency is impacted. With a clamp diode, this voltage spike can be prevented [45], but the energy dissipated in the clamp circuit and it does not help improve the efficiency. In general, the active-clamp converter is not suit for high current applications because of the conduction loss in auxiliary and synchronous switches are significant. However, for low current (<10A) applications, active-clamp based topologies are a good choice at MHz switching frequency [46].

Besides active-clamp, zero voltage transition (ZVT) [47-48] is an active soft switching technique preferred for the converters in which MOSFET is used as an active switch. Converters using this soft switching technique operate as regular **pulse width modulation (PWM)** converters during almost the whole switching period. This technique can reduce MOSFET switching loss. However, ZVT always suffers from large number of passive or active auxiliary elements, which increases the circuit complexity, size, and cost. In addition, the auxiliary switch or diodes are hard-switched, which contributes to switching losses.

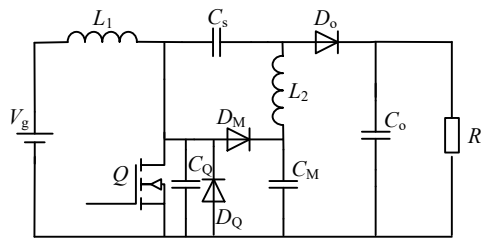


Fig.7. The proposed modified SEPIC circuit [31].

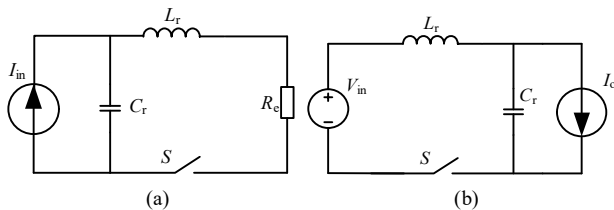


Fig.8. Resonant cell proposed in [36] (a) ICF cell (b) OCS cell.

Fig.9 provides power level and switching frequency comparison of different converters. Table I highlights the strengths and weaknesses of each soft switching technique aforementioned. Table II compares some HF converters which works in 1MHz, the output power ranges from dozens to thousands watt. According to Fig.9 and Table 2, in general, the resonant converters represented by LLC are more suitable for

high power applications and the power density is up to hundreds of W/in^3 , by contrast, the quasi-resonant converters are always used in low power applications. In the actual circumstance, the choice of topology should take application, cost, voltage and current stress and other factors into consideration.

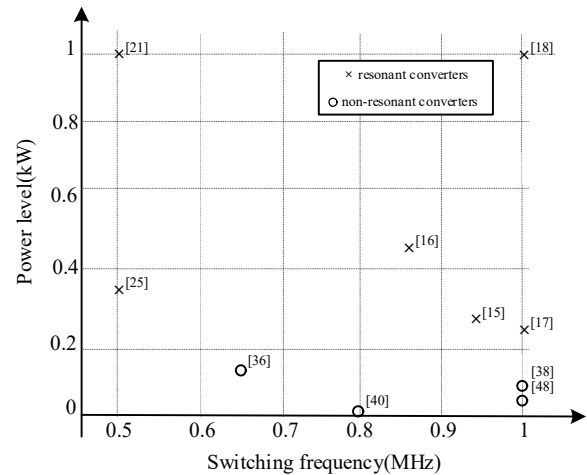


Fig.9. Power level collected from the literature review.

Table 1. Comparison of Different Soft-switching Techniques

Topology	Benefits	Drawbacks
Resonant converters	Soft switching condition for all power devices Low di/dt or dv/dt Symmetrical and continuous operation of transformer	Complex control Significant circulating power
Quasi-resonant converters	Few components No oversizing of power devices	Complex control Soft switching lost at light load
Active-clamp converters	Leakage inductance energy recycled Duty cycle higher than 0.5	Higher voltage across the switch
ZVT converters	Soft switching condition in every switching cycle	Large number of auxiliary elements Additional switching losses

Table 2. Comparison of Different High Frequency Converters

Topology	f_s	Input voltage	Output voltage	Output power	Isolation	Device type	Power density	Efficiency	Switch state		Diode state
									Turn on	Turn off	
LLC [49]	1MHz	400V	48V	3000W	Yes	GaN	$600W/in^3$	97.7%	ZVS	Hard	ZCS
LLC [50]	1MHz	380V	12V	800W	Yes	GaN	$900W/in^3$	97.6%	ZVS	Hard	ZCS
series resonant converter [51]	1MHz	17-43V	340-430V	250W	No	GaN	$14.1W/in^3$	95.5%	ZVS	ZCS	Hard
quasi switched-capacitor [52]	500kHz	400V	48V	400W	Yes	GaN	$21W/in^3$	94.8%	ZVS	Hard	Hard
quasi-resonant flyback [53]	1MHz	80V	12V	36W	Yes	GaN	$15.8W/in^3$	90.4%	valley	ZCS	N.A.
quasi modified SEPIC [54]	1MHz	24V	200V	80W	No	GaN	$69.7W/in^3$	93.1%	ZVS	Hard	Hard

III. RESONANT GATE DRIVER

A. Conventional Gate Driver

In practical applications, MOSFETs are not ideal devices and have some parasitic parameters, as shown in Fig.10. The parasitic parameters in the figure are: gate parasitic inductance L_g , drain parasitic inductor L_d , source parasitic inductor L_s , gate resistor R_g , gate source capacitor C_{gs} , gate drain capacitor C_{gd} and drain source capacitor C_{ds} . These parasitic parameters have

different effects on the switching process of Q . For example, L_g will cause the oscillation of drive signal. In general, due to negative feedback effect, the larger L_s is, the switching speed will be slower and it has a major influence on the switching energy [55]; the larger L_d is, the drain-source voltage oscillation will be more severe. The capacitors of switch are related to the switching loss.

Fig.11 shows the conventional voltage source driver (VSD) circuit, in which the resistor R_g represents the parasitic resistor and the gate resistor of drive circuit. Since the parasitic inductor

and the input capacitance may cause severe oscillation, a resistor is usually connected in series in order to damp the oscillation within an acceptable range. Capacitor C_i represents the equivalent input capacitor of the MOSFET, which is non-linear due to the Miller effect.

In the conventional VSD circuits, the driving loss accounts for the largest portion of the total losses. In addition, there are some losses associated with auxiliary switches, such as the driving loss and switching loss of the auxiliary switches, and the loss of output capacitors. The calculation of these losses is analyzed as follow.

The energy provided by the driving voltage source V_{DD} is expressed as:

$$P_{gate_Q} = V_{DD} f_s \int_0^{T_s} i_g(t) dt \quad (1)$$

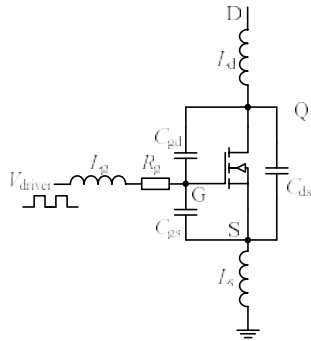


Fig. 10. Simplified model of MOSFET.

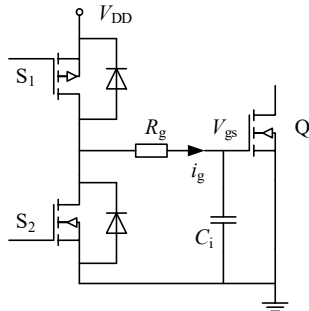


Fig.11. The conventional gate drive circuit.

Where T_s is the switching period, f_s is the switching frequency, and $i_g(t)$ is the instantaneous current flowing out of V_{DD} .

$i_g(t)$ provides total gate charge Q_g when the input capacitor voltage of MOSFET is charged from 0 to V_{DD} . The relationship between $i_g(t)$ and Q_g is:

$$\int_0^{T_s} i_g(t) dt = Q_g \quad (2)$$

Substituting equation (2) into equation (1), we can get the gate driving loss:

$$P_{gate_Q} = Q_g V_{DD} f_s = C_i V_{DD}^2 f_s \quad (3)$$

Here C_i is the equivalent input capacitance of MOSFET and Q_g is the total charge required to drive switch on.

As the switching frequency increases, the loss of auxiliary switches S_1 and S_2 also account for a certain proportion. Assuming the parameters of S_1 and S_2 are the same, the losses of each part related to S_1 and S_2 are introduced as follows.

Driving loss P_{gate_S} of auxiliary switches can be calculated through the following equation:

$$P_{gate_S} = Q_{g_S} V_{gs_S} f_s \quad (4)$$

Where Q_{g_S} is the total gate charge required to drive S_1 or S_2 , V_{gs_S} is the driving voltage.

Switching loss P_{gate_S} of S_1 and S_2 consists two parts: the hard turn-on loss and the loss generated by the output capacitor $P_{C_{oss_S}}$. According to the former analysis, the hard turn-on loss of S_1 or S_2 can be obtained.

$$P_{sw_on} = \frac{1}{2} V_{DD} I_{D_S} t_{on_S} f_s \quad (5)$$

Where I_{D_S} is the current through S_1 and S_2 , t_{on_S} is the turn-on duration, which can be obtained from the datasheet.

When the S_1 and S_2 are turned on, the charge stored in the output capacitor has a discharge path, and the loss generated by this process is:

$$P_{C_{oss_S}} = \frac{1}{2} C_{C_{oss_S}} V_{DD}^2 f_s \quad (6)$$

Therefore, the switching losses of the auxiliary switches can be expressed as:

$$P_{sw_S} = \frac{1}{2} V_{DD} I_{D_S} t_{on_S} f_s + \frac{1}{2} C_{C_{oss_S}} V_{DD}^2 f_s \quad (7)$$

Thus, the total driving loss of a conventional VSD circuit can be expressed as:

$$P_{drive} = P_{gate_Q} + P_{gate_S} + P_{sw_S} \quad (8)$$

With the increase of switching frequency, the loss of the VSD circuit increases proportionally, which seriously affects the efficiency of the power converter, hinders the development of HF, miniaturization, high power density, high efficiency and high performance of the power converter. Moreover, the anti-interference ability of the conventional VSD circuit is weak, and it is easy to cause power switches misconducted.

B. Voltage Source Resonant Gate Driver

In order to solve the above problem, resonant gate drive (RGD) circuits have been proposed to provide a better performance in HF applications [56-61].

The simplest RGD is shown in Fig.12, by adding a resonant inductor L , the energy stored in C is transferred to L to recover the energy [62]. The switching speed can also be improved as well as reduce driving loss and switching loss. However, this kind of structure has some intrinsic drawbacks. For example, as L_r and C_g are in series with V_{cc} during the charging process, L_r is charged first and the energy supplied by V_{cc} is larger than VSD. Though this part of energy can be recovered back, it still causes additional conduction losses. Besides, the four switches in the circuit need to be switch several times during one single switching cycle, which makes the control scheme more complicated. Moreover, the gate voltage changes within 0 and V_{cc} , which is not suit for switches that require reverse bias gate voltage.

The other two common RGD structures are H-bridge and half bridge structures, as shown in Fig.13 and Fig.14 [63-64]. Compared to the H-bridge circuit, the half-bridge circuit needs two more diodes, but it is difficult to control the MOSFETs precisely at the end of every resonant period for the H-bridge circuit because of the Miller effect. In this respect, the half-bridge circuit shows better performance as the diodes can block the reverse resonant current at the end of each resonant period, allowing a much simpler timing control. As the figure shows,

the half-bridge circuit uses a small value resistor to clamp the driven switch gate instead of an inductor in the H bridge circuit, which can suppress the gate voltage noise caused by rapid change in the drain-to-source voltage, but this will cause additional loss.

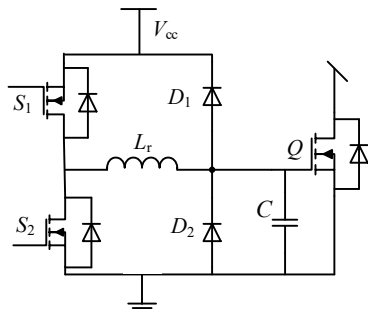


Fig. 12. The conventional resonant gate drive circuit.

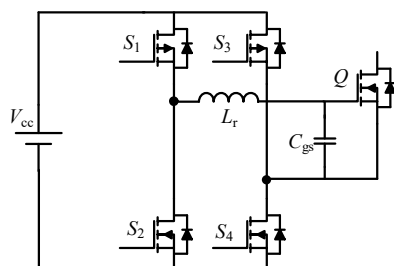


Fig. 13. The H-bridge resonant gate drive circuit [63].

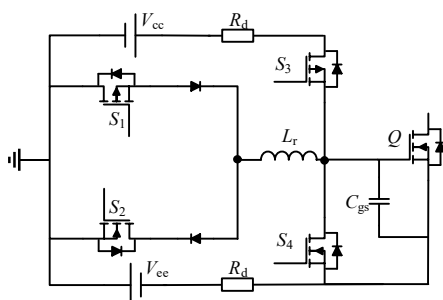


Fig. 14. The half bridge resonant gate drive circuit [64].

RGDs emphasize reduction of gate loss, but they can hardly reduce the switching loss; therefore, the potentials of using RGDs for efficiency improvement are limited.

C. Current Source Resonant Gate Driver

Current source driver (CSD) is a kind of drive circuit which generates the constant drive current to charge and discharge the power MOSFET gate capacitance [65]. Because of the CS inductor, the energy stored in the gate capacitance of the MOSFETs can be also recovered. Besides, it can also reduce the switching losses in hard switching converters with fast switching speed, with better performance than RGD in this aspect.

Depending on the current types of the CS inductor, the CSD topologies can be categorized as continuous and discontinuous. A continuous current dual channel CSD for a Buck converter with the advantages of switching loss reduction and SR gate energy recovery was proposed in [66-68]. However, the change of duty cycle and the switching frequency will cause the change of gate-drive currents, and furthermore, the inductance is relatively high (typically, 1 μ H at the switching frequency of 1 MHz). In addition, the switching frequency variation will impact on the inductance value of the continuous CSDs. In recent years, with the application of continuous CSD in Boost PFC converters, the adaptive continuous CSD was proposed [69-70]. As for the CSD, higher drive current leads to faster switching speed and reduced switching loss, but it also increases the drive circuit loss. The “adaptive” concept is to obtain the optimal trade-off between switching loss and drive circuit loss dynamically. However, the aforementioned continuous adaptive CSD has the following drawbacks: switching frequency, drive voltage and duty cycle will affect the drive current; therefore, the continuous CSD is not suitable to variable frequency applications and design and control of the circuit is complicated. The turn-ON and turn-OFF drive current must be the same, which reduces effectiveness of efficiency improvement over a wide range. Moreover, CS inductor current is continuous that results in high circulating loss in such drive circuits.

In order to reduce circulating loss as well as CS inductance value, the discontinuous CSDs with lower inductance were proposed in [71-73]. The CSD’s switches are controlled to generate discontinuous inductor current enabling the peak portion of the inductor current to be used to charge/discharge power MOSFET’s gate as a current source. Paper [74] proposed a CSD with blocking diode to overcome the current diversion problem, which also improved switching speed. However, the drive current is constant and this may lead to lower efficiency when the switching current varies in a wide range such as for PFC applications. Therefore, adaptive discontinuous CSD was proposed with the advantages of reduced circulating loss, independent turn-on and turn-off current [75]. Besides, the adaptive drive current is independent of the duty cycle and switching frequency, and thereby it can be applied to variable frequency applications. Fig. 15 shows switching signals of RGD, continuous CSD and discontinuous CSD respectively. In the above three gate drivers, the inductor current is obviously different. The driving speed of continuous CSD and discontinuous CSD is faster than RGD, and the loss of discontinuous CSD is less than continuous CSD.

Table III shows comparison of various resonant gate drivers aforementioned. According to the table, it can be seen that the turn-on/turn-off time of VSD is long because of zero initial charging current. The inductance and loss of continuous CSD are larger than discontinuous CSD.

Table 3. Comparison of Different Resonant Gate Driver

Topology	Switching frequency	L_r	Turn on/off time	Loss
Voltage source resonant gate driver[62]	500kHz	470nH	170ns/-	0.134W
Continuous current source driver[66]	1MHz	1 μ H	12ns/13ns	0.327W
Discontinuous current source driver [71]	1MHz	280nH	15ns/15ns	0.202W

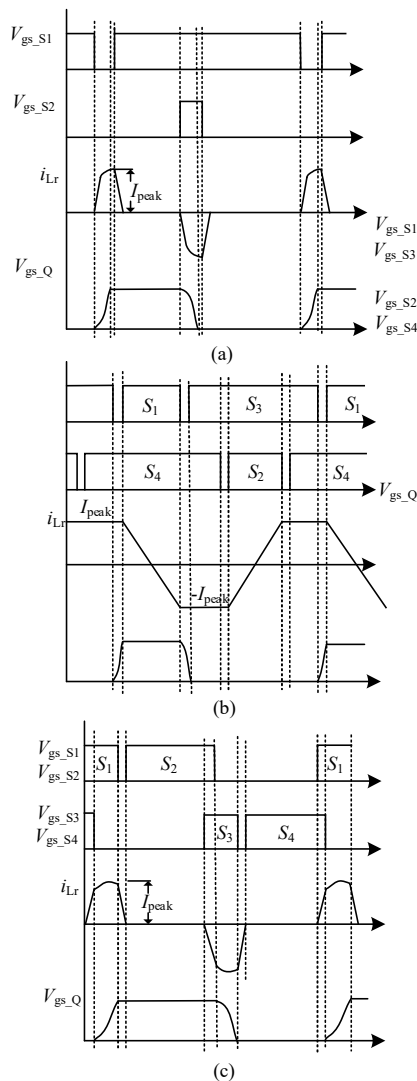


Fig. 15. Switching signals of different gate drives.

IV. HIGH FREQUENCY MAGNETIC COMPONENTS

One major advantage of HF is that the volume of passive components reduces significantly with the increase of switching frequency, which greatly reduces the volume and cost of the converter. However, the losses of traditional winding magnetic components increase dramatically with the increase of switching frequency. By contrast, planar magnetic components show great superiority in HF applications with the advantages of low profile and large heat dissipation area, besides significant improvements in performance are possible through operation at HF using commercially available magnetic materials. In addition to the core shape, magnetic materials should also be considered under HF applications. Generally speaking, as the loss of magnetic components will increase with the increase of switching frequency and magnetic flux density, the low electrical conductivities and low permeability are helpful to reduce loss. At present, companies such as FERROXCUBE, HITACHI, TOKIN have materials suitable for MHz level. Fig.16 shows core loss measurement results of different materials under 1-MHz excitation [76].

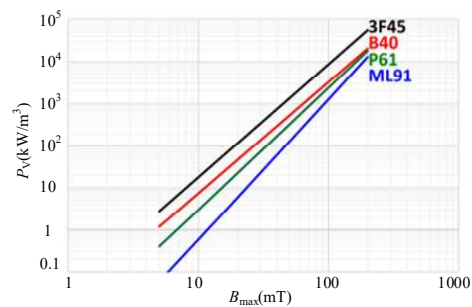


Fig. 16. Core loss measurement results of different materials under 1-MHz excitation.

A. Design Process

The basic design methodology of planar magnetic components was proposed in paper [77], however, many coupled factors such as copper track structures and winding layouts will greatly affect the properties of inductors and transformers in fact. Besides, with the increase of switching frequency, the skin and proximity effects become more severe, and the self and mutual impedances make modeling more challenging, especially when parallel windings are included. Finite-element modeling (FEM) and experimental measurements are widely used in magnetic components design, but these two methods are not analytical and time consuming [78-79]. Therefore, some effective ways are proposed to help the planar magnetics design.

Dowell's results have been the main references for transformer conduction-loss calculations [80]. But the accuracy cannot be guaranteed in practical planar transformer design due to certain restrictions. In [81], winding loss expressions for the n 'th layer in cylindrical coordinates is proposed, therefore specific radial thickness for each layer can be determined to minimize power dissipation. A new formula for the optimum foil or layer thickness is introduced in [82], this method does not need for Fourier coefficients and calculations at harmonic frequencies. A squared-field-derivative method calculating eddy-current losses for transformer and inductor windings is proposed in [83], considering 2-D and 3-D field effects. However, these approaches rely on various assumptions, and sometimes are not easy to use.

Modular layer model (MLM) is a systematic approach to modeling impedances and current distribution in planar magnetics [84]. This model only rely on two assumptions. The model captures skin and proximity effects, and enables accurate predictions of impedances, losses, stored reactive energy, and current sharing among windings. The basic idea of MLM is describing the different layers of planar magnetic elements with the same equation, as shown in equation (9).

$$\begin{cases} d_i E_{Ti} = w_i H_{Ti} \frac{d_i \Psi_i (1 - e^{-\Psi_i/h_i})}{w_i \sigma_i (1 + e^{-\Psi_i/h_i})} + w_i K_i \frac{d_i}{w_i \sigma_i} \frac{2\Psi_i e^{-\Psi_i/h_i}}{(1 - e^{-2\Psi_i/h_i})} \\ d_i E_{Bi} = w_i K_i \frac{d_i}{w_i \sigma_i} \frac{2\Psi_i e^{-\Psi_i/h_i}}{(1 - e^{-2\Psi_i/h_i})} - w_i H_{Bi} \frac{d_i \Psi_i (1 - e^{-\Psi_i/h_i})}{w_i \sigma_i (1 + e^{-\Psi_i/h_i})} \\ H_{Ti} - H_{Bi} = K_i \\ w_i K_i = I_i m_i \end{cases} \quad (9)$$

Here, I_i and K_i represent the current and the current per width. m_i denotes the number of turns. E_{Ti} and E_{Bi} denote the electric field strength on top and bottom surface of the i th layer, H_{Ti} and H_{Bi} are the magnetic field strength, and d_i , h_i , and w_i represent the length, thickness, and width of one turn. ω is the angular frequency, μ_i is the permeability, and σ_i is the electric conductivity.

Each layer can be abstracted into a three-port impedance network, as Fig.17 shows.

$$Z_{ai} = \left(\Psi_i (1 - e^{-\Psi_i h_i}) \right) / \left(\sigma_i (1 + e^{-\Psi_i h_i}) \right)$$

$$Z_{bi} = 2 \Psi_i e^{-\Psi_i h_i} / \left(\sigma_i (1 - e^{-2\Psi_i h_i}) \right).$$

Based on the above analysis, the relationship between the two adjacent layers i and j can be calculated, and impedance network of the magnetic components can finally be established. This method has been proved in [83] by comparing with FEM results.

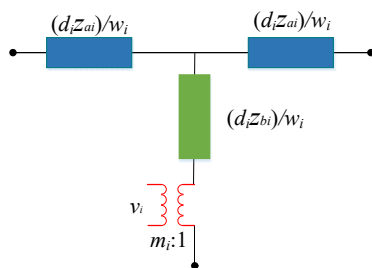


Fig. 17. Three-terminal model of single conductor layer.

B. Method of Reducing Parasitic Parameters

Though there are many advantages of planar magnetic components, the parasitic parameters are inevitable. For better performance of the converter, leakage inductance, AC capacitance and AC resistance should be carefully considered.

Since there is a small part of magnetic flux generated by ac current excitation on the primary side that cannot link with the secondary winding, the leakage inductance always exists. The leakage inductance will cause voltage spikes on the main switches for hard-switching converters, which increases the switching losses and thus reduces the power efficiency, besides creates severe EMI problems. In order to reduce the leakage inductance, interleaving windings is a general method.

Take a four-layer transformer for example, the **turn ratio** is 1:1, and the primary and secondary winding are designed two layers, each layer contains one turns for convenience. The primary and secondary winding are designed to be same. The analytical scheme of **magnetic motive force (MMF)** distribution of the interleaving structure and non-interleaving structure are shown in Fig.18. As shown in the figure, h_1 , h_2 and h_Δ represent the thickness of the primary winding, secondary winding and insulator respectively. According to the analytical MMF distribution, the total energy associated with the leakage inductance can be calculated by the following equation:

$$E_{lk} = \frac{\mu_0}{2} \sum_0^h \int_0^h H^2 \cdot l_w \cdot w \cdot dx \quad (10)$$

Here, l_w is the average turn length, μ_0 stands for the vacuum permeability. Apparently, the interleaving structure provides a significant advantage in reducing leakage inductance.

As for the interleaving structure, the total energy can be expressed by the following equation.

$$E_{lk} = \mu_0 \cdot \frac{l_w}{w} \cdot 2 \left[\frac{h_1 + h_2}{3} + h_\Delta \right] \quad (11)$$

In some specific situations such as LLC, a larger leakage inductance is need. There are two additional methods to increase the leakage inductance, one is to add a magnetic shunt, the other is to adopt fractional turn [85]. As for the first method, in order to provide a relatively lower reluctance return path for the magnetic flux, usually ferrite polymer composites (FPC) material is inserted between the primary and secondary windings. Therefore, returned magnetic flux does not link to the other windings, and a high leakage and low coupling coefficient are obtained. The inserted FPC material is proved to be effective according to FEA simulation results that it leads to a four times higher leakage inductance increment than the case without the FPC. The amplitude of leakage inductance can be controlled by the thickness and the permeability of the inserted magnetic shunts. However, a higher permeability or a thicker magnetic shunt increases the leakage inductance, it will also cause the increase of eddy current effect, which decreases the system efficiency.

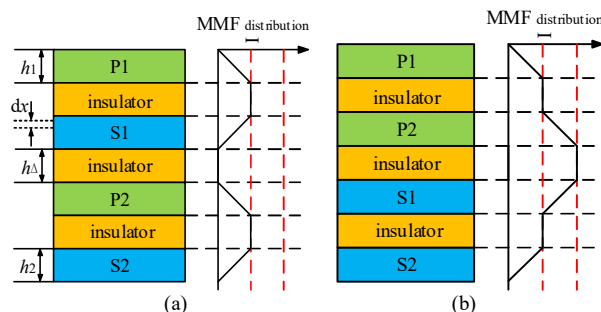


Fig.18. Analytical scheme of MMF distribution of the transformer. (a) interleaving structure. (b) non-interleaving structure.

Fig.19 shows the examples of fractional turns. As can be seen from the figure, in the EI core, the primary winding is placed in the middle leg and the secondary winding is placed in the outer leg. Because of the particular structure, this type of core splits the magnetic flux into two equal portions, and only one portion is linked with the secondary winding, thus high leakage inductance is obtained. The leakage inductance is determined by the ratio of the reluctance of the core leg.

Though the interleaving structure can reduce the leakage inductance, it will increase of the parasitic capacitance at the same time. There is a tradeoff between leakage inductance and parasitic capacitances. These capacitances exist between turns, winding layers, and between windings and core, which will significantly affect the magnetic component performance. For example, the interwinding capacitance always causes leakage currents and aggravates **electro-magnetic interference (EMI)** problem. Paper [86] points out four methods to reduce parasitic capacitance: 1) increase the distance between windings and reduce the surface area of overlapping as possible; 2) reduce the number of turns per layer and increase the number of layers within cost range; 3) minimize the number of intersections

between the primary and the secondary winding when design the structure; 4) arrange winding connection reasonably to obtain minimum energy related to electric field. Paper [87] proposed a new interleaved structure, with this optimized method, smaller leakage inductance and parasitic capacitance can be obtained simultaneously, the structure is shown in the Fig.20. As the figure shows, the primary and secondary windings adopt interleaved structure, but different from the traditional structure, all the turns of secondary winding are in a single layer, while the other layer is only used for the outgoing line. This method is proved to be effective according to the simulation and calculation results.

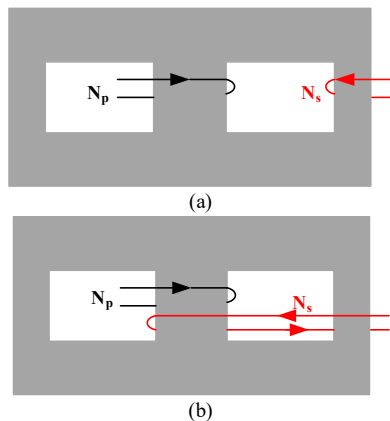


Fig.19. Examples of fractional turns.

Similar to the leakage inductance, the parasitic capacitance is expected to be enhanced in some certain applications such as integrated LLC transformers and EMI filters [88-89]. Depending on the different requirements for capacitance, dielectric material with high or low dielectric permittivity is placed between two planar layers of windings, thus a capacitor is formed. This kind of capacitor can be used to replace resonant capacitors, filters, decoupling and snubber capacitors, and are already commercially available.

In addition, parasitic resistance is a crucial parameter which directly influences the characteristics and efficiency of power converters. With the switching frequency increase, the skin and proximity effects become more severe. Both the skin effect and the proximity effect cause the current density to be nonuniform in the cross section of the conductor; thus, causing a high winding resistance at HF. The DC resistance is easy to be obtained, while the AC resistance is a function of DC resistance. The most commonly used expression for the AC resistance of the m th layer is expressed by equation (12).

$$\frac{R_{ac}}{R_{dc}} = \frac{\xi}{2} \left[\frac{\sinh \xi + \sin \xi}{\cosh \xi - \cos \xi} + (2m-1)^2 \cdot \frac{\sinh \xi - \sin \xi}{\cosh \xi + \cos \xi} \right] \quad (12)$$

Here, $\xi = h/\delta$, δ is the skin depth of the copper, h is the winding thickness. $m = F(h)/(F(h) - F(0))$, $F(h)$ and $F(0)$ are the MMFs at the limits of a layer.

In paper [90], a nonuniform width winding structure is adopted to reduce DC winding resistance, and the winding structure is shown in the Fig.21. The main idea of this winding structure is to achieve a constant track resistance for each turn,

thus the widths of turn geometrically change from inner turn to outer turn. In this structure, the most important factor is the radius ratio of adjacent windings. The minimum DC resistance is determined by the radius ratio and the number of turns per layer simultaneously.

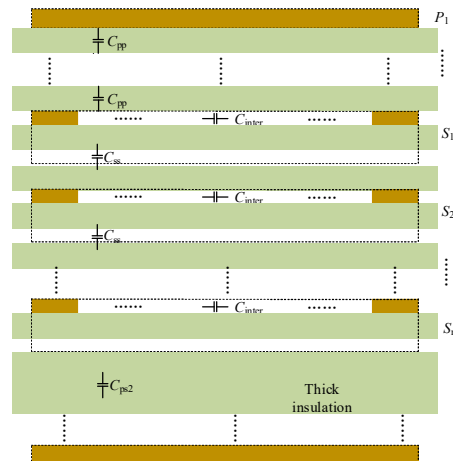


Fig.20. A new interleaved structure proposed in [87].

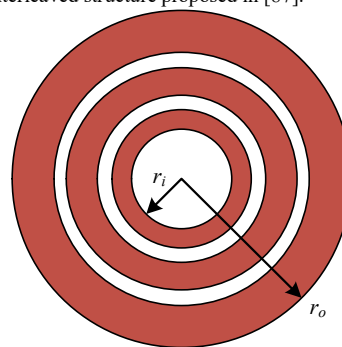


Fig.21. Diagram of the idea variable width spiral winding structure [90].

V. FUTURE RESEARCH HOTSPOTS AND CHALLENGES OF HIGH FREQUENCY

A. Control Method

The increment of switching frequency also proposes a new challenge to traditional control methods, since the digital controller is implemented using a limited clock speed to generate the PWM signals. Moreover, the limited frequency resolution can lead to performance degradation at high switching frequencies because a large switching frequency variation can be induced by a single frequency step in the digital signal processor (DSP). Therefore, it is necessary to explore the control strategy suitable for specific converter in HF applications. For example, paper [91] proposed a PWM and pulse frequency modulation (PFM) Hybrid Control Method for a 1MHz LLC converter, the proposed hybrid algorithm shows not only enhanced output voltage regulation, but also lower current spikes in the primary and secondary sides compared with traditional PFM method.

B. Matrix Transformer

With the rapid increase of cloud computing and the high demand for digital content, low-voltage and high-current LLC

converters are greatly needed. But the design of such LLC converter is very challenging because of high output current, SRs need to be paralld and SRs current sharing and large termination losses of the transformer should be carefully considered. Matrix transformers show outstanding performance in such occasions to reduce the total transformer losses by splitting the current among various elements. It breaks a single transformer into various elemental arrays inter-wired to form a single transformer, and the turn ratio of each individual transformer is thus reduced. It is especially helpful for PCB winding-based transformers. The LLC converter with a matrix transformer is shown in the Fig.22.

The optimum design of matrix transformer is mainly on structure. The number of matrix transformers is not the more the better. The core loss increases with the number of matrix transformers. Based on the consideration of efficiency optimization, the optimal number of matrix transformer needs to be selected according to the actual situation. Paper [92-94] proposed several new structures of matrix transformers to integrate several matrix transformers into one core and arranged the windings reasonably to further reduce core loss. **At the same time, the conventional winding loss model is not applicable to the matrix transformer, an accurately winding dc resistance model and an analytic winding ac resistance model suit for matrix transformer are proposed in [95].**

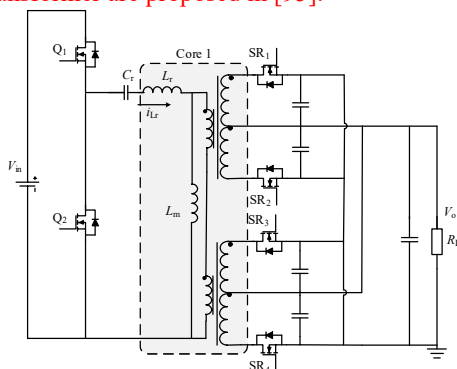


Fig.22. LLC converter with a matrix transformer.

C. Gate Drivers for SiC and GaN

Although resonant gate drive technology has been relatively mature, combined with WBG devices, gate-driver circuit should be designed to optimize the switching performance.

In terms of device characteristics, the transconductance of SiC-MOSFET is lower than Si-MOSFET. Therefore a higher V_{gs} is required to achieve the lowest V_{ds} saturation voltage. The typically V_{gs} is 15V to 20V of SiC-MOSFETs compared with 8V to 10V of Si-MOSFET. On the other hand, the fast switching speed and low turn-on threshold of SiC-MOSFET requires a negative V_{gs} level during turn-off. In general, -2V to -5V drive is recommended for SiC devices. As for GaN MOSFETs, the gate voltage cannot exceed the maximum rating of 6V, and high reverse conduction loss caused by the absence of body diode should also be considered. A resonant gate driver for GaN is proposed in [96] with the output of +6/-3.5V. But the turn on process is interfered by the current and parasitic inductance hence the voltage waveform becomes oscillatory. Paper [97] proposed a three-level gate driver for GaN to reduce reverse

conduction loss, but does not have resonant characteristic. At present, the application of the resonant gate driver in the SiC or GaN-based converter is not widely researched. This is the main research direction in the several decades.

Fig. 23 summarizes the existing technologies and future trends in terms of HF converter topology, HF resonant driver and planar magnetics which are analyzed in this paper. **HF technology includes not only HF converter topology, but also HF driving strategy and magnetic component design. In terms of HF converter topology, topology research has been relative mature, researchers are now more concerned with how to improve performance, in terms of control strategy, cost and reliability. HF driving strategy needs to be combined with WBG devices. Magnetic component design main focuses on parasitic parameters control and utilization.**

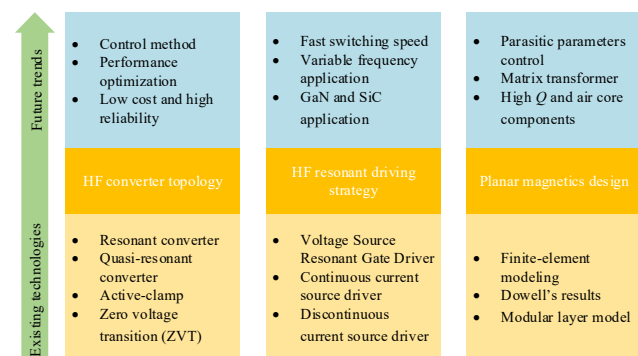


Fig.23. Existing technologies and future trends.

VI. CONCLUSION

Over the past several years, with the fast development of electronic power conversion technology, the feature of high power density is extremely expected in many fields. To achieve the aforementioned goal, the most effective way is to improve the switching frequency, therefore, HF converters are widely studied these years. The commercialization of WBG devices has also promoted the further development of HF converters. Meanwhile, the HF also brings many new challenges, such as the increasing switching loss and magnetic loss.

To obtain better performance, this paper analyzes HF converters from topology, drive circuit and magnetic components three aspects. The topologies are classified into resonant and non-resonant converters. Besides, RGD and CSD are compared with the traditional drive circuit to show their superiority in HF applications. The modeling and optimization of planar magnetic components are also discussed in detail. At last, the hot topics in HF converters in the near decades are stated in general.

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