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A Review of the Pinned Photodiode for CCD and CMOS Image Sensors

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***Abstract*—The pinned photodiode is the primary photodetector structure used in most CCD and CMOS image sensors. This paper reviews the development, physics, and technology of the pinned photodiode.**

***Index Terms*—Charge-coupled device (CCD), CMOS active pixel image sensor (CIS), photodetector, pinned photodiode (PPD), pixel.**

I. Introduction

THE "pinned photodiode" is a photodetector structure used in almost all charge-coupled device (CCD) and CMOS image sensors (CIS) due to its low noise, high quantum efficiency and low dark current. We found that a comprehensive review paper on this device structure was needed in the literature. In this paper we will review the history of the pinned photodiode development, discuss the physics of its operation, briefly discuss its fabrication, and review its application.

II. Historical development

A. Early Pixel Devices

The photosensitive nature of certain materials has been known for over one hundred seventy years [1] and semiconductor photoconductors and photodiodes have been studied and used continuously for well over one hundred years [2]. We start our discussion with the emergence of integrating photodetector arrays used as image sensors. The integrating *pn* junction photodetector was first introduced by Weckler at Fairchild in 1965 [3], [4]. He noted that if a *pn* junction in an integrated circuit was initially reverse biased and then one terminal left floating (e.g. the $p+$ region of a diffused $p+n$ junction), the photocurrent caused the voltage of the photodiode V to discharge according to its capacitance C and the photocurrent I_{ph} flowing into the floating node. The rate of discharge is given by:

$$\frac{dV}{dt} = \frac{I_{ph}}{C(V)} \tag{1}$$

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The photocurrent depends on the wavelength-dependent photon flux $\phi(\lambda)$ incident on the semiconductor and the wavelength-dependent quantum efficiency $\eta(\lambda)$ which accounts for optical reflection, absorption and carrier collection:

$$I_{ph} = q \int_{\lambda} \phi(\lambda) . \eta(\lambda) \, d\lambda \tag{2}$$

The integrating photodiode was the basis for the earliest MOS passive pixel sensors (PPS) [5].

In 1968, Nobel at Plessey proposed a buried photodiode-structure for MOS PPS to reduce dark current (the collected signal in the dark due to thermal generation and diffusion) and to improve the packing density of pixels [6]. (A more modern-looking buried photodiode was proposed by Koike at Hitachi in 1977 to increase photodiode capacitance in MOS PPS [7].)

The CCD was invented in 1969 at Bell Labs by Boyle and Smith [8] and its application to image sensors was immediately apparent and first reported by Tompsett, Amelio and Smith in 1970 [9]. Early CCD devices used a deep-depleted MOS structure as the photodetector and suffered from large dark current from unsuppressed Si-SiO_2 interface traps, among other defect-related traps. The buried-channel CCD was introduced by Bell Labs to avoid the impact of interface traps [10] especially on charge transfer efficiency.

The early CCDs used a full-frame architecture, meaning that the CCD cell serves both as the photodetector (while the CCD clocking signals are "frozen" during signal integration) and as a charge-transfer device through which signals from other pixels pass while the clocking signals are active, and where a pixel is the unit cell of the image sensor. In full-frame CCDs, the potential wells in each pixel are fully depleted at the start of each integration period (no signal carriers). At the output amplifier, correlated double sampling (CDS) [11] is used to suppress reset kTC noise on the floating diffusion so the signal, even under low light, is photon-shot-noise limited. A mechanical shutter is needed for this device to avoid "smearing" the image during readout due to inadvertent photosignal generation.

The interline transfer (ILT) CCD device was proposed by Walsh and Dyck at Fairchild to reduce smear and eliminate a mechanical shutter [12]. The ILT-CCD used a $n+p$ junction photodetector and a separate charge-transfer device in the pixel. At the end of photosignal integration, the signal charge was transferred to the CCD vertical shift register. The shift register ran contiguously and vertically through the pixels and was used for readout while the next photosignal was

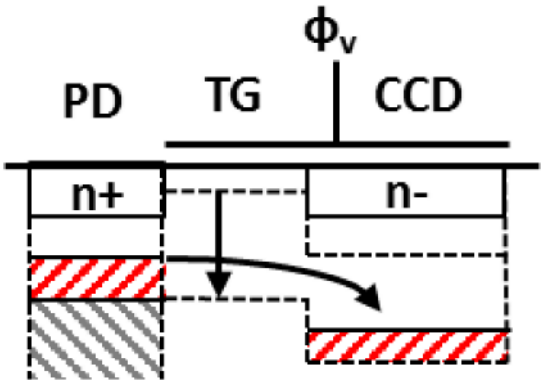

Fig. 1. Signal charge transfer from ILT CCD n + p photodetector.

integrated in the photodetector. The shift register part of the pixel was covered with a metal (or silicide) light shield to eliminate smear. The ILT CCD architecture was more suitable for consumer video application due to reduced smear and more compact chip design than the full-frame CCD. The rapid growth of the consumer electronics video camera market accelerated the improvement of ILT CCD image quality and many advancements were reported in the later 1970's and early 1980's. To further reduce smear from bright light sources, a frame-interline-transfer (FIT) CCD architecture was subsequently developed by Horii, Kuroda and Kunii at Matsushita in 1981 [13] but the pixel structure was essentially identical to that of the ILT CCD.

In the ILT's $n+p$ photodetector, the $n+$ region can be considered to have a nearly infinite number of electrons. To read out signal charge, a transfer gate is used to create a variable potential barrier for carriers in the $n+$ junction as illustrated with the potential-well diagram in Fig. 1. When the transfer gate is "on" (usually meaning a positive bias relative to substrate for an n-channel device) electrons in the $n+$ region transfer across the barrier until the potential in the $n+$ region is approximately equal to the potential barrier. In the process of reading out the signal carriers, the $n+$ region is essentially reset to a higher potential. The transfer gate is then turned "off" to a lower potential. New photoelectrons are collected in the $n+$ photodetector during the integration period with an associated drop in $n+$ region potential. At the end of the integration period, the transfer gate is again pulsed "on" to skim off the collected signal carriers.

While this approach to ILT devices was used for a number of years, it had several performance limitations. First, the reset level of the photodetector is subject to "kTC" noise due to thermionic emission across the TG potential barrier. This noise dominates low light imaging performance and cannot be suppressed by subsequent signal processing.

Second, if a brightly illuminated pixel is then dimly illuminated, carriers from the brightly illuminated integration period may continue to transfer out of the $n+$ region in subsequent frames. This "lag" gives rise to the well-known "comet tail" in CCD video cameras (as well as in older tube cameras). The lag is related to subthreshold conduction in MOSFETs and can be substantial.

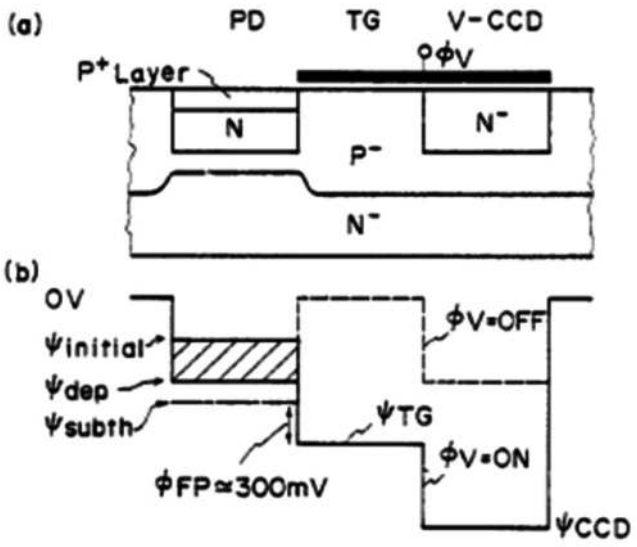

Fig. 2. Complete charge transfer from a pinned photodiode. (a) structure including VOD (b) potential well diagram (from Teranishi et al., 1982).

Third, blue light with a short absorption length in silicon may be absorbed in the $n+$ region and the photohole may recombine before separation by the $n+$ p junction and be "lost." This leads to reduced quantum efficiency in the blue part of the spectrum.

Besides the image sensor architecture, another CCD development theme was the simplification and improvement of the clocking electrodes across the image sensor. Different ways to implement "built-in" asymmetry for simplifying clocking had been investigated by many researchers in the 1970's [14]. In 1978, Hynecek at Texas Instruments filed for a patent on a "virtual-phase" full-frame CCD [15] and published a paper in 1979 [16]. In this device, one of the phases in a CCD transfer device was replaced by a "virtual phase" consisting of a shallow, heavily-doped p-type surface layer that maintained the channel under it at a fixed potential due to "valence-band pinning" [17], [18]. A second more heavily doped channel region was adjacent, providing a built-in potential step to the channel. Such a built-in "frozen" phase allowed "uniphase" operation and better manufacturing yield. The virtual-phase CCD had better low-light sensitivity compared to other full-frame CCD image sensors since it had less overlying polysilicon. Significantly reduced dark current was also reported. The virtual-phase CCD was promoted as a simpler, easier to manufacture, and higher performance alternative to other CCDs.

B. Complete Charge Transfer to Eliminate Lag

To solve the ILT lag (and kTC noise) problem, a low-lag structure was invented by Teranishi, et al. at NEC in 1980 [19] and reported in 1982 [20] as shown in Fig. 2. They recognized that lag would be eliminated if all the signal carriers could be transferred from the photodiode to the CCD. By creating a buried-diode structure with a $p+$ cap layer ($p+np$ vertical structure) the n layer could be fully depleted with application of sufficient transfer-gate voltage. Since it is a buried photodiode, dark current was also suppressed. In the

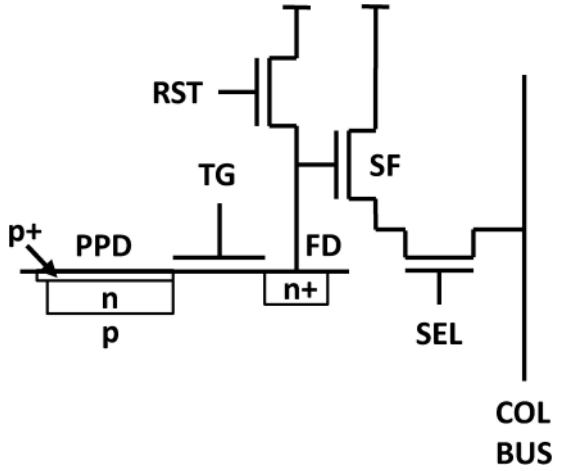

Fig. 3. Schematic of CMOS APS pixel with PPD.

1982 paper they also added a vertical anti-blooming structure (i.e. $p+npn$) or vertical overflow drain (VOD) so that when the capacity of the n storage region was filled, excess carriers would drain to the substrate rather than bloom to neighboring pixel storage areas or into the CCD readout device. Another nice feature of the device was that the $p+$cap layer was integrally tied to the other p layer like the Noble device.

In 1984, the structure received the name "pinned photodiode" (a.k.a. PPD) in a paper published by Burkey et al. at Kodak [21]. In this paper, the improved blue QE of the structure (due to the thin pinning layer) and its high charge capacity were emphasized. Starting in 1987 the PPD was incorporated into most ILT CCD architectures [22] and became a fixture in consumer electronics video cameras and, later, in digital still CCD cameras. A review of various photodetector elements for ILT CCDs was presented by Kodak in 1991 [23].

C. Other Contributions to the PPD Invention

The PPD structure, while invented for low lag ILT CCD application, shares a strong resemblance to the Hynecek virtual-phase CCD structure, with the exception of the VOD. The two inventions were solving different problems with essentially the same device structure and operating principles.

In 1975, Hagiwara at Sony filed a patent application on bipolar structures for CCDs in which a *pnp* vertical structure was disclosed, among several structures [24]. The top p layer was connected by metal to a bias used to control full-well capacity and the n-type base layer was proposed for carrier storage. In an unusual paper, Hagiwara, in 1996, revisited the 1975 invention and claimed it was essentially the invention of both the virtual phase CCD and the NEC low-lag structures, as well as the basis of the Sony so-called "Hole Accumulation Diode," or HAD structure [25]. However, the 1975 application did not address complete charge transfer, lag or anti-blooming properties found in the NEC low-lag device, and does not seem to contain the built-in potential step and charge transfer device aspects of the virtual-phase CCD. Hagiwara repeats these claims in a 2001 paper [26] and shows a VOD structure that is not found in the 1975 patent application. Sony did not seem to pursue the HAD structure until well after the NEC paper was published. However, the "narrow-gate" CCD with an open p-type surface region for improved QE also disclosed in the 1975 application was reported in more detail by Hagiwara et al. at Sony in 1978 [27]. A similar structure was used extensively by Philips [28].

The PPD, as it is most commonly used today, bears the strongest resemblance to the Teranishi et al. ILT CCD device. Thus, these days Teranishi is considered as the primary inventor of the modern PPD [29].

D. Application to CMOS Active Pixel Image Sensors

In 1993, a CMOS active pixel image sensor (APS) with intra-pixel charge transfer was proposed by Fossum et al. at JPL [30], [31]. Performance improvement using backside illumination (BSI) and a pinned photodiode was suggested in 1994 [32]. A CMOS APS pixel with a PPD is shown schematically in Fig. 3. Signal charge collected by the pixel photodetector is transferred to a floating diffusion (FD) whose potential is monitored by a source-follower (SF) within the pixel. FD is reset by transistor reset signal (RST) prior to transfer and the source-follower is connected to the column bus line (COL BUS) using a row-select transistor (SEL).

Implementing a pinned photodiode (PPD) with a CMOS APS was technically challenging since the CCD PPD required high transfer gate voltages to reduce any potential barriers and achieve complete charge transfer. Such high voltages (12-15 V) were not generally compatible with CMOS processes. Integrating the CCD PPD into a CMOS APS was first reported in 1995 from a JPL and Kodak collaboration in which Kodak developed a low voltage PPD implementation [33]. Further refinement [34–36] and widespread adoption of the PPD in CMOS image sensors occurred in the early 2000's and helped CMOS APS achieve imaging performance on par with, or exceeding, CCDs.

Since the PPD is often used in pixels with nominally four (4) transistor gates, such a CMOS APS pixel is often referred to as a "4T" pixel. (This is in contrast to a "3T" pixel which refers to CMOS active pixel sensors where the photodiode is directly connected to the in-pixel source-follower, and complete intrapixel charge transfer from the photodiode is not performed. Sometimes "partially pinned photodiodes" [37] were used in 3T CMOS APS devices.)

Shared readout refers to the connection of multiple pixel FDs to a single source-follower output and reset gate [38], [39]. In this case components of the "normal" 4T APS pixel are now spread across 2 or 4 pixels, making the average transistor count per pixel 2.5T, 1.75T, or 1.5T depending on the degree of sharing and other circuit economies. Readout circuit sharing allows either improvement in fill factor or pixel density.

Conceptually, thinning for backside illumination (BSI) originated with silicon targets for vidicon tubes [40]. Backside illumination of CCDs – that is, illuminating the device from the side opposite the "front" side with metal wiring and transistors – was first reported by Shortes et al. [41], [42] and used primarily in scientific and defense applications [see e.g., [43], [44]. Extension of this concept to CMOS image sensors was suggested early [30] and the first patent application on a BSI

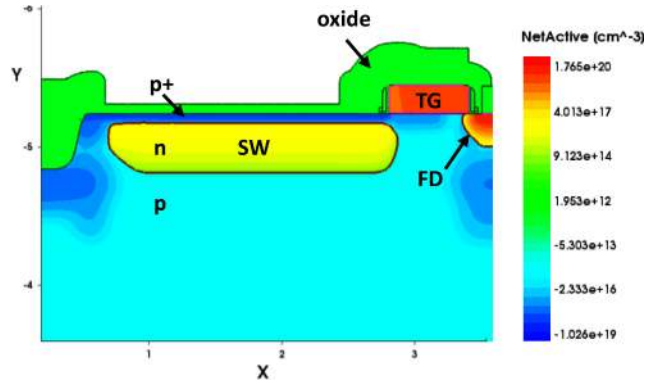

Fig. 4. Example of a pinned photodiode implemented in a CMOS image sensor showing doping concentrations. (Dimensional units are microns).

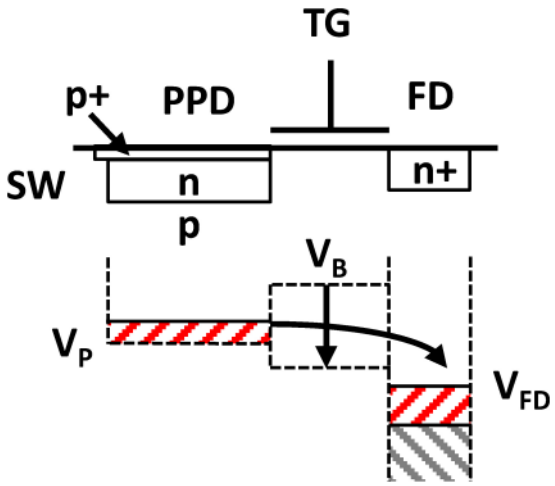

Fig. 5. Ideal potential well diagram for FSI PPD. Turning on transfer gate TG.

CMOS manufacturing method was filed in 1999 [45]. Since then, many other methods for BSI manufacturing have been proposed using both SOI and bulk processes. Mass-production of BSI PPD CMOS image sensors is now routine [46]–[48]. Color filter arrays and microlenses are also placed on the backside, and frontside metallization can serve as a reflector for boosting QE [49], [50]. Aside from an increase in fill factor with BSI, the thinned active layer combined with a thinner optical stack on the back surface permits a greater optical acceptance angle and reduced optical and carrier crosstalk for a given pixel size. Frontside metallization layout is simplified and an option for 3D stacking of electronics is emerging [51].

Combined with low power and "camera-on-a-chip" functions [5], and owing to its now-standard incorporation into mobile phones, a rapid growth in the CMOS image sensor market occurred. Today in 2013 over 2.2 billion CMOS image sensors are manufactured per year worldwide [52], corresponding to over 60 cameras per second 24/7. Between CCDs, and now CMOS image sensors, one can estimate that the pinned photodiode has already been used in about 20 quadrillion ($2x10^{16}$) pixels [53] and is one of the key elements in making image capture devices ubiquitous in modern society.

III. Structure and Device Physics

The structure and device physics of the PPD are now discussed. In this paper we are concerned with the PPD itself and signal carrier transfer from the PPD, but some discussion of the readout of the pixel is inevitable and will be made to a small degree. It is not the intent of this paper to review all possible configurations of CMOS image sensors that use PPD pixels. Also not discussed is the coupling and wavelength selection of light into the pixel using microlenses, light guides, color filter arrays and other micro-optical structures. For these topics, the reader is referred to other papers [54], [55].

A. Basic Structure

The thicknesses and lateral dimensions of doping layers in the PPD have evolved over the years due to technology and device performance improvements. The structure of a modern pinned photodiode used in CMOS image sensors is shown in Fig. 4. It can be considered as a JFET with photogate tied to substrate, as a bipolar *pnp* device with emitter tied to collector, or as a partial virtual-phase-CCD cell. The device can also be implemented in reverse polarity with some reported advantages [56]. The main elements are an *n*-type buried signal charge storage well (SW) region sandwiched between a lower *p*-type layer and a *p* + pinning layer at the top surface in contact with the lower active layer, a transfer gate (TG), and an *n* + output floating diffusion (FD). In a 180 nm process, the *p* + pinning layer might be about 100 nm thick, the *n*-layer about 2,500-5,000 nm thick, and the *p*-layer a few microns thick. The *pnp* PPD sandwich can be built using a *p* on *p* + epi substrate, or implemented by *p*-well in an *n* on *n* + epi substrate. Having an *n*-layer under the sandwich can be used for a VOD and/or improved isolation.

In the BSI PPD architecture, the entire photodetector is 2-5 um in total thickness and may be primarily *n*-type material to simplify thinning and/or carrier collection. Passivation of the backside surface is quite important [44] and not discussed in detail here, but typically a very thin, heavily doped, *p*-type layer is desired for the back surface which also must be held at fixed potential.

In normal operation, the imaging cycle starts with the PPD *n*-region fully depleted by prior charge transfer. The potential in the PPD has a maximum in the *n*-region with a value called the pinning potential, V_p as illustrated in Fig.5. Between the PPD and the FD is a minimum potential or barrier potential V_B controlled primarily by TG.

In a frontside illuminated (FSI) architecture, prevalent until the recent widespread adoption of BSI, light enters the top surface and is absorbed in the *pnp* layers in accordance with the wavelength dependent absorption coefficient. An important feature of the FSI PPD is that blue light is not blocked by polysilicon-gate layers above it, nor is it substantially absorbed in the pinning layer, and carriers generated relatively close to the surface can be collected into the SW by diffusion and drift without much recombination and signal loss. Green and red light is absorbed with good quantum efficiency and collection efficiency, though the doping may be tailored to

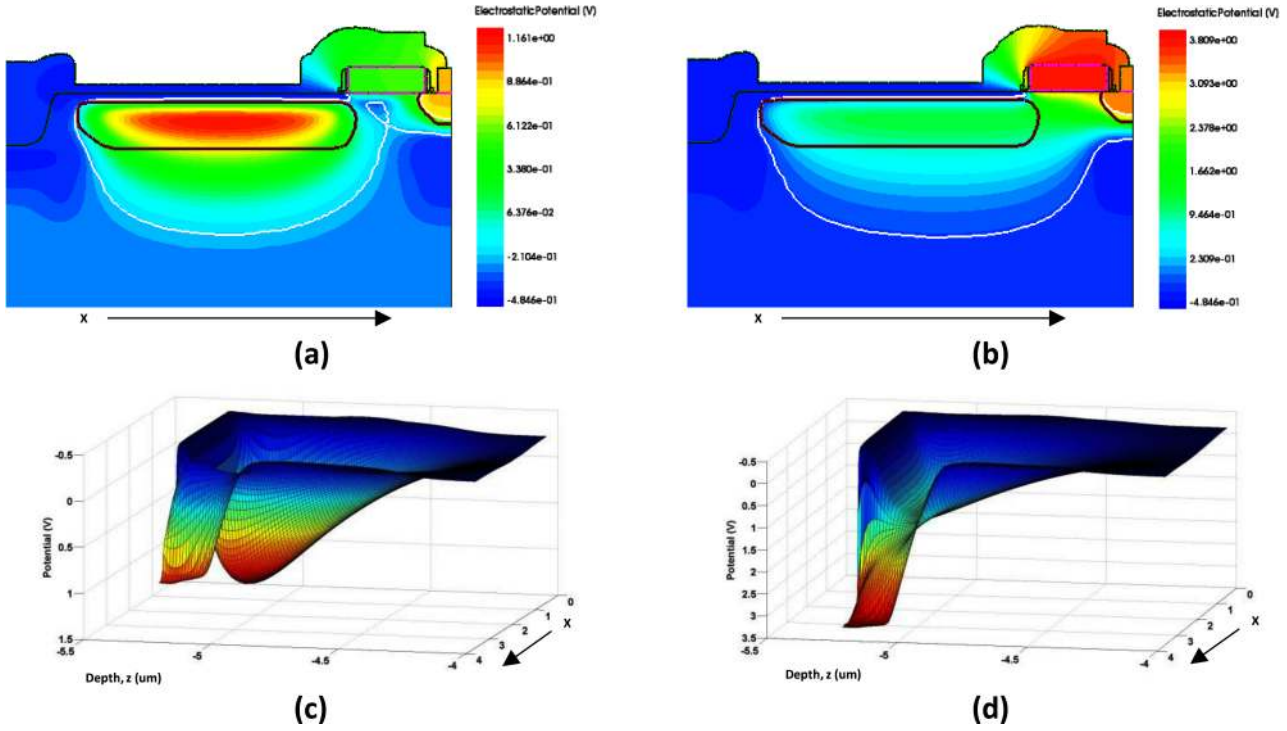

Fig. 6. Potentials inside the PPD. (a) Empty SW with TG "off" and some signal on FD. (b) Empty SW with TG "on" showing monotonically increasing potential from SW to FD. FD has been reset. (c) 3D visualization of potential corresponding to (a), with depth, z, into semiconductor from left to right, surface at left, and x position as labeled with TG barrier front and left. (d) 3D visualization of potential corresponding to (b). Note change in potential scale between figures. Scale for x-axis is microns. Depth scale origin set by TCAD prior to epitaxial layer growth step.

extend the depletion region as deeply as possible to improve collection efficiency and reduce crosstalk. Tailoring of doping profiles has been suggested for individual red, green and blue pixels [57]. Retrograde doping in the p-region can aid carrier collection due to a built-in electric field in the undepleted region below the storage well [58]–[60]. Longer wavelength (e.g. near-infrared or NIR) photons may be absorbed deeply in the $p+$ substrate and the signal carriers recombine before diffusing to the SW region, or in the case of VOD, blocked by a potential barrier. Shallow trench isolation (STI) is most commonly used for pixel isolation although deep trench isolation is being explored for improved cross talk reduction [61], [62]. A more heavily doped p-type region under FD and in other places helps repel photoelectrons so they may be collected by the storage well.

B. Basic Operation

Signal carriers are collected and integrated in the SW prior to readout. The SW is isolated from FD by a low voltage on TG. To achieve correlated double sampling of the signal carriers, FD is reset by the reset transistor (RST) as the first step in the readout cycle and then left floating. The floating potential of FD is sampled by the readout signal chain using source-follower SF. TG is then pulsed high to transfer signal carriers from SW to under TG and on to FD. The TG pulse voltage, the doping profile under TG, and the FD potential must cause a monotonic increase in potential from the SW to FD to allow complete transfer of all signal carriers from SW to FD. Any carriers under TG at the end of the transfer should be subsequently transferred to FD at the end of the pulse period and not back to SW. An example of a monotonically increasing potential is shown in Fig. 6.

The change in potential ΔVon FD is determined by the capacitance C of the FD node and the photogenerated charge Q_{ph} transferred from SW to FD. The ratio of $q\Delta V/Q_{ph}$is the conversion gain with value of the order of 50 uV/e-. If not limited by the readout signal chain, the full well of the pinned photodiode N_{FW}, measured in signal carriers, is determined by the lesser of the capacity of SW or the capacity of FD for complete charge transfer. Generally, increasing the dopants in the SW increases its capacity but also increases the maximum potential of the empty SW and makes complete charge transfer more difficult to achieve for the same transfer gate voltage. Increasing the FD capacity for a given reset potential reduces the conversion gain of the pixel (volts/electron) and increases input-referred read noise.

The primary challenge in fabricating the PPD is achieving both good full-well capacity and complete charge transfer. The challenge increases with reduced operating voltages and smaller pixel size. Secondary challenges include reducing leakage and dark current from the transfer gate, and decreasing charge transfer times.

C. Full Well

The nominal full-well capacity of the SW is evident from Fig. 5 simply as

$$N_{FW} = \frac{1}{q} C_{PPD} \left(V_p - V_B \right) \tag{3}$$

where C_{PPD} is the average capacitance of the PPD. The capacitance C_{PPD} is typically dominated by the $p+n$ junction capacitance and can be readily estimated, but the pinning potential V_p is more challenging to estimate accurately. The pinning potential has been determined analytically by Krymski [63], and more recently by Pelamatti et al. [64]. For more accurate results, TCAD simulation in 2D, or for smaller pixels (e.g. 2.2 um pitch or less), simulation in 3D is required since 2D and 3D effects become important.

The estimate of N_{FW} from (3) is likely high since it is not practically possible to fill a potential well to the brim. This is because of thermionic emission and diffusion of carriers over the barrier in any realistic structure and the need for a practical storage time. It is estimated that an extra barrier height of about 0.5 volts ($20kT$) is required to keep electrons in the well [65], [66] although thermionic emission occurs at all barrier heights and there is no absolute cut off for the process. Under illumination, it is possible that optical carrier generation balances emission across the barrier and a solar-cell-like logarithmic dependence of full well as a function of illumination level might be realized [64].

Good image quality typically requires at least 3,000 electrons full-well capacity since 3,000 electrons with 3 e- rms read noise yields a maximum dynamic range $DR = 20\log(\frac{3000}{3})$ of 60 dB and a maximum shot-noise limited SNR of $3000/\sqrt{3000} = 34$. Dynamic range can be improved by reducing read noise and employing other techniques not addressed here. Shot-noise limited SNR can be improved by optimizing quantum efficiency. Larger pixels, e.g. 6 um pitch, like those used in DSLR camera applications, may have full wells as large as 40,000 e- or higher [67] achieving a maximum SNR of 200 and dynamic range greater than 80 dB.

D. Noise and Lag

Noise from PPD pixels is typically limited by readout electronics such as the first source-follower, rather than from the PPD or FD itself, since CDS suppresses the reset noise on FD. Read noise is typically under 3 e- rms in most commercial devices. However, higher conversion gain can help reduce input-referred read noise at the expense of lower charge handling capacity.

If the potential between SW and FD does not increase monotonically from any point in the PPD structure, there exists a barrier to charge transfer and some signal carriers may never be removed even after long transfer times as shown in Fig. 7. Thus, barriers can lead to both lag (defeating the major intended advantage of the original invention) and noise [68–70]. For very small barriers and longer transfer times, it is possible that all the nominally blocked carriers will be thermionically emitted over the barrier before the end of the TG pulse period and thus such barriers are effectively inconsequential [71]. In the case of slightly larger barriers, the lag from a small reservoir of blocked carriers may be acceptably small.

Lag can also arise from deeply generated photocarriers that are not collected by SW prior to charge transfer. The problem becomes more acute at longer wavelengths and when diffusion is the carrier collection mechanism for SW. Lag can also arise from carrier trapping by defects either in the SW, or under TG. The use of a VOD structure can reduce lag and carrier crosstalk due to deeply generated carriers by blocking them from the SW [72]. However, this is often more easily accomplished by using 3-7 microns of p-epitaxial layer on $p+$ substrate where these deep unwanted photocarriers can recombine.

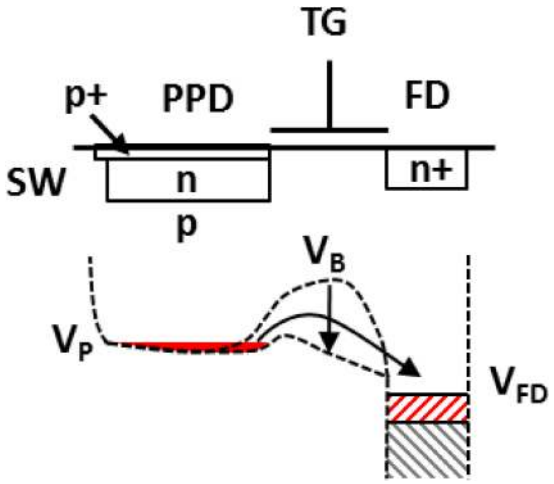

Fig. 7. Example of a barrier that can lead to incomplete charge transfer, lag and noise.

E. Charge Transfer

The transfer physics of carriers from the PPD is similar to CCD charge transfer and many models of transfer time and noise have been published [e.g., 14,73,74,75]. Self-induced drift dominates initial transfer for large signals. For small pixels, fringing fields lead to rapid end-stage transfer. For field-assisted transfer across distance l, transfer time scales as l^3, so for smaller pixels, transfer time is reduced both by an increase in fringing field from TG and from reduced lateral dimension of the SW. However, in larger pixels with "flat" potentials in the SW, transfer becomes diffusion-limited for end-stage transfer. The average transfer time scales as l^2/D_n where D_n is the electron diffusion coefficient, and can start to become significant for larger pixels. For example, at 5.6 um, the average transfer time is 12 nsec but at 40 um it grows to 600 nsec. The time to ensure complete charge transfer may be a factor of 5-10x longer. To increase the rate of charge transfer, a lateral electric field can be created by additional implants or by varying the width of PPD [76]–[79]. The transfer time is then dominated by the drift velocity.

Care must be taken in layout to avoid reducing the width of the PPD channel or transfer gate (TG) transistor such that 3-D "narrow channel" effects cause a reduction in channel potential and increase the barrier to charge transfer. This can happen in diagonal transfer gate layout at the corner of the PPD, for example.

F. Blooming and Dark Current

Blooming in the PPD occurs when the full well capacity of the SW is exceeded. In essence, the PPD becomes a photovoltaic device and excess carriers diffuse away from the

SW. However, the diffusion process is greatly affected by the potential profile in the vicinity of the PPD and carriers typically preferentially diffuse under TG to FD. From FD, further diffusion can occur under the reset gate to the reset drain. In essence, the reset transistor becomes a built-in lateral overflow drain. Thus, blooming in the PPD in a CMOS image sensor is not as consequential as it is in a CCD ILT pixel where the excess carriers bloom into the readout CCD and contaminate many other pixels in the image (although adjacent pixels may be impacted in CIS [80].) Hence, the advantage of a VOD structure is relatively moot in a CMOS implementation of the PPD except for rejecting deeply generated carriers. VOD implementation is also not readily possible with BSI.

Dark current in image sensors can vary significantly from pixel to pixel depending on local defects and statistical process variations, leading to some pixels with very high dark current. These outlier pixels result in "white spot" blemishes in the image. Compared to other photogate structures (e.g. MOS), the PPD has very low average dark current with state-of-the-art values below 15 e-/s at 60C for a 1.4 um pixel and concomitant fewer white spots [81]. The shallow $p+$ pinning layer maintains the Si-SiO_2 surface in thermal equilibrium and the high surface hole concentration ensures that Si-SiO_2 interface states are starved by an absence of electrons. Furthermore, the absence of a metal contact (and alloyed spikes) on the $p+$ layer also contributes to the low dark current. Similarly, with almost the remainder of the SW surrounded by high quality neutral silicon with long minority carrier lifetime, dark current collection by diffusion is also very low. Higher doping concentrations, especially in the SW to increase N_{FW}, can increase electric field strengths resulting in higher average dark current and more white spots. However, reduction of dark current is a never-ending quest and recurring issue as new processes are introduced as part of pixel shrink.

The weak link in dark current is the adjacent TG. Depending on the 3D doping profile and biasing of the TG, dark current can be generated by Si-SiO_2 interface states, or by defects below the surface, and collected in the SW. It is not surprising that the detailed fabrication process around the edge of the TG is highly engineered in a PPD. Not only must the profile result in no significant barrier for complete charge transfer, but defects must also be minimized. A small built-in field under TG that drives dark current to FD instead of SW is sometimes introduced [82]. Negative bias on TG during signal integration can help draw holes to under the PPD edge of TG and suppress dark current generation from Si-SiO_2 interface states [83]–[85]. Negative bias on TG can also help increase the full-well capacity by increasing the barrier between SW and FD and/or reduce leakage current from SW to FD. Increased gate length of TG beyond minimum length improves fabrication ease and improves barrier control.

IV. Fabrication

The fabrication processes that have been used for making PPD devices have been rarely published except in the patent publication literature until recently [86]. For the PPD, the alignments between the pinning layer edge, storage well edge, and the transfer gate TG, are critical, and depend on doping and operational conditions. In the past, spacer and dummy layers and angled implants were often used to achieve the desired alignments to reduce barriers and dark current [87]. In more recent devices, angled implants are not typically used because of shrinking dimensions, better lithography, and better modeling. Eliminating angled implants (aside from normal tilt) simplifies shared-readout layout.

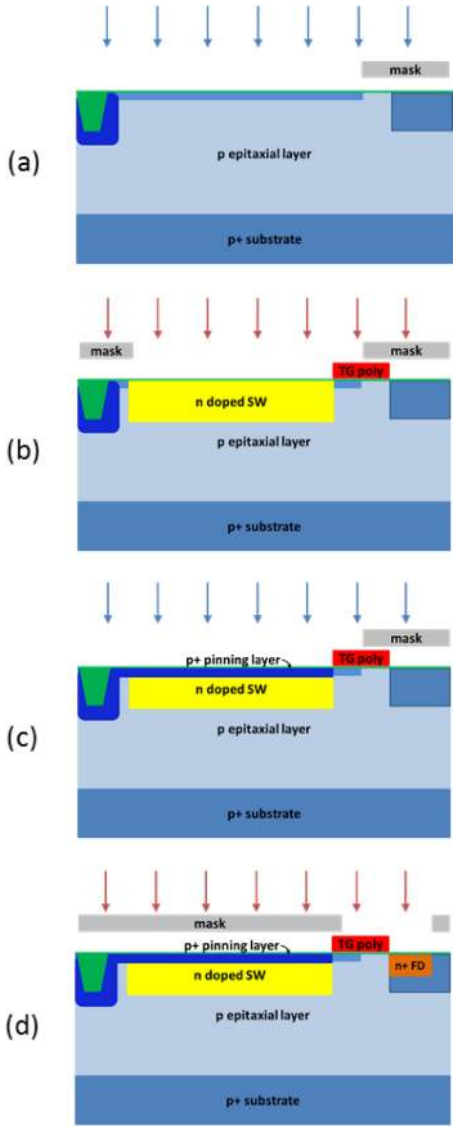

Fig. 8. Examples of essential PPD fabrication implants: (a) TG threshold adjust: B $1.5x10^{12}/cm^2$ at 10keV, (b) SW formation: p $2.5x10^{12}/cm^2$ at 65keV, (c) pinning layer formation: BF_2 $1x10^{13}/cm^2$ at 10keV, (d) FD formation: As $1.0x10^{15}/cm^2$ at 35 keV plus P $7x10^{14}/cm^2$ at 20keV.

For educational purposes, in Fig. 8 we present a hypothetical fabrication process flow (focused on the PPD) for which TCAD shows the desired functionality. These fabrication conditions result in the structure and potentials shown in Figs. 4-6.

An example of a fabricated 1.4 um pitch, 1.35T (8-way shared readout) commercial BSI CMOS image sensor is shown below in Figs. 9–11 [88].

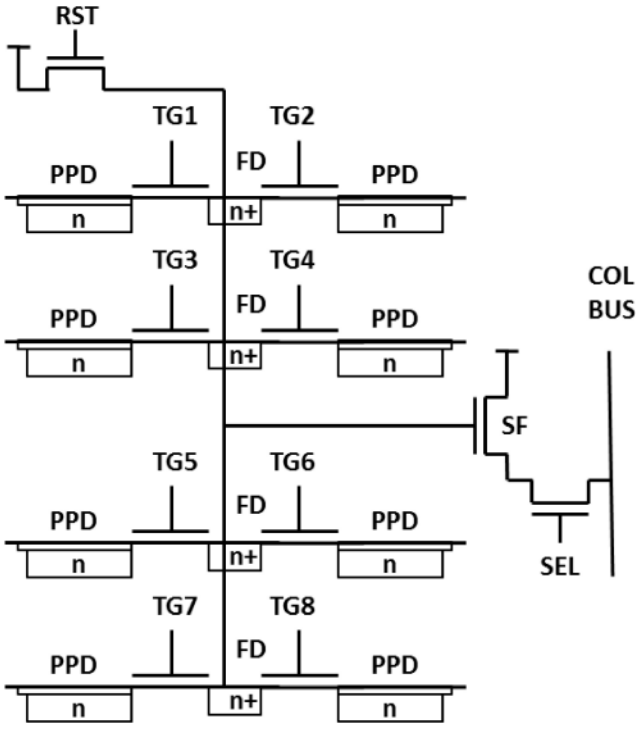

Fig. 9. 8-way shared readout 1.35T pixel schematic.

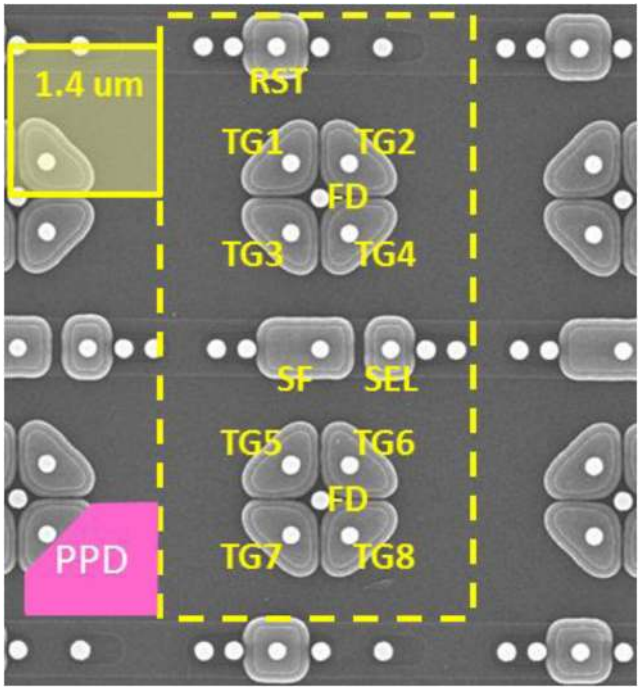

Fig. 10. Annotated microphotograph of partially etched frontside surface of 1.375T BSI CMOS image sensor showing clover leaf clusters of shared readout transfer gates. The dashed line encloses 8 pixels with one shared readout. One PPD region is shown in pink (from SCM data). Photo courtesy of R. Fontaine/Chipworks.

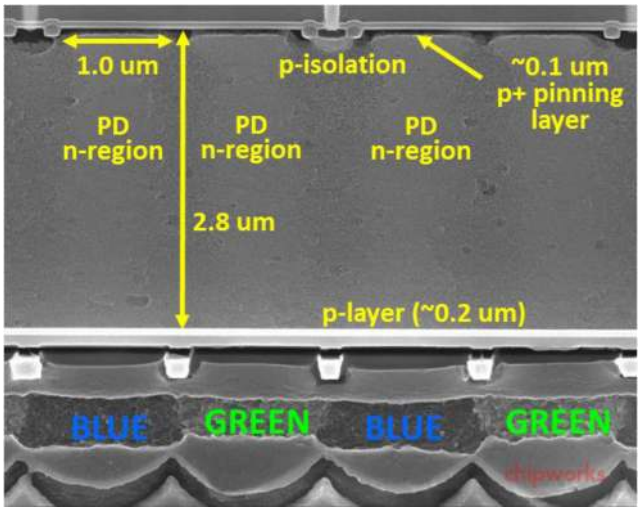

Fig. 11. Annotated microphotograph of cross-section of BSI CMOS image sensor. For BSI, light enters at the bottom, travelling through microlenses and color filters before entering the backside of the silicon chip. Photo courtesy of R. Fontaine/Chipworks.

V. Pixel shrink

Scaling of pixels is an important aspect of image sensor technology roadmaps [89], [90]. Generally, pixel pitch follows Moore's Law; the number of transistors per unit area doubles every two years – which for pixels suggests the pitch should halve every four years [91]. If the minimum feature size (or technology node) is L, pixels typically scale between $10L$ to $20L$ [89], [91], [92] depending on shared readout and other design factors. This is illustrated in Fig. 12. The number of pixels in 0.18 um technology reflects the accessibility of this node by users in a number of communities.

Recently, there has been a slowing of pixel size shrink rate to below that anticipated by the simple Moore's Law. This is due to both technological and physical challenges of making sub-diffraction limit (SDL) pixels as well as relaxation of the market-driven race for more megapixels per sensor. The same data of Fig. 12 is replotted in Fig. 13 as a function of reported year. A line showing the Moore's Law slope is shown for reference.

Reduction of operating voltages continues to challenge the complete transfer of charge from the PPD SW. To partially compensate, the pinning voltage of the PPD has been reduced. Combined with the reduced area of shrunken pixels, the full-well capacity of the PPD has emerged as a major issue in scaling. Better use of the vertical dimension and corrugated topology to increase charge handling capacity is expected in the future. [93]–[96]. Compensating small full well through faster readout times and digital integration has been proposed as an alternative approach. [97]–[99].

One fundamental property that is not scalable is photon absorption length. As pixels shrink, the aspect ratio of pixel pitch to absorption length has inverted from greater than unity to substantially less than one. This exacerbates issues with optical crosstalk between adjacent pixels.

VI. Use in other applications

The CMOS active pixel sensor combined with the pinned photodiode has found use in applications adjacent to consumer cameras as discussed below.

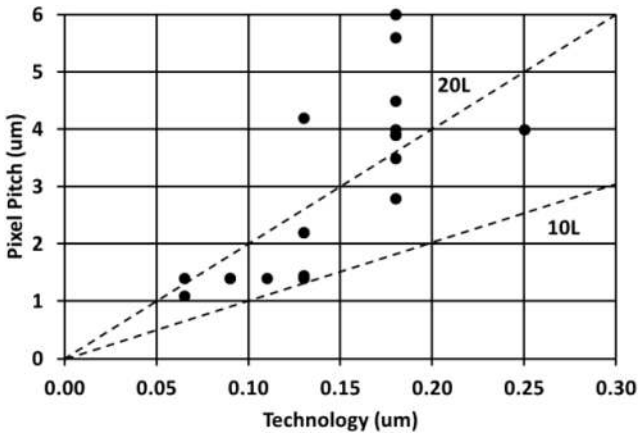

Fig. 12. Sampling of reported pixel pitch as a function of technology node. Both 20*L* and 10*L* scaling shown by dashed lines.

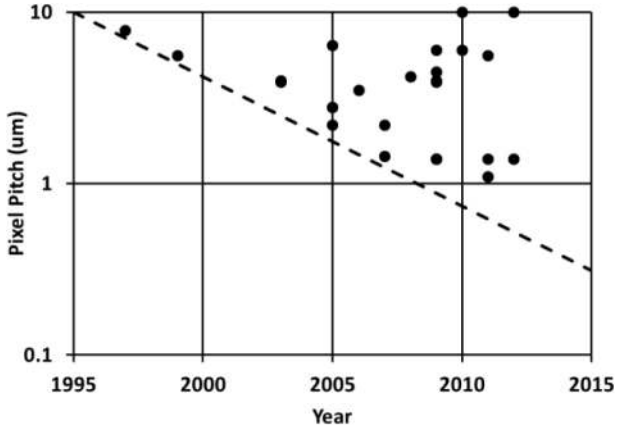

Fig. 13. Sampling of reported pixel pitch as a function of year. The Moore's Law slope is shown for reference.

A. Global Shutter

Global shutter is important for some imaging applications that cannot tolerate artifacts generated by a rolling shutter such as high speed motion capture cameras. Adding a global shutter function to the pixel invariably increases minimum pixel size. It can be implemented by adding another charge transfer stage to each pixel so that charge is transferred from the pinned photodiode SW to a second storage area. For readout, charge is transferred from storage area to the FD. Proposed in the mid-nineties [100], it was first reported using pinned-photodiode technology in 2009 [101]. A novel pump-gate global shutter using two pinned diode structures was presented by Aptina in 2013 [102]. The CMOS image sensor global shutter can also be implemented in-pixel with sample-hold circuits which may be more compatible with BSI technology due to possible optical contamination of the stored signal, though CDS may be more challenging.

B. Time-of-Flight Ranging Application

Time-of-flight (ToF) sensors used for measuring the distance to objects in the scene have also used the pinned photodiode. In this application, typically two or more output ports, or transfer gates from the pinned region are used and modulated at high frequency. [103], [104]. Due to the short transit times required, e.g. under 10 nsec, either small pixel sizes or channels with lateral drift field are required [105]. Mixed mode color and ToF sensors, so-called RGBZ sensors, have also employed pinned photodiode devices [106], [107].

C. Radiation Effects

The use of CMOS image sensors in space and high energy physics experiments has led to a number of recent studies on the radiation hardness of PPDs in CMOS image sensors [108]–[110]. Generally, compared to CCDs, CMOS image sensors are quite radiation hard. However, an increase in room temperature dark current with total dose, typically associated with the transfer gate, remains an issue.

VII. Conclusion

The pinned photodiode has been in use for nearly 30 years and has been utilized in both first generation and second generation solid-state image sensors. It will not be surprising if the PPD is adopted for use in some third generation solid-state image sensor in the future. It is likely that the essential concepts of the PPD will be retained, such as storage well isolation from surface effects and complete charge transfer, whereas the detailed structure may change. If new materials replace silicon as the primary photodetector, they will have a difficult time achieving the high performance of the silicon pinned photodiode.

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