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A Rigorous Approach to the Robust Design of Continuous-Time $\Sigma\Delta$ Modulators

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***Abstract*—In this paper we present a framework for robust design of continuous-time $\Sigma\Delta$ modulators. The approach allows to find a modulator which maintains its performance (stability, guaranteed peak SNR, ...) over all the foreseen parasitic effects, provided it exists. For this purpose, we have introduced the $\mathcal{S}$-figure as a criterion for the robustness of a continuous-time $\Sigma\Delta$ modulator. This figure, inspired by the worst-case-distance methodology, indicates how close a design is to violating one of its performance requirements. Optimal robustness is obtained by optimizing this $\mathcal{S}$-figure. The approach is illustrated through various design examples and is able to find modulators that are robust to excess loop delay, clock jitter and coefficient variations. As an application of the approach, we have quantified the effect of coefficient trimming. Even with poor trim resolution, good performance can be achieved provided beneficial initial system parameters are chosen. Another example illustrates the fact that also the out-of-band peaking behaviour of the signal transfer function can be controlled with our design framework.**

***Index Terms*—analog-to-digital (A/D) conversion, continuous-time sigma-delta ($\Sigma\Delta$) modulation, robust stability, robust performance.**

I. Introduction

$\Sigma\Delta$ modulation has become a standard technique for high-accuracy analog-to-digital (A/D) conversion. For high-bandwidth applications the family of continuous-time (CT) $\Sigma\Delta$ modulators has shown substantial advantages over the more traditional discrete-time (DT) variant in the last few years [1]–[3]. To achieve good performance over a large bandwidth, these modulators usually combine a low oversampling ratio (OSR) with a multibit quantizer, which is also the focus of this paper.

Fig. 1 shows the general block diagram of such a CT $\Sigma\Delta$ modulator with multibit quantization. It consists of a CT loop filter $H(s)$, a feedback digital-to-analog converter (DAC) which is represented by the transfer function $H_{DAC}(s)$ and a multibit quantizer sampled at f_s. It is well justified to replace this quantizer by an additive DT white noise source $Q(z)$. By using the impulse-invariant-transformation (IIT) an equivalent DT loop filter $H_{eq}(z)$ can be identified which can be linked

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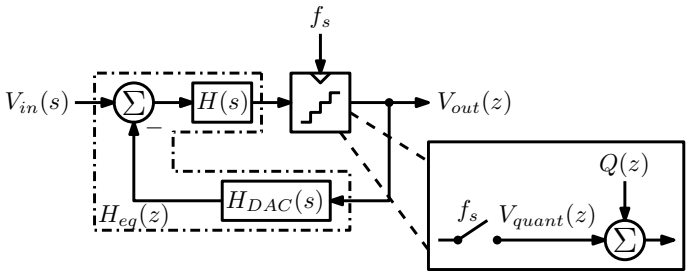

Fig. 1. General block diagram of a CT $\Sigma\Delta$ modulator with identification of the equivalent DT loop filter and the linearized quantizer model.

to the discrete-time (DT) noise transfer function (NTF) [4]:

$$H_{eq}(z) = \text{IIT}\{H(s)H_{DAC}(s)\} = \frac{1 - NTF(z)}{NTF(z)} \quad (1)$$

With the introduction of the NTF, the output of the modulator can be written as:

$$V_{out}(z) = \big[\underbrace{H(s)NTF(e^s)}_{STF(s)} V_{in}(s)\big]^* + NTF(z)Q(z) \quad (2)$$

The $*$-operator denotes the sample operation as in [5]. The signal transfer function (STF) indicates the contribution of the input signal and should be close to unity in the signal band. The contribution of the quantization noise signal $Q(z)$ is similar to DT $\Sigma\Delta$ modulators.

A well-established design methodology for CT $\Sigma\Delta$ modulators consists of first choosing the NTF according to one of the design strategies from DT modulators [6], [7]. In a second step this NTF is mapped on a CT loop filter $H(s)$ using the inverse IIT. However, it is well known that CT $\Sigma\Delta$ modulators are sensitive to various parasitic effects, which are much less pronounced in DT modulators. Amongst them are integrator coefficient RC variations, excess loop delay (ELD), parasitic poles and zeros in the integrator transfer functions and increased clock jitter sensitivity [8]–[11]. All these effects make that the actual implemented NTF deviates from the desired one [12]. This way, the modulator's performance can vary largely from wafer to wafer or even from die to die. To tackle these problems, current designs often add features such as trimming and/or calibration options [1], [2].

In this paper we present a new design strategy which already incorporates the knowledge on realistic parasitic effects. We will choose the system parameters directly in the CT domain, in such a way that the system maintains its performance requirements over all foreseen parasitic effects. In section II we will give a brief overview of possible parasitic effects and

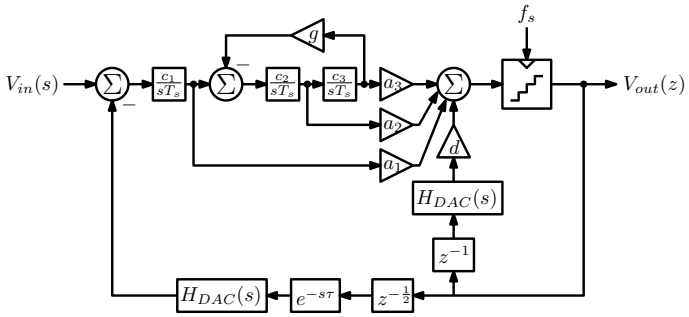

Fig. 2. Third-order CT $\Sigma\Delta$ modulator architecture with the loop filter in a feedforward (FF) topology.

how they are incorporated in our system model. Section III introduces a framework for robustness consisting of a parametric system model, normalized parameter variations and modulator performance requirements. The $\mathcal{S}$-figure is introduced as a figure of merit to express the modulator's robustness. In section IV we focus on how to calculate the $\mathcal{S}$-figure and on its use as a design optimization criterion. Section V contains some design examples and finally, section VI gives a conclusion.

II. Parasitic Effects in Continuous-Time $\Sigma\Delta$ Modulators

We will now briefly review some important parasitic effects in a CT modulator which are required for the remainder of the paper. Without loss of generality, we will use the third-order CT $\Sigma\Delta$ modulator architecture shown in fig. 2 to illustrate the main effects. The loop filter is a feedforward (FF) topology with zero spreading in the signal band. It is common practice to relax the settling of the quantizer by introducing a flip-flop in the feedback path. Here the delay is set to half a clock cycle. This way explicit ELD is introduced, which is compensated by a direct feedback path to the input of the quantizer [1], [2], [8], [10], [13]. A current-steering feedback DAC is present, which generates a non-return-to-zero (NRZ) pulse:

$$H_{DAC}(s) = \frac{1 - e^{-sT_s}}{s} \tag{3}$$

It is important to notice that this architecture is purely instructive and that the effects described here are equally present in a feedback (FB) or a hybrid FF/FB topology, potentially also with other types of feedback DACs.

A. Coefficient Variations

The loop filter integrators can be implemented by opamp-RC circuits or alternatively by using g_mC-integrators. Either way the integration coefficients c_i are determined by a combination of a capacitance and a resistance. Since these are two devices of a different type, large process variations are expected on the integrator coefficients:

$$c_{i,actual} = c_{i,nominal}(1 + \delta_{IC}) \tag{4}$$

Here δ_{IC} is a statistical parameter and can easily range up to $\pm$ 20 %:

$$-|\delta_{IC,max}| \leq \delta_{IC} \leq |\delta_{IC,max}| \tag{5}$$

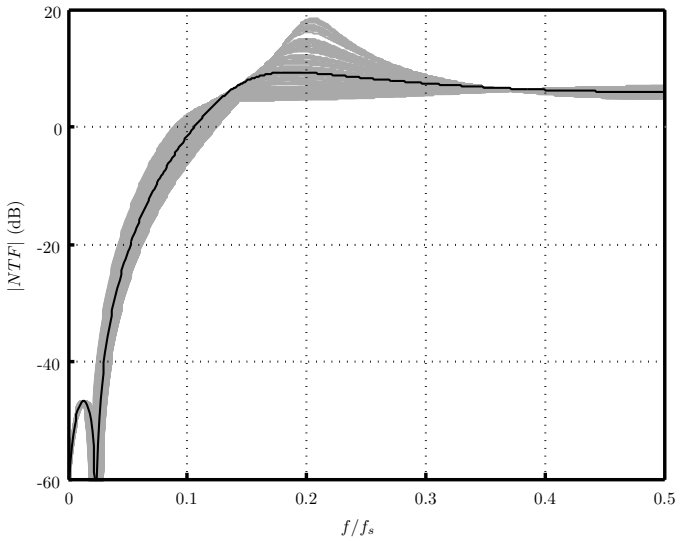

Fig. 3. Effect on the NTF for $\pm$ 20 % coefficient variations in the architecture of fig 2. ($a_1 = 1$, $a_2 = 1$, $a_3 = 1$, $c_1 = 1.6845$, $c_2 = 0.5927$, $c_3 = 0.2588$, $d = 0.7236$, $g = 0.1508$, $\tau = 0$)

where $|\delta_{IC,max}|$ equals 20 %. Although mismatch can also create deviations between the integrator coefficient errors, we assume δ_{IC} is equal here for all integrator coefficients within the same modulator. By design the mismatch error can indeed be made quite small (1% or less), while the process variations cannot be avoided.

The other coefficients in the system model are assumed to be exact. In a typical implementation the a_i feedforward coefficients (or feedback coefficients in a FB topology) are determined by a ratio of resistor or capacitor values. This is also true for the direct feedback coefficient d. Hence they are only subject to mismatch (which is neglected here).

Fig. 3 shows the effect of coefficient variations of $\pm$ 20 % on the NTF for a typical 3rd-order modulator design. The nominal NTF is shown in black, while the gray band indicates the influence of the variations. All modulators remained stable but from the figure it is clear that the out-of-band gain ($\mathcal{H}_\infty$) varies over more than 5 dB. As such, for an OSR of 16 and a 3-bit quantizer, the signal-to-noise ratio (SNR) of the nominal system was 77.8 dB while the actual modulators (with coefficient variations) reached SNR values in the range of 69 to 79 dB.

B. Excess Loop Delay (ELD)

Although the ELD seems fixed here by an explicit synchronization flip-flop in the feedback path (the factor $z^{-1/2}$ in fig. 2), this does not completely resolve the issue for high-bandwidth designs. In this case the parasitic delay τ of the synchronisation latch is no longer negligible compared to the sampling period T_s. Moreover this parasitic loop delay is sensitive to process-voltage-temperature (PVT) variations. In a design with up to GHz clock frequency [1], [14] its nominal value may well be as high as 10 % of the sampling period, with a variation of 50 %. Formally this leads to:

$$\tau_{actual} = \tau_{nominal}(1 + \delta_\tau) \tag{6}$$

where $\tau_{nominal}$ can be e.g. $T_s/10$ and δ_τ is bounded:

$$-|\delta_{\tau,max}| \leq \delta_\tau \leq |\delta_{\tau,max}| \tag{7}$$

with $|\delta_{\tau,max}|$ equal to 50 %.

C. Parasitic Poles and Zeros

Depending on the actual integrator circuit topology (single-stage opamp-RC, two-stage opamp-RC with Miller compensation, g_mC, ...), the integrator coefficient c_i may be affected and multiple parasitic poles and zeros can be present. If needed all of these can be incorporated in the design framework presented here. Usually it is sufficient to take the dominant parasitic pole into account:

$$TF_{int,actual} \approx \frac{c_i}{sT_s}\frac{1}{1+s\tau_p} \tag{8}$$

In most cases the parasitic time constant τ_p corresponds to the opamp's GBW [9]. This way, τ_p is largely controlled by the designer, but similar to the integrator coefficients, there is an uncertainty of up to $\pm 20\%$ or more on its value.

D. Clock Jitter

Finally, a CT $\Sigma\Delta$ modulator is known to be sensitive to clock jitter [10]. This gives rise to an additional in-band noise component, depending on the DAC pulse used. In the case of an NRZ pulse the in-band noise contribution for the case of wideband white jitter equals [11]:

$$IBN_{jitt} = \frac{\sigma^2_{\Delta T_s}}{T_s^2}\frac{1}{2\pi OSR}\int_0^{2\pi} |(1-e^{-j\omega})NTF(e^{j\omega})|^2 \frac{\Delta^2}{12} d\omega \tag{9}$$

Here $\sigma^2_{\Delta T_s}$ corresponds to the jitter variance. The jitter noise contribution gets worse for a more aggressive NTF (higher $\mathcal{H}_\infty$).

III. A Framework for Robustness

We will now set up a framework to find a system-level design which maintains its performance (peak SNR, stability, ...) against possible parasitic effects that can occur. The design framework consists of 3 elements: a parametric system model (such as the one from fig. 2), normalized variations on some of the system parameters and performance requirements. These 3 elements are combined into one number, the $\mathcal{S}$-figure. It expresses the degree in which the current system parameter selection is able to meet all the performance requirements, even in the presence of variations on these parameters.

We will clarify the design framework by means of a one dimensional example. This means that only one parameter variation is present. This will be extended in Section IV.

A. System Model

The system model describes the construction of the loop filter and its design parameters. As system model we use the 3rd-order modulator architecture from fig. 3 here. However, we will fix some of the parameters by forehand. We choose all feedforward coefficients (a_i's) equal to 1. As such we do not account for scaling of the integrator outputs, which can always be done afterwards. Also we do not account for parasitic loop delay here, which makes $\tau = 0$. In each integrator transfer function we introduce a fixed parasitic pole at $2\,f_s$ according to equation (8). The only design parameters which remain this way, are the integrator coefficients c_i, the zero spreading coefficient g and the direct feedback coefficient d. As DAC type we choose a NRZ-DAC. The OSR is fixed at 16 in combination with a 3-bit quantizer.

B. Parameter Variations

In this illustrative example we will only introduce one parameter variation, namely the RC variation on the integrator coefficients. As described by equation (5) we can expect up to say 20 % variation. In our framework we will normalize the parameter variations:

$$\Delta_{IC} = \frac{\delta_{IC}}{|\delta_{IC,max}|} \tag{10}$$

This way equation (5) can be rewritten as:

$$-1 \leq \Delta_{IC} \leq 1 \tag{11}$$

The procedure for including other variations, such as parasitic loop delay described by equation (7) or variation on the parasitic pole and/or zero locations, is straightforward and leads to similar normalized Δ's.

C. Performance Requirements

The third step consists of the formulation of the performance requirements. An obvious requirement is of course stability. The poles p_i of the NTF must always stay inside the unit circle, independent of the parameter variations. Next to this also the peak SNR must be preserved, which can be calculated through the maximum stable amplitude (MSA) [10] as:

$$SNR_{peak} \approx \frac{(MSA)^2}{2IBN} \tag{12}$$

where IBN corresponds to the in-band quantisation noise:

$$IBN = \frac{1}{2\pi}\int_0^{\frac{\pi}{OSR}} |NTF(e^{j\omega})|^2 \frac{\Delta^2}{12\pi} d\omega \tag{13}$$

The MSA on itself can be estimated by the following equation:

$$MSA \approx V_{FS} - \frac{3}{2}\sqrt{\frac{1}{2\pi}\int_0^{2\pi} |NTF(e^{j\omega})-1|^2 \frac{\Delta^2}{12} d\omega} \tag{14}$$

where Δ symbolizes the quantization step and equals

$$\Delta = \frac{2V_{FS}}{2^B - 1} \tag{15}$$

with V_{FS} the full scale quantizer voltage and B the number of quantization bits. Equation (14) originates from the rms value of the contribution of the quantization noise to the input signal of the quantizer, $V_{quant}(z)$ in fig. 1:

$$V_{quant}(z) = [STF(s)Vin(s)]^* + [NTF(z)-1]Q(z) \tag{16}$$

It is important to note that the MSA is defined here with regard to the full-scale output signal of the modulator, and

not with regard to the input. However, as the STF should be close to unity in the signal band, for in-band input signals this MSA-expression is also valid for input amplitudes. Through extensive time-domain computer simulations, we found that equation (14) has a worst-case inaccuracy of about 2 dB as long as the calculated MSA is larger than -3 dB relative to full scale. Fortunately, this is a commonly desired input range. Also other predictions of the MSA e.g. [7] can be used in our approach, but these were found to be too conservative. Equation (14) indicates that, a more aggressive NTF will have a higher risk for quantizer overloading and thus a lower MSA.

As an extra criterion we also require a minimum value for the MSA, such that the modulator can process at least -3 dB input signals. In total we thus have 3 performance requirements for our modulator:

$$\forall i, |p_i| < 1 \tag{17}$$

$$SNR_{peak} > SNR_{peak,guaranteed} \tag{18}$$

$$MSA > \frac{1}{\sqrt{2}} \tag{19}$$

D. The $\mathcal{S}$-figure

We now introduce the $\mathcal{S}$-figure, our figure of merit to quantify the robustness of a CT $\Sigma\Delta$ modulator. We will start by choosing the system parameters such that a maximally flat NTF [6] is designed (with out-of-band gain $\mathcal{H}_\infty = 2.5$). In fact, this leads to the design shown in fig. 3. The nominal peak SNR equals 76.8 dB and we propose a guaranteed peak SNR of 75.5 dB for this design. Variations in the integrator coefficients are inserted, by sweeping the normalized parameter variation Δ_{IC} according to equation (11). It is instructive to represent this graphically, by drawing the performance boundaries on the Δ_{IC} axis (see fig. 4). The valid range for the integrator coefficients is on the Δ_{IC} interval $[-1, 1]$. The performance requirements of equation (17)-(19) are represented by their boundaries as dashed vertical lines. To the left side, as the integrator coefficients become smaller, we expect the peak SNR to drop. In this case, when the relative variation of the integrator coefficients becomes -0.24, the peak SNR of 75.5 dB cannot be guaranteed anymore. To the right side, the integrator coefficients rise, and the NTF becomes more aggressive. We therefore expect both the stability and the MSA boundary to eventually be broken. The MSA requirement is broken when $\Delta_{IC} = 0.64$. Stability is only broken outside the valid parameter range, namely when Δ_{IC} is already 1.45. As such, the maximally flat design example will remain stable over all foreseen parameter variations. However, it is not possible to meet the peak SNR and MSA requirement over the entire variation range. The $\mathcal{S}$-figure is now identified as the minimum normalized variation that will cause one of the performance boundaries to be broken. In this case, the $\mathcal{S}$-figure is connected to breaking the SNR contrstaint and equals 0.24.

We now propose a different parameter selection for the design which will prove to be more robust than the maximally flat design. The coefficients are $c_1 = 2.0252$, $c_2 = 0.3805$, $c_3 = 0.6289$, $g = 0.1532$, $d = 0.8435$. Again all FF coefficients are equal to 1. The nominal NTF reaches a peak

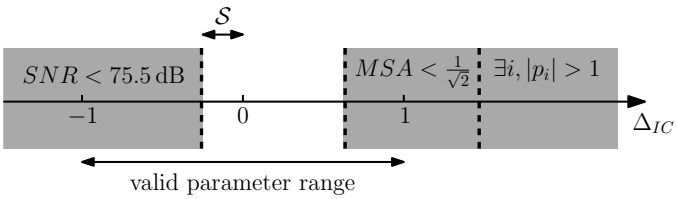

Fig. 4. Graphical representation of the performance boundaries on the Δ_{IC} axis for a 3rd-order maximally flat design with only one parameter variation.

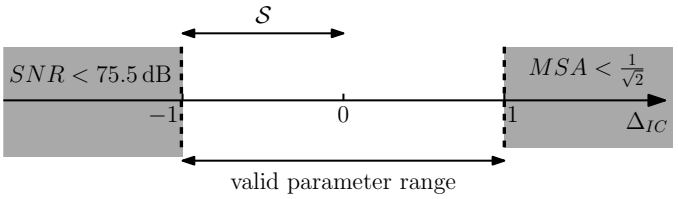

Fig. 5. Graphical representation of the performance boundaries on the Δ_{IC} axis for a 3rd-order optimal design with only one parameter variation.

SNR of 77.4 dB here, only slightly more than the maximally flat design. Fig. 5 again shows the graphical representation of the performance boundaries. We get a completely different image here. The distance to breaking the stability boundary is not shown in the figure anymore, as this only happens for $\Delta_{IC} = 3.2$. Both the distances to the peak SNR and MSA boundary are 1 and the resulting $\mathcal{S}$-figure thus equals 1. This means that the system is robust against the full 20 % variation of the integrator coefficients. Suppose now that $\mathcal{S}$ was larger than 1. This would mean that the system could tolerate higher variations than foreseen and either it could achieve a higher peak SNR or a higher MSA. Furthermore, the nominal system is perfectly centered between the performance boundaries, as this always leads to the maximum $\mathcal{S}$-figure. As such, we denote this system as the optimal system, as it is perfectly centered between at least two of the performance boundaries with distance to these boundaries (or $\mathcal{S}$) equal to 1.

Fig. 6 shows the resulting NTFs of the optimal system with the influence of the parameter variations. Similar to the maximally flat design of fig. 3, $\mathcal{H}_\infty$ is about 9 dB. However, as we can see, the maximally flat design can have a worst-case $\mathcal{H}_\infty$ of 19 dB due to parameter variations while in the optimal system the out-of-band gain only rises to 12 dB. Clearly the maximally flat design can be identified as a more aggressive system and therefore the MSA criterion cannot be fulfilled over all variations. Also the peak SNR can drop to 69 dB, while the optimal design always achieves a guaranteed peak SNR of 75.5 dB.

Time-domain simulations were performed on perturbated versions of the optimal system. The MSA criterion was always met for input signals in the signal band. However, for out-of-band tones, it is well known that the STF of a FF topology shows peaking and equation (14) is no longer valid. In this case the out-of-band peaking for the optimal modulator was 15.6 dB. Later on, we will show that we can also control the STF with our design framework, to limit the amplification of these out-of-band interferers.

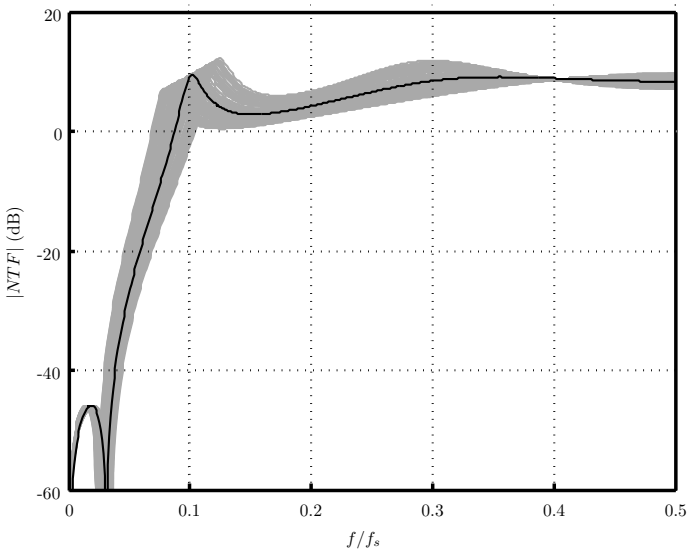

Fig. 6. NTFs with parameter variation influence for the 3rd-order optimal design with only one parameter variation.

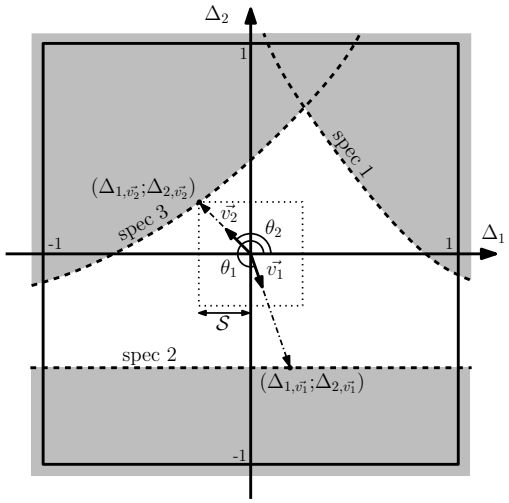

Fig. 7. Graphical representation of the performance boundaries in a 2D parameter variation situation.

IV. Calculation and Optimization of the $\mathcal{S}$-figure

In the previous section we have illustrated the meaning of the $\mathcal{S}$-figure in a graphical way. Furthermore, only one variation was present which allowed an easy interpretation. Here we will extend the $\mathcal{S}$-figure to multiple dimensions and we will provide an effective calculation method. This allows us to use the $\mathcal{S}$-figure as an optimization criterion to find the optimal CT $\Sigma\Delta$ modulator design.

A. The $\mathcal{S}$-figure in Multiple Dimensions

A similar graphical representation as in the previous section is shown in fig. 7 for the case where there are two parameter variations Δ_j and three design specs. In the origin we have the nominal system which should meet the required design specifications by definition. The performance boundaries are again indicated by the dashed lines. Consider now the vector $\vec{v_1}$ which makes an angle θ_1 with the Δ_1 axis. If we increase the norm of this vector, we will cross design spec 2 at the point $(\Delta_{1,\vec{v_1}};\Delta_{2,\vec{v_1}})$. We identify the maximum absolute value of these two coordinates as the "local $\mathcal{S}$-figure" for the direction θ_1, in this case:

$$\mathcal{S}_{local,\theta_1} = \max\left[|\Delta_{1,\vec{v_1}}|;|\Delta_{2,\vec{v_1}}|\right] = |\Delta_{2,\vec{v_1}}| \qquad (20)$$

We can now repeat this procedure for all other angles. A special type of angle is formed by the corner points of the variation space, for which both coordinates change equally when increasing the vector norm in that direction. This is for example the case for the direction θ_2 in fig. 7. Design spec 3 is crossed here and the local $\mathcal{S}$-figure equals:

$$\mathcal{S}_{local,\theta_2} = |\Delta_{1,\vec{v_2}}| = |\Delta_{2,\vec{v_2}}| \qquad (21)$$

The $\mathcal{S}$-figure is now defined as the minimum of all these "local $\mathcal{S}$-figures":

$$\mathcal{S} = \min_{\forall i}\left[\mathcal{S}_{local,\theta_i}\right] \qquad (22)$$

As such, in two dimensions the $\mathcal{S}$-figure equals half of the side of the largest inner square which can be drawn around the origin in the variation plane, without breaking the performance requirements. If the normalized parameter variations remain smaller than $\mathcal{S}$ the system will definitely satisfy all the specifications. The concept can be extended to 3 or more dimensions where the inner square then becomes a cube or a hypercube.

B. Calculating the $\mathcal{S}$-figure

The $\mathcal{S}$-figure is one of the variants of the "worst case distance" methodology [15]. Obviously, determining this $\mathcal{S}$-figure is non-trivial. There are many possible ways to calculate it [15]. Summarizing there are two important aspects. First, we need an efficient algorithm to calculate the "local $\mathcal{S}$-figure" for a given direction. By investigating only one direction, this has become a scalar problem which can always be solved as follows: we start from the origin and we gradually increase the vector norm until the corresponding system violates the design constraints. In our implementation we first made a rough sweep which determines an upper and lower boundary for $\mathcal{S}_{local,\theta_i}$. Then we use a bisectional (binary search) algorithm to obtain a more accurate result.

Second, we need to scan all the possible directions, to find the worst-case "local $\mathcal{S}$-figure". Obviously, this procedure would be numerically intensive. We therefore make the assumption that this worst-case always lies in the direction of one of the diagonals of the search space. E.g. in the 2D example of fig. 7 the location of the $\mathcal{S}$-figure coincides with the direction of vector $\vec{v_2}$ at an angle of 135 °. These diagonal directions correspond to the corners of the square, cube or hypercube built around the origin. Although it cannot be guaranteed that this is always the case, there is a strong intuitive feeling to it. In fig. 7 increasing Δ_2 and decreasing Δ_1 both deteriorate design spec 3. By identifying θ_2 as the worst-case direction, we assume that specification 3 decays

fastest when introducing parameter variations of the same magnitude. Empirically, we have found that this assumption is valid for each of the examples considered in this paper. This extremely simplifies the problem and provides a fast and effective way of determining the robustness of a CT $\Sigma\Delta$ modulator. In fact, this is only possible by choosing the square variant from [15] (using the ℓ_∞ norm). In this way, we really consider the worst case parameter variations, without making any assumptions about the statistics of these variations. For our 2D example this means that we only have to execute the algorithm for finding the "local $\mathcal{S}$-figure" four times. The resulting $\mathcal{S}$ is selected as the minimum of these four values.

C. Optimization of the $\mathcal{S}$-figure

From the discussion above it is clear that this $\mathcal{S}$-figure is an unambiguous figure of merit to assess the robustness of a CT $\Sigma\Delta$ modulator against foreseeable imperfections, and hence it can be used as an optimization target. Finding the most robust modulator now boils down to maximization of the $\mathcal{S}$-figure in function of the design parameters. We used a popular genetic algorithm to perform this optimization [16]. However, this algorithm is only used as a black-box solution to perform the optimization and other global optimization algorithms could be used equally well. The authors want to emphasize that the core of finding the optimal modulator lies in the use of the $\mathcal{S}$-figure and its effective calculation method described in the previous section.

However, we only require the the modulator to be robust against all parameter variations that can occur in practice. In this way, it is sufficient that the modulator has an $\mathcal{S}$-figure that is equal to or larger than 1. Hence we define the optimal modulator as the modulator with the best performance that has an $\mathcal{S}$-figure that is equal to or larger than 1. To find this optimal modulator, we first perform the optimization for reduced performance specs, which are easy to attain even in the presence of parameter variations. In our design examples we first performed the optimization for a low peak SNR. This results in an $\mathcal{S}$-figure much larger than 1. As this system is more robust than needed, we gradually increase the peak SNR and rerun the optimization, with the previously found system included as one of the initial population points for the genetic algorithm. We continue this step until we have found an optimized design with $\mathcal{S}$ reaching 1. If we would further increase the specification on the peak SNR, the design will not be robust against all parameter variations anymore. We identify this design as the optimal CT $\Sigma\Delta$ modulator for the expected parameter variations and for the required performance specs.

V. CT $\Sigma\Delta$ Modulator Design Examples

In this section we will determine the optimal parameters for 3rd-order CT $\Sigma\Delta$ modulator design examples. For all designs we fix the OSR at 16, the number of quantizer bits at 3 and we introduce parasitic poles at $2\,f_s$ in the integrator transfer functions according to equation (8).

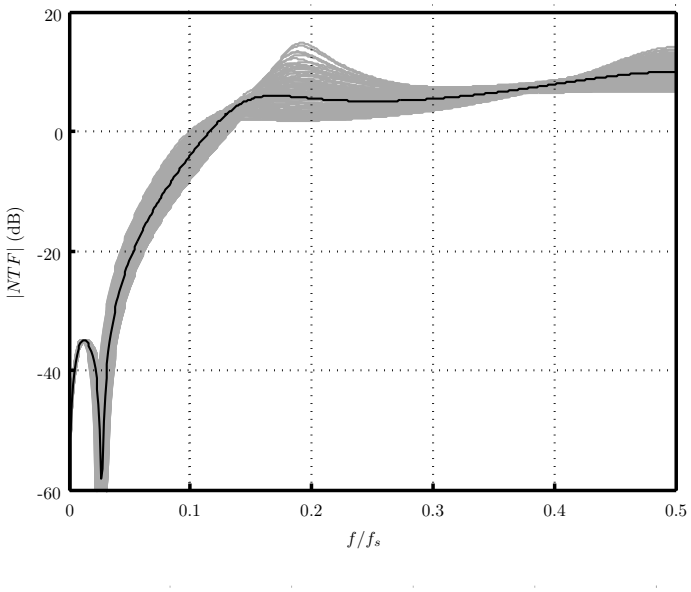

Fig. 8. NTFs with parameter variation influence for the 3rd-order optimal design robust to large RC variations and parasitic ELD.

A. Example 1: Robust to RC Variations and ELD

In the first three examples the modulator architecture of fig. 2 is used. Again, we choose all feedforward coefficients (a_i's) equal to 1. In fact we do an optimization of the loop filter. This is justified as the performance requirements will only be dependent on the loop filter and not on the particular scaling used. The integrator coefficient scaling can therefore be safely done afterwards, without affecting the feasibility of achieving the performance specifications. This scaling can be employed to limit the output swings, while still providing enough suppression of the circuit noise of the following stages. In the first example we introduce an RC variation of 20 % and a nominal ELD of $T_s/10$ with 50 % variation according to equation (7):

$$-0.2 \leq \delta_{IC} \leq 0.2 \quad , \quad -0.5 \leq \delta_\tau \leq 0.5 \tag{23}$$

The performance requirements are taken identical to the ones from equations (17)-(19).

TABLE I
Optimal coefficients for example 1

c_1	c_2	c_3	g	d	SNR_{peak}	
					nominal	guaranteed
1.5492	0.6139	0.0236	1.9092	1.03602	67 dB	64.5 dB

The optimal parameters which give rise to an $\mathcal{S}$-figure equal to 1 are shown in table I. As one can see the third integrator coefficient is already quite low. This indicates the fact that the optimizer actually considers a 2nd-order system as a more robust solution. Increasing the order would normally enhance the system performance, however it also introduces extra sensitivity to parameter variations, which are large here. In this example, clearly the extra variation in the system outweighs the possible performance enhancement by increasing the order.

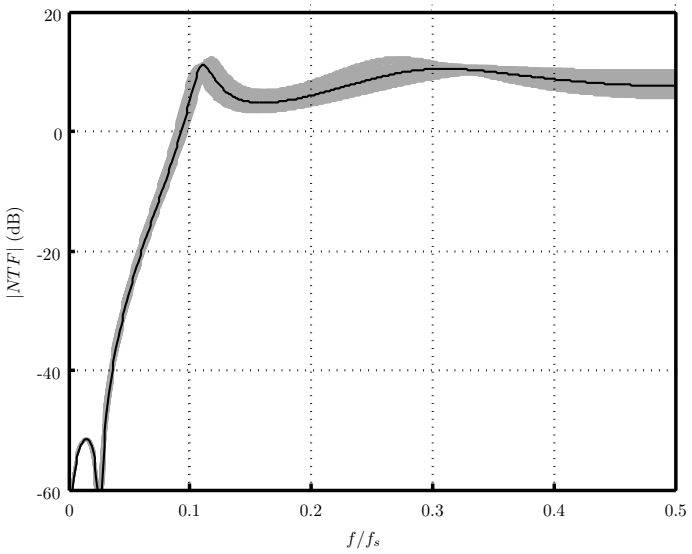

Fig. 9. NTFs with parameter variation influence for the 3rd-order optimal design with modest coefficient trimming.

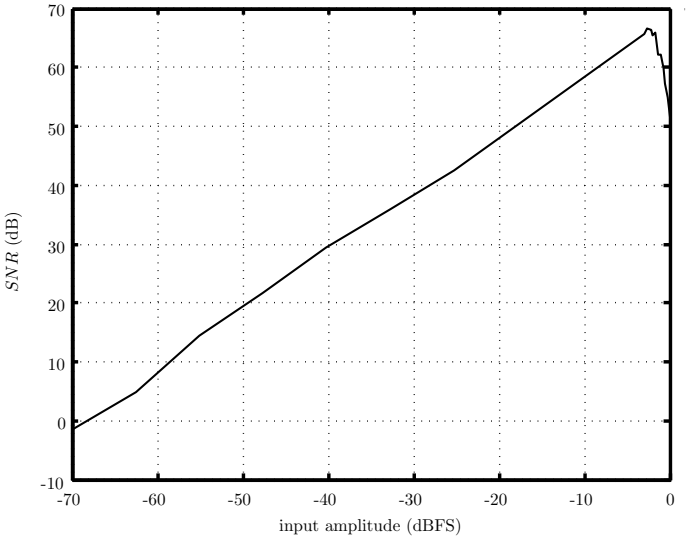

Fig. 10. SNR in function of the input amplitude for the system of table I with perturbation $[\Delta_{IC} = 1; \Delta_\tau = 1]$.

The nominal peak SNR amounts 67 dB and a guaranteed performance of 64.5 dB is achieved. In fig. 8 the influence of the perturbations on the NTF's is illustrated. The influence of ELD in combination with large RC variations is clearly significant, as the guaranteed peak SNR has dropped by more than 10 dB compared to the one dimensional example of section III.

In reality there is also RC variation on the parasitic poles in the integrator transfer functions. However, to not overcomplicate the problem we have neglected this in the optimization. Afterwards the $\mathcal{S}$-figure for the optimal design was recalculated with 20 % variation on these poles included. In this case $\mathcal{S}$ dropped from 1 to 0.97 proving the relatively less important role of this variation.

Extensive time-domain simulations were carried out to obtain the SNR_{peak} for a significant number of perturbated systems. Also all corner points of the variation space were added. In fig. 10 the peak SNR is plotted versus the input amplitude for the corner point $[\Delta_{IC} = 1; \Delta_\tau = 1]$. A single tone of frequency $\frac{f_s}{4OSR}$ is applied. An MSA of -2.5 dB was predicted. The time-domain simulations match very well with the analytical approach. The slight deviations in MSA or peak SNR are mainly due to the inaccuracy of the estimation of the maximum stable amplitude of equation (14) and some slight tonal behaviour of the quantisation noise.

B. Example 2: Robust after Coefficient Trimming

A general way to tackle the large parameter deviations is to introduce trimmable devices on chip. E.g. a switchable capacitor bank can be used to trim the integrator coefficients [1], [2]. We will now elaborate the situation with a very modest trimming accuracy resulting in RC variations of 5 %:

$$-0.05 \leq \delta_{IC} \leq 0.05 \quad , \quad -0.5 \leq \delta_\tau \leq 0.5 \qquad (24)$$

The same optimizations and time-domain simulations as for the previous case were performed and the resulting optimal modulator parameters are shown in table II. Due to the smaller variations, a real 3rd-order design was now found (with significant c_3). It is clear that the impact of trimming (even with this modest accuracy) is very large, as the guaranteed peak SNR has increased to 82 dB. Fig. 9 shows the perturbated NTFs. The higher SNR performance can immediately be identified by comparing the NTF in-band behaviour to the one of the non-trimmed example.

TABLE II
OPTIMAL COEFFICIENTS FOR EXAMPLE 2

c_1	c_2	c_3	g	d	SNR_{peak}	
					nominal	guaranteed
2.3017	0.4330	0.6555	0.0982	1.0398	83 dB	82 dB

Again time-domain simulations were performed which showed good agreement with the analytical approach. Also in this case, 20 % RC variation of the integrator poles had a negligible impact on the robustness as the resulting system was still robust against this extra variation ($\mathcal{S}$ still larger than 1).

C. Example 3: Adding Robustness to Clock Jitter

The approach can easily be extended to also take the effect of clock jitter into account. For this, we can keep the performance requirements (17)-(19), but for the calculation of the peak SNR we also take the in-band jitter noise into account according to equation (9). Suppose now that we want to design a modulator that is tolerant to a very high level of wideband clock jitter with an effective value $\sigma_{\Delta T_s}$ up to 1% of the clock period T_s. We keep the trimming condition of the previous example and hence use the same variations of equation (24). The optimal modulator parameters are summarized in table III. It is clear that a lot of performance is lost compared to the case without wideband jitter. The guaranteed peak SNR merely reaches a value of 61.4 dB.

TABLE III
OPTIMAL COEFFICIENTS FOR EXAMPLE 3

c_1	c_2	c_3	g	d	SNR_{peak}	
					nominal	guaranteed
0.8916	0.1831	0.5219	0.2720	0.0716	61.7 dB	61.4 dB

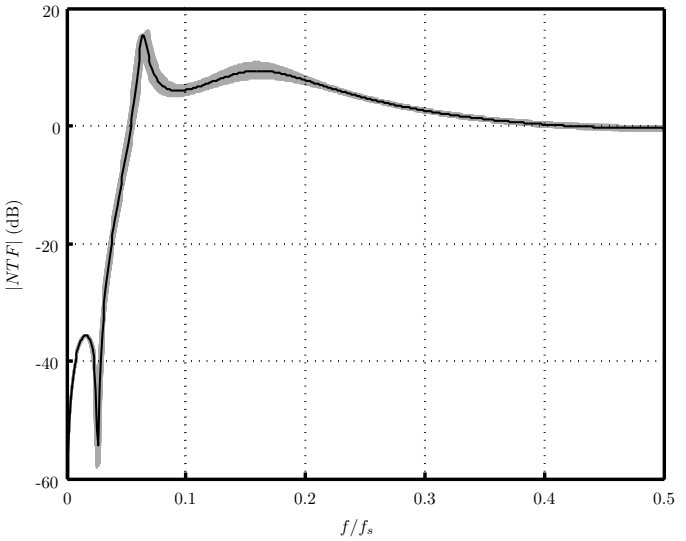

Fig. 11. NTF's with parameter variation influence for the 3rd-order optimal design with extra robustness to wideband clock jitter.

The resulting NTF's over all variations are plotted in fig. 11. Unlike the optimization result for the case without jitter, a low out-of-band gain is maintained over all variations (particularly near $f_s/2$). This is consistent with [11] where it was shown that this is indeed required for good clock jitter sensitivity.

D. Example 4: Controlling the STF

The previous examples all used the FF topology, which is more sensitive to out-of-band peaking of the STF. The control of the peaking behaviour to an acceptable level is important, as it allows relaxation of the ADC pre-filter. In this example we propose the modulator topology of fig. 12, which is also used in [1]. This hybrid feedforward/feedback topology compromises a trade-off between second-order anti-aliasing behaviour and reduced out-of-band peaking by introducing an extra feedback path. Again, we choose the FF/FB coefficients equal to 1 and thus perform a loop filter optimization. The parameter variations are taken from the example with modest coefficient trimming. The performance requirements (17)-(19) are now extended with an extra equation which limits the out-of-band STF peak to 2 dB:

$$\max_{\omega} |STF(j\omega)| < 2\,\text{dB} \tag{25}$$

For comparison, the previous 3 examples gave a worst-case STF out-of-band peak of 11, 18 and 17 dB respectively. The resulting optimal modulator parameters are given in table IV. Clearly, controlling the STF has to be paid for with a performance penalty. The guaranteed peak SNR was found to be 65 dB.

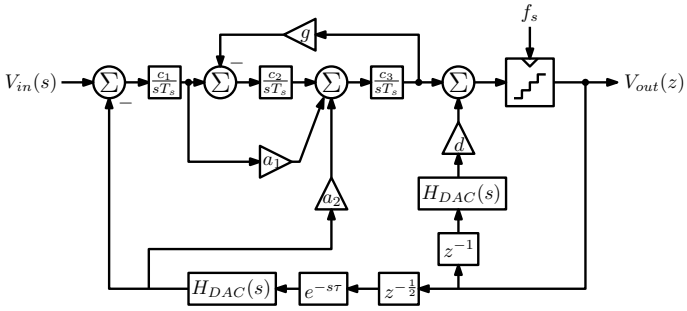

Fig. 12. Third-order CT $\Sigma\Delta$ modulator architecture with the loop filter in a hybrid feedforward/feedback (FF/FB) topology.

TABLE IV
OPTIMAL COEFFICIENTS FOR EXAMPLE 4

c_1	c_2	c_3	g	d	SNR_{peak}	
					nominal	guaranteed
0.4369	0.0114	2.0253	0.6706	1.1417	66.5 dB	65 dB

Fig. 13 shows the resulting STFs under influence of parameter variations. The STF has unity gain in the signal band. For higher frequencies the anti-aliasing performance has a second order profile dropping at 40 dB per decade. The out-of-band peaking is indeed limited to 2 dB as required.

VI. CONCLUSION

In this paper a new design strategy for robust design of continuous-time $\Sigma\Delta$ modulators has been presented. In the framework parasitic effects are included as variations on the system parameters. The goal of our approach is to find a modulator which maintains its performance (stability, guaranteed peak SNR, ...) over all the foreseen parasitic effects. For this purpose, we have introduced the $\mathcal{S}$-figure as a criterion for robustness. This way optimal robustness is achieved by optimizing the $\mathcal{S}$-figure. The approach has been used to find modulators that are robust to RC variations and parasitic excess loop delay. We also quantified the effect of coefficient trimming to enhance the modulator's performance. Even with a modest trim resolution of 5 %, the impact was found to be very significant. The approach has also been used to find robust modulators that are tolerant to extreme clock jitter. Also requirements on the signal-transfer-function can be included which allowed us to find modulators with controlled out-of-band peaking of the signal transfer function. The framework is very versatile and can easily be adopted to take various other parasitic effects into account.

VII. ACKNOWLEDGEMENT

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REFERENCES

[1] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani, "A 20-mW 640-MHz CMOS Continuous-Time $\Sigma\Delta$ ADC With 20-MHz Signal Bandwith, 80-dB Dynamic Range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2641–2649, 2006.

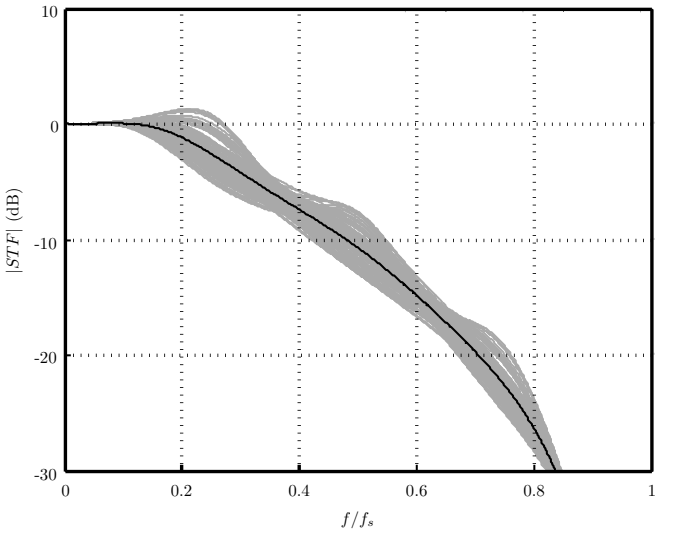

Fig. 13. STFs with parameter variation influence for the optimal hybrid 3rd-order with controlled STF behaviour.

[2] S. Yan and E. Sánchez-Sinencio, "A Continuous-Time ΣΔ Modulator With 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 75–86, 2004.

[3] E. J. van der Zwan, K. Philips, and C. A. A. Bastiaansen, "A 10.7-MHz IF-to-Baseband ΣΔ A/D Conversion System for AM/FM Radio Receivers," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1810–1819, 2000.

[4] J. A. Cherry and W. M. Snelgrove, "Excess Loop Delay in Continuous-Time Delta-Sigma Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 46, no. 4, pp. 376–389, 1999.

[5] J. De Maeyer, P. Rombouts, and L. Weyten, "Efficient Multibit Quantization in Continuous-Time ΣΔ Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 54, no. 4, pp. 757–767, Apr. 2007.

[6] R. Schreier, "An Empirical Study of High-Order Single-Bit Delta-Sigma Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 40, no. 8, pp. 461–466, 1993.

[7] J. G. Kenney and L. R. Carley, "Design of Multibit Noise-Shaping Data Converters," *Analog Integrated Circuits and Signal Processing*, vol. 3, no. 3, pp. 259–272, 1993.

[8] M. Keller, A. Buhmann, J. Sauerbrey, M. Ortmanns, and Y. Manoli, "A Comparative Study on Excess-Loop-Delay Compensation Techniques for Continuous-Time Sigma-Delta Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 55, no. 11, pp. 3480–3487, 2008.

[9] M. Ortmanns, F. Gerfers, and Y. Manoli, "Compensation of Finite Gain-Bandwidth Induced Errors in Continuous-Time ΣΔ Modulators," *IEEE Trans. Circuits Syst.-I*, vol. 51, no. 6, pp. 1088–1099, 2004.

[10] J. A. Cherry and W. M. Snelgrove, "Clock Jitter and Quantizer Metastability in Continuous-Time Delta-Sigma Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 46, no. 6, pp. 661–676, 1999.

[11] K. Reddy and S. Pavan, "Fundamental Limitations of Continuous-Time Delta-Sigma Modulators Due to Clock Jitter," *IEEE Trans. Circuits Syst.-I*, vol. 54, no. 10, pp. 2184–2193, 2007.

[12] B. De Vuyst, P. Rombouts, J. De Maeyer, and G. Gielen, "The Nyquist Criterion: A Useful Tool for the Robust Design of Continuous-Time ΣΔ Modulators," *IEEE Trans. Circuits Syst.-II*, vol. 57, no. 6, pp. 1–5, 2010.

[13] S. Pavan, "Systematic Design Centering of Continuous Time Oversampling Converters," *IEEE Trans. Circuits Syst.-II*, vol. 57, no. 3, pp. 158–162, Mar. 2010.

[14] E. Prefasi, L. Hernandez, S. Paton, A. Wiesbauer, R. Gaggl, and E. Pun, "A 0.1 mm^2, Wide Bandwith Continuous-Time ΣΔ ADC Based on a Time Encoding Quantizer in 0.13-μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2745–2754, 2009.

[15] K. J. Antreich, H. E. Graeb, and C. U. Wieser, "Circuit Analysis and Optimization Driven by Worst-Case Distances," *IEEE Trans. on Computer-Aided Design of Integrated Circuits Syst.*, vol. 13, no. 1, pp. 57–71, 1994.

[16] R. Storn and K. Price, "Differential evolution - A simple and efficient heuristic for global optimization over continuous spaces," *Journal of Global Optimization*, vol. 11, no. 4, pp. 341–359, 1997.