A Robust and Physical BSIM3 Non-Quasi-Static Transient and AC Small-Signal Model for Circuit Simulation

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***Abstract*— A new non-quasi-static (NQS) MOSFET model, which is applicable for both large-signal transient and small-signal ac analysis, has been developed. It employs a physical relaxation time approach to take care of the finite channel charging time to reach equilibrium and the effect of instantaneous channel charge re-distribution. The NQS model is formulated independently from the dc $I-V$ and the charge-capacitor model, thus can be easily applied to any existing simulators. The model has been implemented in the newly released BSIM3 version 3, and comparison has been made among this model, common quasi-static (QS) SPICE models and PISCES two-dimensional (2-D) numerical device simulator. While predicting accurate NQS behavior, the time penalty for using the new model is only about 20–30% more than the common QS models. It is much less than the time required by other NQS models reported. Limitations and compromises between simplicity, efficiency and accuracy are also discussed.**

I. Introduction

As MOSFET is becoming more performance-driven, it becomes essential to predict the circuit performance when it is operating near the device cut-off frequency. However, most models available in SPICE use the quasi-static (QS) formulation, which has been shown to be inadequate [1]–[4]. In the QS approach, the channel charge is assumed to achieve equilibrium once biases are applied, thus the finite charging time of the carriers in the inversion layer is ignored. This gives erroneous simulation results for signals with rise or fall time comparable to or smaller than the channel transit time. The most common QS model with 40/60 drain/source charge partition [1], for example, causes an unrealistic large drain current spike during fast turn on as shown in Fig. 1. Besides affecting the accuracy of the simulation, this nonphysical result can also cause oscillation and convergent problem during subsequent numerical iterations. It is common among circuit designers to bypass the convergent problem by using a 0/100 drain/source charge partitioning ratio [5], which attributes all transient charge to the source side. However, this ad-hoc nonphysical solution merely shifts the problem to the source as shown in Fig. 2, thus only work when the source is grounded.

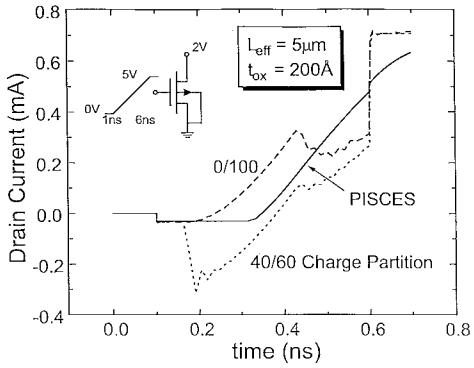

Fig. 1. NMOSFET drain current during turn-on transient simulated by different QS models and PISCES numerical simulator.

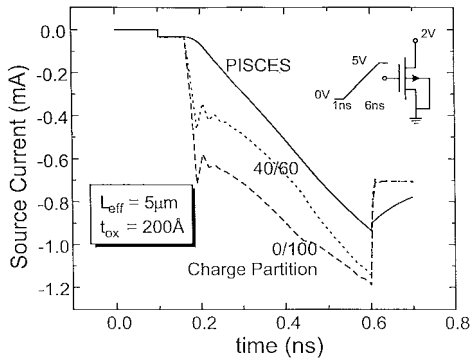

Fig. 2. NMOSFET source current during turn-on transient simulated by different QS models and PISCES numerical simulator.

Moreover, none of these QS models can be used to predict the high-frequency transadmittance of a MOSFET correctly as pointed out in [4]. The simulated current response when biasing a 200-μm-long MOSFET in strong inversion saturation appeared completely different from that of its equivalent circuit with two 100-μm-long MOSFET s in series as shown in Fig. 3. The equivalent circuit of breaking down a MOSFET into N equal parts in series (N-lumped model) has been used in high-frequency small-signal network due to the lack of non-quasi-static (NQS) models. The accuracy increases with N, at the expense of simulation time (of the order of $N^{1.4}$ times longer [6]). However, the method becomes impractical when the device channel length is scaled because artificial short-

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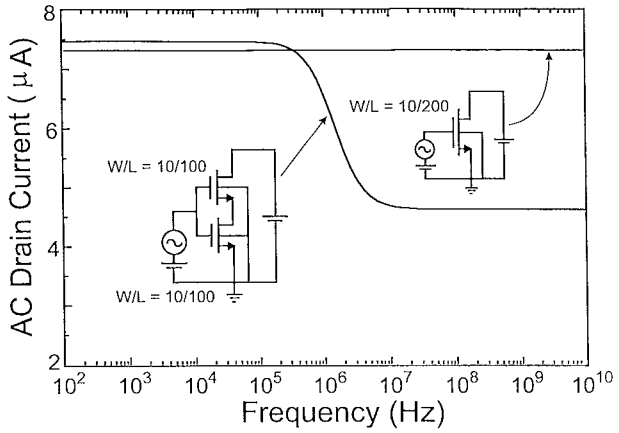


Fig. 3. AC drain current versus frequency for a 200-μm long MOSFET and an equivalent combination of two 100-μm long devices using an existing SPICE QS model.

channel effects in the sub-transistors may be activated. It should be noted that NQS behavior is not only confined to long channel transistors. It can be observed in short-channel devices as well, which has been experimentally demonstrated recently [7].

Some NQS models [8]–[10] have been published, but the complexity of the formulations prohibits intuitive insight into the NQS effect. These models usually require four to five times longer circuit simulation time than the common QS models, which makes them unattractive for simulating large circuits. Moreover, most of these models considered the transient and ac small-signal behavior separately, which can lead to inconsistent simulation results in the time domain and frequency domain.

In this work, we have developed a robust physical NQS model for both transient and ac small-signal analysis based on the channel charge relaxation approach. This NQS model is an attempt to compromise between accuracy, efficiency and easy adaptation to the popular approach of physical modeling and to avoid the necessity of solving complicated differential equations. A novel implementation strategy is employed to improve the efficiency as well as the flexibility for incorporating the NQS effect into other existing models. The NQS model has been implemented into the newly released BSIM3 version 3, and the results verified by PISCES. While providing significant improvement in accuracy to the existing QS models, the time penalty in using this new model is less than 30% for both transient and ac analysis.

II. Formulation

The channel of a MOSFET can be viewed as to a bias dependent RC distributed transmission line [11] as shown in Fig. 4(a). In the QS approach, the gate capacitors are lumped to the external source and drain nodes as in Fig. 4(b), thereby ignoring the finite delay time required for channel charge build-up. Breaking down the transistor into N smaller ones connected in series [Fig. 4(c)] gives a better approximation to the RC network but it has the drawbacks mentioned in previous section. A physical approach to model the NQS effect, would be to formulate an estimate for the delay time through the channel RC network and incorporate this time constant into the model equations.

One of the widely used methods to approximate the RC delay was proposed by Elmore [12], [13], by using the mean, or first moment, of the impulse response. Utilizing Elmore's approach, the RC distributed channel can be approximated by a simple RC equivalent, which retains the lowest frequency pole of the original RC network. The new equivalent circuit is shown in Fig. 4(d). The Elmore resistance $(R_{\rm Elmore})$ in strong inversion can be calculated from the total channel resistance, which is given by

$$R_{\rm Elmore} = \frac{L_{\rm eff}}{\varepsilon \mu_{\rm eff} W_{\rm eff} Q_{\rm ch}} \tag{1}$$

where $Q_{\rm ch}$ is the instantaneous channel inversion charge and ε is the Elmore constant to match the lowest frequency pole. The value of ε is found to be around 3 by matching the output of the equivalent circuit in Fig. 4(a) and (d), and it is invariant with respect to W and L**.** The time domain and frequency domain response of the Elmore equivalent approximation [Fig. 4(d)] and the original device with RC distributed channel [Fig. 4(a)] are compared and shown in Figs. 5 and 6, respectively. In the first case, a fast pulse is applied to the gate with both source and drain grounded and the gate current is measured. In the second case, a small-signal voltage is applied to the gate and the voltage fluctuation caused by the excitation is measured at different part of the channel. In both cases, a very good match between the RC Elmore equivalent circuit and the real distributed RC network are observed. However, in the actual BSIM3 implementation, ε is chosen to be 5 and the reasons will be given in the discussion section. For subsequent simulations, ε will assume the value of 5.

Direct implementation of the model shown in Fig. 4(d) is straight forward, but requires the creation of two additional nodes. This will increase the time to solve the Jacobian Matrix in SPICE by more than 70%. The need to change the device topology also requires modifications to the existing model equations, which is undesirable as well. A simpler way to incorporate the newly formulated NQS model will be employed to provide better robustness, flexibility and extensibility.

To simplify the model implementation, some of the current equations are reviewed. The transient node currents to the gate, drain, and source can be described by the equation

$$I_{G,D,S}(t) = I_{G,D,S}(t)|_{\rm DC} + X_{G,D,S}\frac{dQ_{\rm ch}(t)}{dt} \tag{2}$$

where $I_{G,D,S}(t)$ are the gate, drain or source current, $I_{G,D,S}(t)|_{\rm DC}$ are the gate, drain, or source current under dc condition. $Q_{\rm ch}(t)$ is the actual channel charge at given time t, and $X_{G,D,S}$ is the channel charge partition ratio [14], [15] to the gate, drain and source with

$$X_D + X_S = X_{=}1 \tag{3}$$

If the geometrical factor is taken into consideration, X_D varies from 0.5 at $V_D = 0$ V to 0.4 in the saturation region, and X_S varies from 0.5 to 0.6, respectively [1]. As the 0.4/0.6 partition covered larger voltage operation range and the error introduced

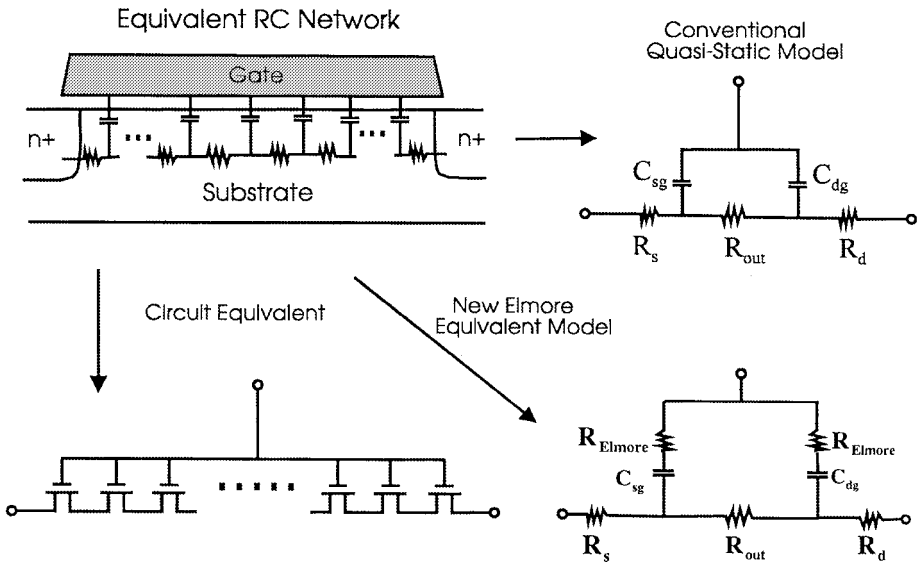


Fig. 4. Different possible equivalent transient and ac small-signal models for a MOS transistor.

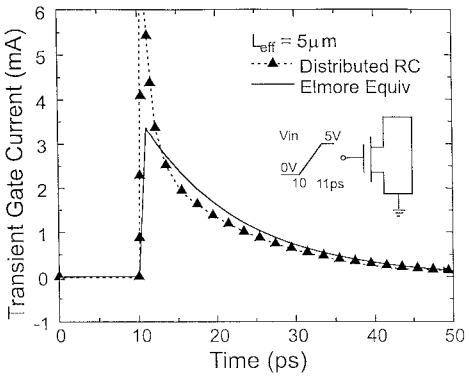


Fig. 5. Verification of the Elmore equivalent circuit in the time domain, indicating it is a good first order approximation to the RC network.

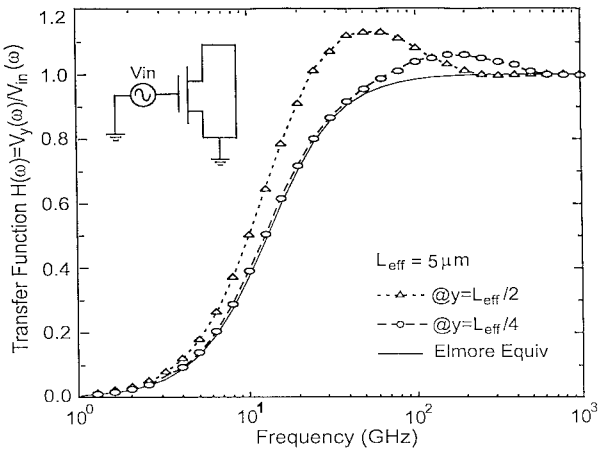


Fig. 6. Verification of the Elmore equivalent circuit in the frequency domain, showing a good agreement is attained between the Elmore equivalent circuit and the distributed RC network.

by taking a constant $X_D = 0.4$ and $X_S = 0.6$ is less than 5% in the worst case, these values will be adopted to simplify the model.

In the QS approach, it is assumed that

$$\frac{dQ_{\rm ch}(t)}{dt} = \frac{dQ_{\rm cheq}(t)}{dt} = \frac{dQ_{\rm cheq}}{dV}\,\frac{dV}{dt} \tag{4}$$

where $Q_{\rm cheq}(t)$ is the equilibrium channel charge under the biases at time t. The assumption of equilibrium at all time gives rise to error in calculating the NQS currents. To account for the NQS effect, a new state variable Qdef has been introduced to keep track of the amount of deficit (or surplus) channel charge necessary to achieve equilibrium at a given time where

$$Q_{\rm def}(t) = |Q_{\rm cheq}(t) - Q_{\rm ch}(t) \tag{5}$$

and

$$\frac{dQ_{\rm def}(t)}{dt} = \frac{dQ_{\rm cheq}(t)}{dt} - \frac{dQ_{\rm ch}(t)}{dt} \tag{6}$$

$Q_{\rm def}$ is allowed to decay exponentially into the channel with a bias dependent NQS relaxation time τ, which represents the delay due to the RC distributed network in the channel. Thus the charging current can be approximated by

$$\frac{dQ_{\rm ch}(t)}{dt} \approx \frac{Q_{\rm def}(t)}{\tau}. \tag{7}$$

Substituting (7) into (6) we get

$$\frac{dQ_{\rm def}(t)}{dt} = \frac{dQ_{\rm cheq}(t)}{dt} - \frac{Q_{\rm def}(t)}{\tau}. \tag{8}$$

$Q_{\rm def}(t)$ can be calculated from (8) with a subcircuit as shown in Fig. 7, which is a direct translation of (8) into basic circuit elements. The node voltage of the subcircuit gives the value of $Q_{\rm def}(t)$, and the branch current flowing through the resistor with value τ gives the total charging NQS currents. This charging current is then partitioned to the gate, drain and source with the corresponding charge partition ratios. With this approach, only one addition node is required and the topology of the original transistor is preserved.

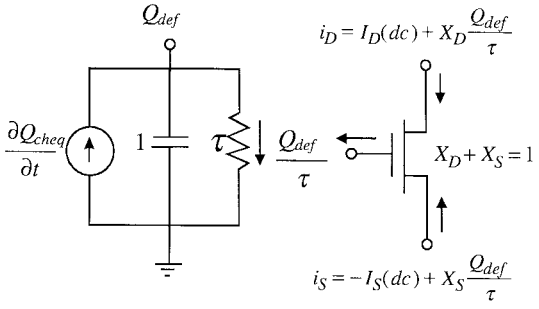


Fig. 7. BSIM3 implementation of the new model. A subcircuit is constructed to evaluate $Q_{\rm def}$ and additional NQS currents calculated by the subcircuit are superimposed to the MOSFET.

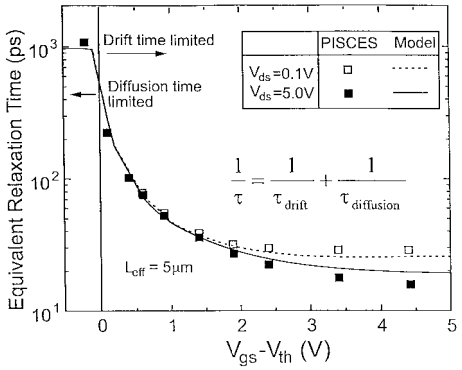


Fig. 8. Comparison between the relaxation time constant (τ) used in the new model and the value obtained from PISCES simulation.

The value of the channel relaxation time constant τ is composed of the diffusion component which dominated in the subthreshold region and by the drift component (calculated from the RC Elmore equivalent discussed at the beginning of this section) dominated in the strong inversion region. Various components of τ are given by

$$\tau_{\rm diffusion} = \frac{q(L_{\rm eff}/4)^2}{\mu_{\rm eff} kT} \tag{9}$$

$$\begin{aligned}\tau_{\rm drift} &\approx 0.5(C_{SG}+C_{SG})W_{\rm eff}L_{\rm eff}R_{\rm Elmore} \\ &= \frac{(C_{SG}+C_{DG})L_{\rm eff}}{2\varepsilon\mu_{\rm eff}(Q_{\rm cheq}-Q_{\rm def})} \\ &\approx \frac{C_{\rm ox}L_{\rm eff}}{2\varepsilon\mu_{\rm eff}Q_{\rm cheq}} \quad \text{and} \end{aligned} \tag{10}$$

$$\frac{1}{\tau} = \frac{1}{\tau_{\rm diffusion}} + \frac{1}{\tau_{\rm drift}}. \tag{11}$$

In the $\tau_{\rm drift}$ term, C_{SG} and C_{DG} are the source-to-gate and drain-to-gate capacitance respectively as in Fig. 4(d). Due to the complexity of calculating the derivatives of the capacitances, the total capacitance $(C_{SG}+C_{DG})$ is approximated by $C_{\rm ox}$. Actual value of $(C_{SG}+C_{DG})$ varies between $C_{\rm ox}$ for small V_D and $0.75C_{\rm ox}$ for $V_D > V_{D\rm sat}$ [16]. The error due to this approximation will be discussed in the discussion section. Also in (10), the instantaneous channel charge $(Q_{\rm ch})$ is approximated by the equilibrium inversion charge $(Q_{\rm cheq})$ to simplify the calculations. The validity of this approximation has been verified for rise time slower than ten times the cutoff frequency (f_T) of the device and is sufficient for most of the practical circuits. Fig. 8 compared the value τ used in the new model with result obtained from PISCES simulation by applying a small step input at the gate and observing the decay time of the gate current. The comparison shows that the model agrees reasonably well with the two-dimensional (2-D) simulator despite the approximations made.

III. Simulation Results

The new model has been implemented in the BSIM3 version 3 release [17]. A number of benchmark simulations have been performed and the results verified by PISCES 2-D device simulator. Fig. 9 shows the simulated turn-on and turn-off transients in the linear region (small V_D). Good agreement between the new model and PISCES is observed in both cases. The small discrepancy at the beginning of the turn-on is mainly due to the inaccuracy of the dc model around the threshold voltage rather than the NQS model. The simulation result in the saturation region (high V_D) is shown in Fig. 10. Despite some minor errors at the on-set of the transient (will be discussed in the next section), the model describes the NQS behavior with very high accuracy.

TABLE I
Time Required for Simulating the DAC Cell by Different Models. The Time Penalty for Using the NQS Model is About 30%

	DC	0/100	40/60	New
Total time (sec)	1.777	1.863	1.906	2.243
# of iteration	732	729	781	848
# of time pt.	173	186	187	252
accepted time pt.	121	124	127	186

Fig. 11 shows the result of the high-frequency transadmittance test suggested in [4], where the real part of the transadmittance is plotted against the frequency of operation. The discrepancy caused by the QS models in simulating a single transistor and its N-lumped equivalent has been resolved by the new NQS model. The NQS model and the N-lumped model both predict the transadmittance to fall off around the same frequency. It is also observed that simulation results obtained from the N-lumped model go asymptotically to those obtained from the NQS model as N increases. Similar results are also observed in the amplitude and phase plots of a simple resistive load inverter as shown in Fig. 12.

As a practical example to illustrate the importance of the NQS effect in circuit design, a low-voltage, high-speed current output Digital/Analog converter (DAC) cell [18] as shown in Fig. 13 was simulated. In this circuit, $M1$ and $M1b$ operate as current sources when turned on, and an output current appears as $I_{\rm out}$ or $I_{\rm dump}$. To obtain high output resistance, $M1$ must be greater than the minimum length (9.6 μm was used). Current switching was limited by the speed of the switching of the voltage at node 1. Fig. 14 shows a simulation using standard QS models and the new NQS model. The new model indicates slower rise and settling times, limited by NQS effect in the long channel of $M1$. It illustrates an intrinsic limitation to the speed of this DAC circuit, which is not apparent with the QS models. Table I compares the time required to simulate the

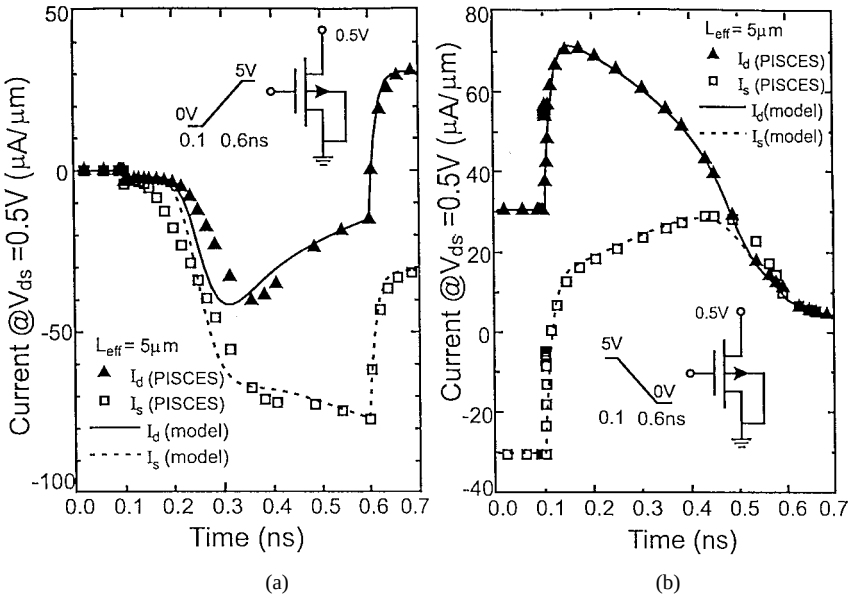


Fig. 9. Simulated $I-V$ characteristics in the linear region (low V_D). Excellent match between the model and PISCES is observed.

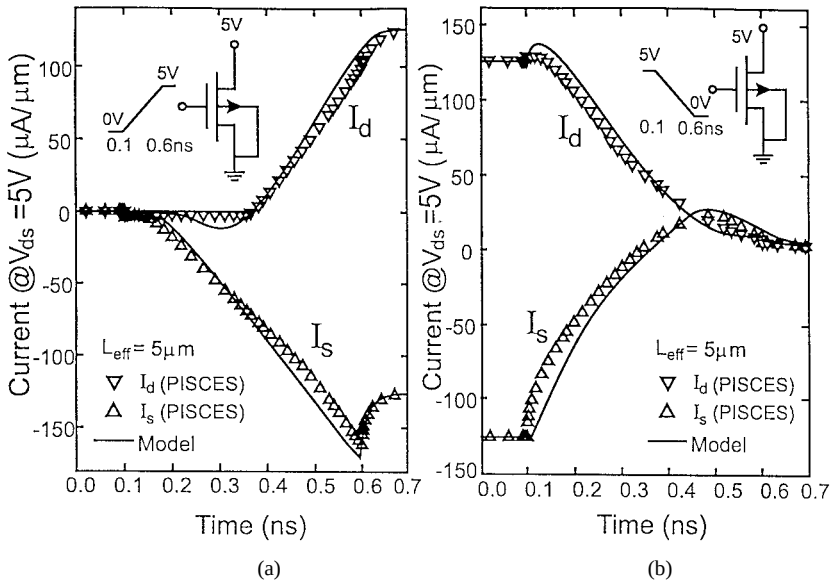


Fig. 10. Simulated $I-V$ characteristics in the saturation region (high V_D). Very good agreement between the model and PISCES is observed.

DAC cell using different models. The overall simulation time penalty introduced by the new NQS model is less than 30%.

IV. Discussion and Limitation of the Model

In this version of the NQS model, we intend to provide a practical and efficient solution, which can be easily implemented in existing simulators. A lot of compromise has been made between simulation efficiency, complexity and accuracy. A number of physical effects have been ignored, such as the body current. It has little effect on the ac simulation, but can lead to error during transient simulation. The body current can be included by partitioning the gate current from $Q_{\rm def}$ between the gate and the body. As the body current is usually small compared to the gate current as shown in Fig. 15, and the robustness of the model takes higher priority, we chose to leave it aside. Nevertheless, the new NQS model has been shown to provide substantial improvement over existing BSIM3 charge models even without the substrate current.

Another limitation for the model is the oversight of the saturation region operation during the formulation. The derivation of $\tau_{\rm drift}$ in (10) is based on operation in the linear region, thus no velocity saturation is considered. When a MOSFET is operated in the velocity saturation regime, the channel conductivity reduces and the value of $R_{\rm Elmore}$ increases. However, this increase is partially compensated by the decrease in the term $(C_{SG}+C_{DG})$ from $C_{\rm ox}W_{\rm eff}L_{\rm eff}$ to about $0.75C_{\rm ox}W_{\rm eff}L_{\rm eff}$ [16] due to nonuniform channel charge

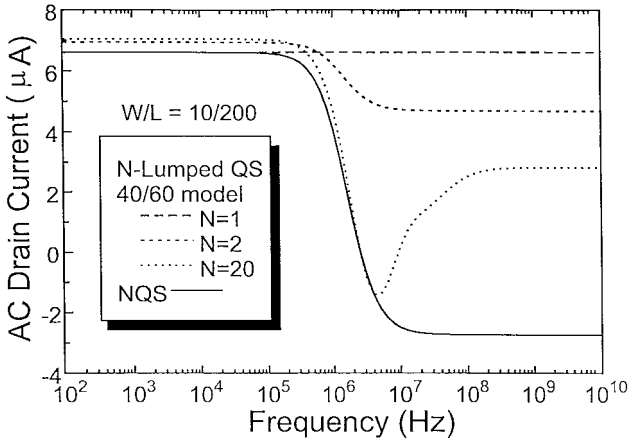
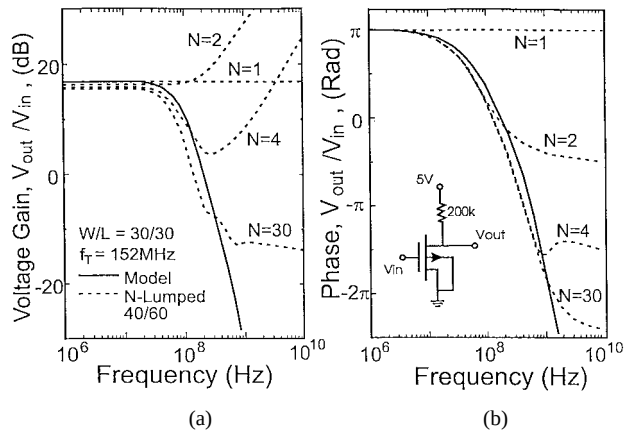


Fig. 11. Result of high-frequency transadmittance test. The NQS model is capable of predicting the transadmittance fall-off at high frequency, which agrees with the N-lumped model. The result from the N-lumped model follows asymptotically to the rest from the NQS model as N increases.



(a) (b)

Fig. 12. Frequency response of a NMOS inverter with a resistive load simulated using the new NQS model and the N-lumped model. The result from the N-lumped model follows asymptotically to the result from the NQS model as N increases.

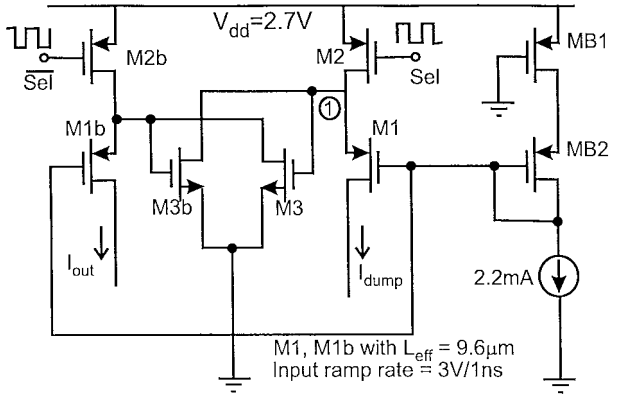


Fig. 13. A low-voltage, high-speed current output Digital/Analog Converter (DAC) cell simulated by existing QS models and the new NQS model.

distribution as V_D increases from 0 V to $V_{D\mathrm{sat}}$. The resulting τ_{drift} increases slightly by about 30% as shown in Fig. 16. The worst case error in node currents when the device is operated in the velocity saturation region is thus less than 20%. This error can be reduced to less than 10% by choosing

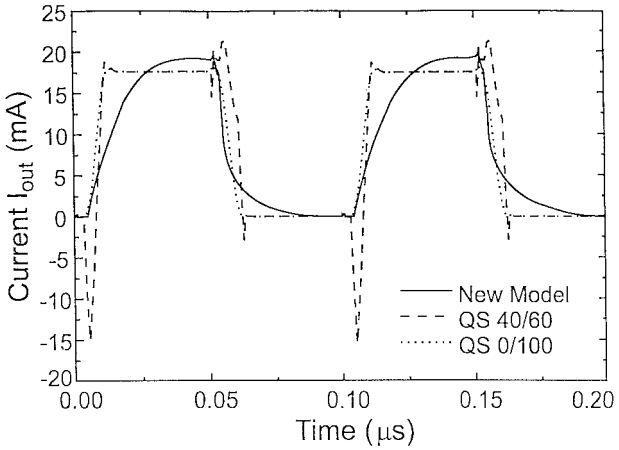


Fig. 14. Simulated current output (I_{out}) of the DAC cell by different models. The NQS model predicted a longer settling time compared with the QS models.

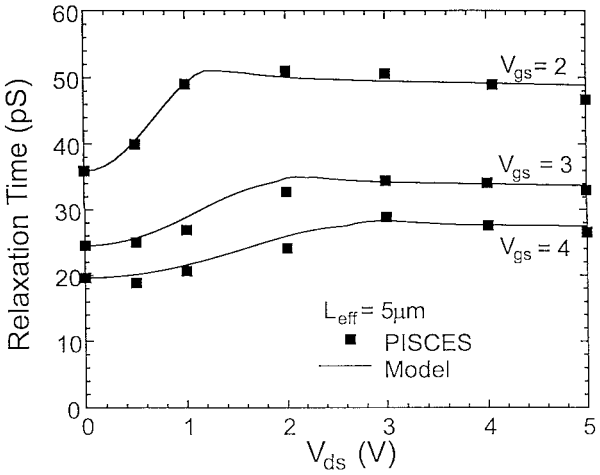


Fig. 15. Relaxation time constant as a function of drain bias with the effect of velocity saturation included. Empirical fit given by (12) is superimposed for comparison.

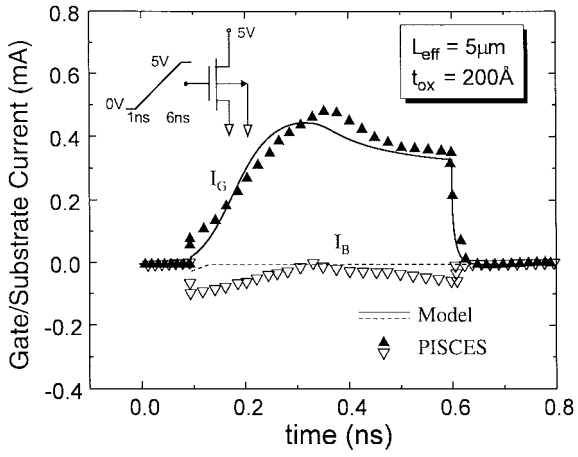


Fig. 16. Simulated gate current and substrate current and the comparison with PISCES result.

a compromising Elmore constant (ε) between the linear region and the saturation. Due to this reason, the default ε in the BSIM3 model is chosen to be five instead of three calculated

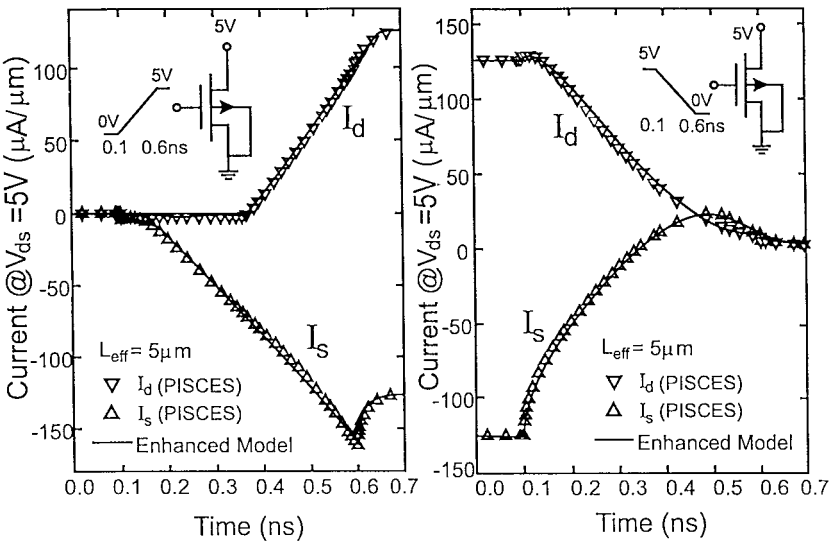


Fig. 17. Simulated $I-V$ characteristics in the saturation region (high V_D) after the enhancement equations are included. Significant improvement to the accuracy of the new model is observed.

in the linear region. When a more accurate result is desired, the drift component of the relaxation time given in (10) can be replaced by the following empirical model

$$\tau_{\rm drift} = \begin{cases} \dfrac{(C_{SG}+C_{DG})L_{\rm eff}\left(1+\left(\dfrac{V_{ds}}{V_{d\rm sat}}\right)^2\right)}{2\varepsilon\mu_{\rm eff}(Q_{\rm eqch}-Q_{\rm def})} & \text{for } V_{DS} \le V_{D\rm sat} \\ \dfrac{(C_{SG}+C_{DG})L_{\rm eff}}{\varepsilon\mu_{\rm eff}(Q_{\rm eqch}-Q_{\rm def})} & \text{for } V_{DS} > V_{D\rm sat} \end{cases}. \quad (12)$$

Comparison between the empirical model and PISCES is shown in Fig. 15 indicating a very good agreement between them. But this model has been left out again for simplicity reasons.

The effects of high-channel electric field in the velocity saturation region deserve further consideration. At high drain voltage, high electric field is developed near the drain/channel junction. This electric field prevents the carriers to flow into the channel from the drain side during fast turn-on. In this case, all the channel charge will be provided by the source, and the drain current cannot go negative for NMOSFET (vice versa for PMOSFET) as in Fig. 10(a). Note that it is only true for velocity saturation region, and the drain current can actually go negative in the linear region as in Fig. 9. This effect can be taken care simply by restricting the drain current to be positive when the drain voltage is larger than the saturation drain voltage. That is

$$I_d \ge 0 \quad \text{for} \quad V_D \ge V_{D\rm sat}. \quad (13)$$

During turn-off transient, another restriction has to be imposed due to the fact that the maximum drain current is limited by the number of the carriers controlled by the drain and the maximum speed they can move. Therefore, the maximum current must satisfy

$$I_D \le W_{\rm eff} v_{\rm sat}(Q_{\rm cheq} - X_D Q_{\rm def}). \quad (14)$$

After including the enhancements given by (12)–(14) in the model, simulation has been performed with high V_D. The results of the simulation are shown in Fig. 16, which show a nearly perfect fit. The improvement after adding the enhancement is more obvious after comparing Figs. 17 and 10. However, with the restrictions added, the nice continuous properties in the BSIM3 formulation cannot be preserved and leading to slower convergence as in some older models. Due to this consideration, the restriction is not imposed in the release. Nevertheless, the small negative current, which appears in extremely fast ramping, only shows up as a small overshoot in most simulation. The implemented model is able to predict the delay time and the frequency fall off with very high accuracy in the present form.

V. Conclusion

Based on the relaxation time approach, a NQS MOSFET model, valid in both fast transient and ac small-signal analysis, has been developed and implemented in BSIM3 version 3. The formulation is independent of any particular $I-V$ or C-V model, and can be implemented with any existing MOS models. Most of the parameters required by the new model can be deduced from the existing dc and charge model, and thus no new parameter extraction scheme is necessary. Extensive simulation has been performed with the new model and results verified by PISCES. The time penalty for using the new model is less than 30%, mainly due to an additional node and more time points are required for convergence during transient simulation. Limitations and enhancements to include the effects such as substrate current and velocity saturation

are also discussed. Excellent agreement between PISCES and the new model is achieved over a wide range of biases and physical dimensions.

REFERENCES

[1] S. Y. Oh, D. E. Ward, and R. W. Dutton, "Transient analysis of MOS transistors," *IEEE J. Solid-State Circuits*, vol. SC-15, no. 4, pp. 636–643, 1980

[2] Y. P. Tsividis and G. Masetti, "Problems in the precision modeling of the MOS transistor for analog applications," *IEEE Trans. Computer-Aided Des.*, vol. CAD-3, pp. 72–79, Jan. 1984.

[3] J. J. Paulous and D. A. Antoniadis, "Limitations of quasistatic capacitance models for the MOS transistors," *IEEE Electron Device Lett.*, vol. EDL-4, pp. 221–224, 1983

[4] Y. P. Tsividis and K. Suyama, "MOSFET modeling for analog circuit CAD: problems and prospects," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 3, pp. 210–216, Mar. 1994.

[5] P. Yang and P. K. Chatterjee, "SPICE modeling for small geometry MOSFET circuits," *IEEE Trans. Computer-Aided Design*, vol. CAD-1, pp. 169–182, Oct. 1982.

[6] T. L. Quarles, "SPICE 3 Implementation Guide," Memo. no. UCB/ERL M89/42, Apr. 1989.

[7] R. Singh, A. Juge, R. Joly, and G. Morin, "An investigation into the nonquasistatic effects in MOS devices with an wafer S-parameter techniques," *Proc. IEEE Int. Conf. Microelectron Test Structures*, Barcelona, Mar. 1993.

[8] C. Turchetti, P. Mancini, and G. Masetti, "A CAD-orianted nonquasi-static approach for the transient analysis of MOS IC's," *IEEE Journal of Solid-State Circuits*, vol. SC-21, no. 5, pp. 827–836, 1986

[9] M. Bagheri, and Y. Tsividis, "A small-signal dc-to-high-frequency nonquasi-static model for the four-terminal MOSFET valid in all regions of operation," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 2383–2391, Nov. 1985.

[10] H. J. Park, P. K. Ko, and C. Hu, "A charge-conserving nonquasi-static MOSFET model for SPICE transient analysis," in *IEDM Tech. Dig.*, 1987, pp. 652–655.

[11] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987.

[12] W. C. Elmore, "The transient response of damped linear networks with particular regard to wideband amplifiers," *J. Appl. Phys.*, vol. 19, no. 1, pp. 55–63, 1948.

[13] L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. Computer-Aided Design*, vol. 9, pp. 352–366, Apr. 1990.

[14] J. G. Fossum, H. Jeong, and S. Veeraraghavan, "Significance of the channel-charge partition in the transient MOSFET model," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 1621–1623, Oct. 1986.

[15] M. F. Sevat, "On the channel charge division in MOSFET modeling," *ICCAD Tech. Dig.*, Nov. 1987, pp. 208–210

[16] B. J. Sheu, P. K. Ko, "Measurement and modeling of short-channel MOS transistor gate capacitances," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 3, pp. 464–472, June 1987.

[17] Y.-H. Cheng, M. Chan, K. Chen, J. Chen, J. H. Huang, Z. H. Liu, M. C. Jeng, K. Hui, P. K. Ko, and C. Hu, "BSIM3 version 3.0 manual," July 1995, Univ. California, Berkeley.

[18] T. Miki, Y. Nakamura, Y. Nishikawa, K. Okada, and Y. Horiba, "A 10 bit 50 MS/s CMOS D/A Converter with 2.7 V power supply," *1992 Symp. VLSI Circuits Dig. Tech. Papers*, 1992, pp. 92–93.

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Mansun Chan (S'92–M'95), for a photograph and biography, see p. 212 of the January 1998 issue of this TRANSACTIONS.

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