A SAW-Less GSM/GPRS/EDGE Receiver Embedded in 65-nm SoC

Chi-Yao Yu, *Member, IEEE*, Ivan Siu-Chuang Lu, *Member, IEEE*, Yen-Horng Chen, Lan-Chou Cho, Chih-Hao Eric Sun, Chih-Chun Tang, Hsiang-Hui Chang, Wen-Chang Lee, *Member, IEEE*, Sheng-Jui Huang, Tzung-Han Wu, *Member, IEEE*, Chinq-Shiun Chiu, and George Chien, *Senior Member, IEEE*

***Abstract*—A quad-band GSM/GPRS/EDGE receiver, implemented in 65 nm CMOS, complies with the ETSI standard without the need of external SAW filters. By exploring the properties of passive mixers and current-mode operation from RF to baseband, the receiver can achieve a SAW-filter-like selectivity with inexpensive on-chip components such as resistors and capacitors. In addition, to alleviate the linearity bottleneck at the LNA input stage, Class-AB self-bias LNTA is employed to break the conventional trade-off's among NF, linearity and power consumption. For single-to-differential conversion, external LC-CL baluns (instead of on-chip baluns) are used to balance the on-chip die and external BOM cost. This receiver solution is embedded as a part of a cellular phone SoC and achieves < -110 dBm sensitivity, $> +1$ dBm Out-of-Band $P_{1\,dB}$ and consumes 58.9 mA. In FTA test, the receiver passes out-of-band blocker test with > 4 dB margin.**

***Index Terms*—Blocker detection, class-AB, current-mode, dynamic range, GSM, impedance transformation, receiver, SAW-less.**

I. Introduction

OVER the last decade, demands of mobile communication have seen an explosive growth where the coverage of second-generation (2G) mobile communication standard such as GSM has reached $>$ 1.5 billion people across more than 212 countries [1]. Many of these are emerging countries where the convenience of wireless communication can greatly enrich people's lives in different ways. To realize this, significant efforts have been made towards increasing integration and reducing the bill of material (BOM) for mobile devices, which in turn reduce costs of ownership.

In recent years, an increasing number of radios with CMOS implementation and high level of integration (e.g., single-chip phone) [2] have been introduced in the market. To meet the GSM standard, external filters are generally used to filter blocker or interference signals in receivers (RX) and to reduce noise in the RX band of transmitters (TX). With innovative TX architectures and circuits, external transmit filters have largely been eliminated [3], while receive filters are still present. Due to the stringent filtering requirements, these RX filters are generally made with surface acoustic wave (SAW) technology. Not only do these filters reduce the RX sensitivity due to filter insertion loss, but they make up a big part of the external BOM cost for the wireless system. Therefore, for high-volume application, significant cost savings offered by a SAW-filter-less solution is a genuine advantage and a key product differentiator.

In wireless radios, the received spectrum typically consists of a weak desired signal accompanied by interferers that can be much stronger in power at various offset frequencies. For conventional quad-band GSM RXs, the received signal passes through the antenna switch module (ASM), followed by four external SAW filters before entering the four on-chip low noise amplifiers (LNAs), as shown in Fig. 1(a). These filters reject strong out-of-band (OOB) blockers to minimize their negative effects on the RXs. As the name suggests, SAW-less RX eliminates the need for SAW filters and improves the RX sensitivity. In addition, as shown in Fig. 1(b), only two baluns and two on-chip LNAs are required due to the close proximity of the GSM frequencies. By removing the SAW filter and having a smaller ASM with only two RX ports, the external BOM required for a GSM phone can be reduced by up to 50%. This is of great importance for a high-volume, low-cost market like the 2G cellular phone market today.

In this paper, Section II introduces the GSM specifications and the unique design challenges for a SAW-less receiver. Sections III–V describe the techniques and circuit implementations which break the conventional wisdom of RX design, namely, noise, linearity, and power consumption trade-offs. Measurement results are included in Section VI, while Section VII concludes the paper.

II. GSM SAW-Less Receiver Design Challenges

A. GSM Specifications

Fig. 2 shows the GSM900/PCS receive spectrums defined in the GSM specifications. In addition to the adjacent channel interference signals within the GSM bands, it also requires a radio to successfully receive a desired signal at -99 dBm while withstanding a 0-dBm continuous wave (CW) blocker signal at 20 MHz away for 850/900 bands or 80 MHz away for DCS/PCS bands. A typical SAW filter provides at least 20-dB rejection at 20-MHz offset, which attenuates the 0-dBm blocker to roughly the same level as the 3-MHz adjacent channel interference (ACI). Without the protection of the SAW

Manuscript received April 13, 2011; revised July 31, 2011; accepted August 06, 2011. Date of publication October 06, 2011; date of current version November 23, 2011. This paper was approved by Guest Editor Yorgos Palaskas.

C.-Y. Yu, L.-C. Cho, C.-H. E. Sun, C.-C. Tang, H.-H. Chang, T.-H. Wu, and C.-S. Chiu are with MediaTek Inc., Hsinchu, Taiwan 30078 (e-mail: chiyao.yu@mediatek.com; lanchou.cho@mediatek.com; chao.sun@mediatek.com; cc.tang@mediatek.com; hh.chang@mediatek.com; amos.wu@mediatek.com; cs.chiu@mediatek.com).

I. S.-C. Lu and G. Chien are with MediaTek USA Inc., San Jose, CA 95134 USA (e-mail: Ivan.lu@ mediatek.com; george.chien@mediatek.com).

Y.-H. Chen and W.-C. Lee are with MediaTek Inc., Austin, TX 78730 USA (e-mail: yenhorng.chen@mediatek.com; charles.lee@mediatek.com).

S.-J. Huang is with MediaTek Inc., Woburn, MA 01801-1130 USA (e-mail: analogbb.huang@mediatek.com).

Digital Object Identifier 10.1109/JSSC.2011.2166657

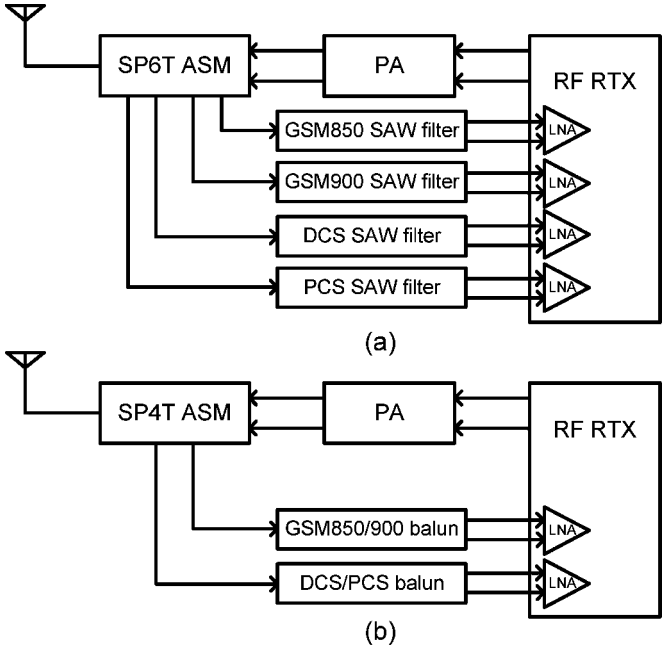


Fig. 1. (a) Conventional SAW-based receiver front-end. (b) SAW-less receiver front-end.

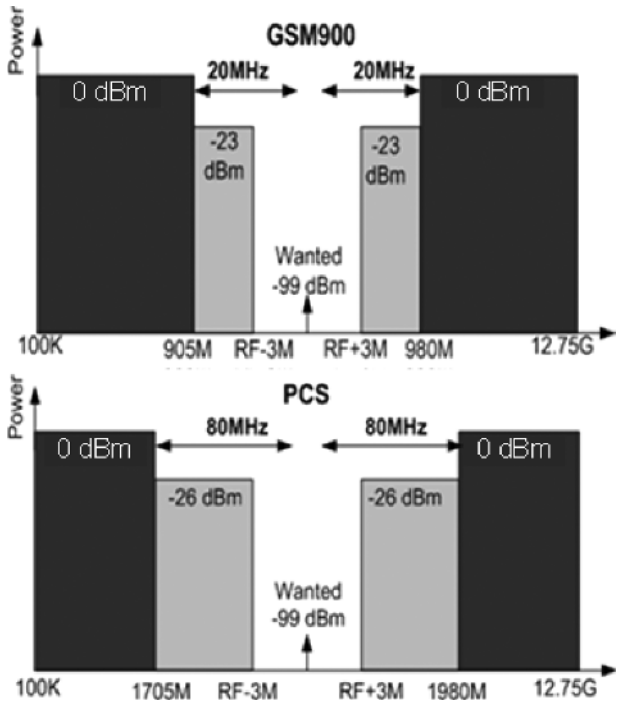


Fig. 2. PCS/GSM900 receive spectrums defined in the GSM specification.

filter, conventional RX will suffer severe signal desensitization and blocker induced noise that would not normally be there.

B. Dynamic Range Versus Power Versus Noise

In a SAW-less RX, the 0-dBm OOB blocking signal must be received simultaneously with −99 dBm desired signal. The required SNR to properly demodulate the GSM signal is around 6 dB; this translates to $>$ 100–dB dynamic range required for the RX. To overcome the linearity limitation due to the 0-dBm blocker, a highly selective frequency down-conversion interface is introduced. By employing passive mixers followed by a current-mode low-pass filter, this technique creates a low impedance node at the low-noise transconductance amplifier (LNTA) output at the blocker frequency to reduce the voltage swing and effectively filters the blocker energy before entering the transimpedance amplifier (TIA). It successfully removes linearity bottlenecks at the LNTA output and TIA input in conventional RX. A detailed analysis can be found in Section III.

While linearity bottlenecks in other parts of the RX have been removed, the LNTA still needs to process the 0-dBm blocker signal as it enters the RX input. With the matching gain, the single-ended blocker swing at LNTA input ports can reach 1 $\mathrm{V_{pp}}$. To keep the LNTA g_m linear over such a large input range, a Class-AB adaptive bias is introduced. This LNTA, under typical condition, functions like a normal transconductance amplifier. When blocker signal power increases beyond −15 dBm, the Class-AB adaptive bias action starts to provide a gain boosting effect to increase the $\mathrm{P_{1\ dB}}$ compression point. In turn, this improves the overall RX dynamic range and keeps the power consumption low under normal conditions. Detailed discussion can be found in Section IV.

C. Reciprocal Mixing

In any RX, the received desired signal is mixed by the LO spectrum and down-converted to baseband frequency for further signal processing. In the same way, the adjacent channel signal in the received spectrum is also mixed by LO phase noise (PN) and down-converted to the same baseband frequency; this degrades the SNR of the RX. The PN requirement of the LO signal is given by

$$PN_{\max}\left(\frac{\mathrm{dBc}}{\mathrm{Hz}}\right) \leq -(P_{\mathrm{block}} - P_{\mathrm{signal}}) - 10\log(BW_{\mathrm{signal}}) - \mathrm{SNR}. \quad (1)$$

Based on (1), for a GSM SAW-less RX with 0 dBm blocker at 20 MHz offset, −99 dBm signal, 200-kHz signal bandwidth, and 6-dB SNR, the maximum LO PN at 20-MHz offset is −158 dBc/Hz. To minimize the PN contribution to the overall RX noise floor, the actual LO PN target is set at −163 dBc/Hz. This value is around 20 dB tougher compared with a conventional RX where the 0-dBm OOB blockers have been rejected by the SAW filter. In addition, spurs present in the LO spectrum can inadvertently down-convert the blocker and further degrades the SNR.

In summary, to implement a SAW-less RX successfully, the receive signal path needs to have $>$ 100 dB dynamic range, low noise, and low power; and the LO signal also needs to be extremely pure with low PN and low spurs.

III. Current-Mode Receiver With Highly Selective Frequency-Conversion Interface

A. Overview of the Current-Mode Receiver Architecture

In the conventional voltage-mode RX architecture [4]–[6], a G_m stage is often adopted between the LNA and the mixer for noise suppression and LO-to-RF port isolation purposes. Since the G_m stage usually has high input impedance, the voltage gain of the LNA is the key factor to suppress the noise from the following stages. Typically, in GSM system, to achieve −110 dBm sensitivity, the required LNA voltage gain is usually more than

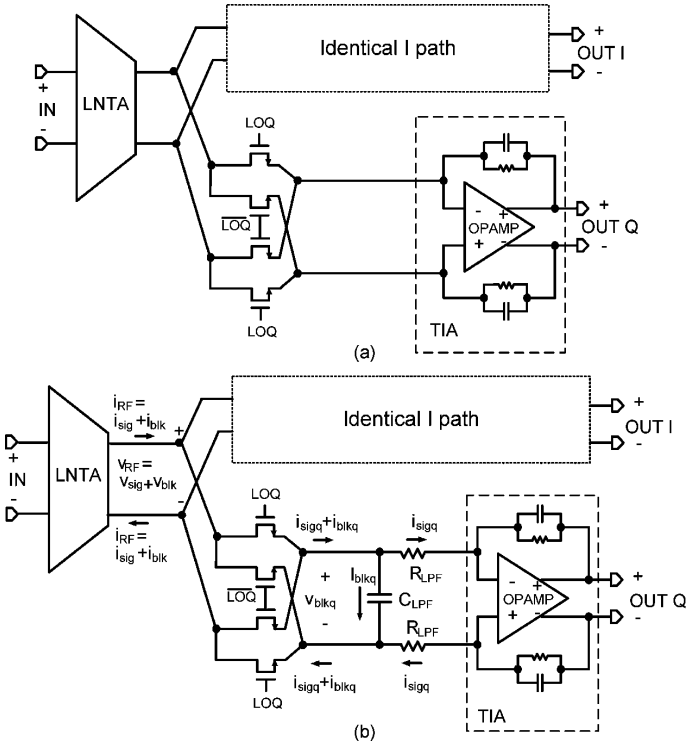


Fig. 3. (a) Current-mode receiver architecture. (b) Receiver with the proposed high-selectivity frequency-conversion interface.

20 dB. Therefore, the LNA output node becomes the dynamic range bottleneck in the voltage-mode RX architecture.

Recently introduced RX topology [7]–[10] bypasses the G_m stage and uses a passive mixer followed by a TIA, as shown in Fig. 3(a). Since the in-band input impedance of the TIA is relatively low and can be up-converted to the RF side of the passive mixer [9], most of the LNA output current flows through the mixer and is down-converted while the LNA output voltage swing is kept small, leading to improved RX linearity. In this RX topology, the LNA functions like an LNTA with voltage input and current output. Despite the obvious improvement over the voltage mode RX, this structure still fails to deal with the 0-dBm OOB blocker because the down-converted blocker current can still saturate the TIA. Considering a 0-dBm blocker with a specified LNTA g_m of 120 mA/V, the TIA input blocker current, after the 25% duty cycle LO down conversion, is ideally up to 8.6 mA, which can saturate the TIA output stage. Moreover, in the GSM system, the 0-dBm blocking signal is located at least 20 MHz offset from the band edge. Therefore, if an OPAMP-based TIA is used, the input impedance of the TIA is no longer negligible at frequencies above 20 MHz due to the finite opamp gain bandwidth product [8]. This results in a large OOB blocker voltage swing at the LNTA output and limits the receiving dynamic range.

To overcome the limitations discussed above, a highly selective frequency-conversion interface is proposed to filter out the down-converted blocker current before entering the TIA while maintaining a small OOB voltage swing at the output node of the LNTA. Fig. 3(b) shows the proposed current-mode RX architecture. It consists of a passive mixer followed by a passive current-mode low-pass filter (LPF) formed by $C_{\rm LPF}$ and $R_{\rm LPF}$. The 25% duty-cycle clocks are applied to the mixer switches as the LO signal. The corner frequency of the LPF, denoted by $\omega_{\rm LPF} = 1/2R_{\rm LPF}C_{\rm LPF}$, should be located between the down-converted blocker and in-band signal frequency. Also shown in Fig. 3(b) are the in-band and OOB blocker signal flows. On the baseband side of the frequency conversion interface (i.e., input of the TIA), the down-converted blocking current ($i_{\rm blkq}$) is filtered out by $C_{\rm LPF}$, and does not appear at the TIA output; at the same time, the in-band signal ($i_{\rm sigq}$), passing through $R_{\rm LPF}$, can be amplified by TIA and is not influenced by the blocker signal. On the RF side (i.e., input of the mixer), due to the natural impedance up-conversion mechanism of the passive mixer, the input impedance of the mixer is approximately equal to [9]

$$Z_{\rm RF}\left(\omega_{\rm LO}+\Delta\omega\right) = \frac{v_{\rm RF}\left(\omega_{\rm LO}+\Delta\omega\right)}{i_{\rm RF}\left(\omega_{\rm LO}+\Delta\omega\right)} \approx R_{\rm SW} + \frac{4R_{\rm LPF}}{\pi^2\left(1+j\frac{\Delta\omega}{\omega_{\rm LPF}}\right)} \tag{2}$$

where $v_{\rm RF}$ and $i_{\rm RF}$ are the mixer input voltage and current, respectively, and both of them consist of in-band ($i_{\rm sig}$ and $v_{\rm sig}$) and blocker signal ($i_{\rm blk}$ and $v_{\rm blk}$). $R_{\rm SW}$ is the ON resistance of the switch. The LO frequency and the offset frequency of the input signal are denoted by $\omega_{\rm LO}$ and $\Delta\omega$, respectively. If the corner frequency of the LPF ($1/2R_{\rm LPF}C_{\rm LPF}$) is much smaller than the down-converted blocker frequency, denoted by $\omega_{\rm blk}$, $v_{\rm blk}$ can be estimated by

$$v_{blk} \approx \left(R_{\rm SW} + \frac{2}{\pi^2\left(j\omega_{\rm blk}C_{\rm LPF}\right)}\right) i_{\rm blk}. \tag{3}$$

Using Fig. 3(b) and (3), the blocker voltage swing at the output ($v_{\rm blkq}$) and input ($v_{\rm blk}$) of the passive mixer can be suppressed by increasing the sizes of the capacitance in the LPF and the switch devices. Under this condition, the OOB blocker is also successfully filtered by the LPF, and the dynamic range requirement of the baseband circuits after this frequency-conversion interface can be relaxed significantly.

B. Output Load of the LNTA

The equivalent single-ended LNTA output load used in this design is shown in Fig. 4. The voltage headroom for the active devices in the LNTA can be maximized by using the inductor load, $L_{\rm load}$. $C_{\rm load}$ and $R_{\rm load}$ represent the equivalent capacitive and resistive loads at the LNTA output port, respectively. The $C_{\rm ac}$ shown in Fig. 4 is the AC coupled capacitor; moreover, the low-frequency even-order distortion (e.g., IM2) from the LNTA can also be blocked by the same capacitor. The design of the LNTA output load is important since improper design may generate a large voltage swing at the LNTA output node and create nonlinearity.

To make the analysis more intuitive based on (2), the mixer input impedance can be modeled by an *RLC* tank in series with the switch ON resistance, shown in Fig. 4. The $R_{\rm eq}$, $L_{\rm eq}$, and $C_{\rm eq}$ can be calculated as

$$R_{\rm eq} = \frac{4}{\pi^2}R_{\rm LPF} \tag{4}$$

$$L_{\rm eq} = \frac{4}{\pi^2\omega_{\rm LO}^2 C_{\rm LPF}} \tag{5}$$

$$C_{\rm eq} = \frac{\pi^2 C_{\rm LPF}}{4} \tag{6}$$

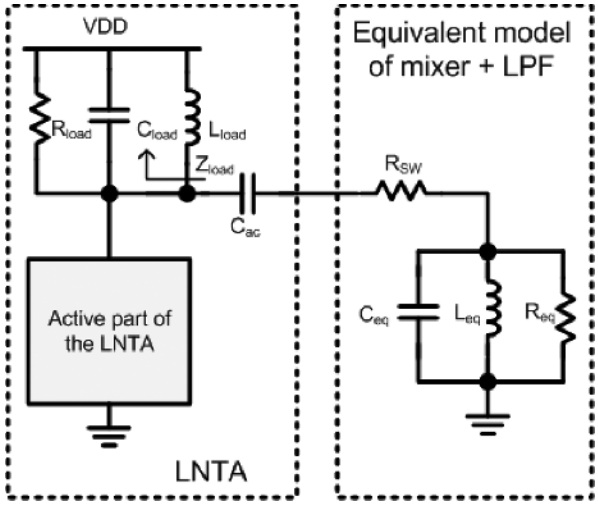


Fig. 4. Equivalent LNTA single-ended output load and model of the mixer and LPF.

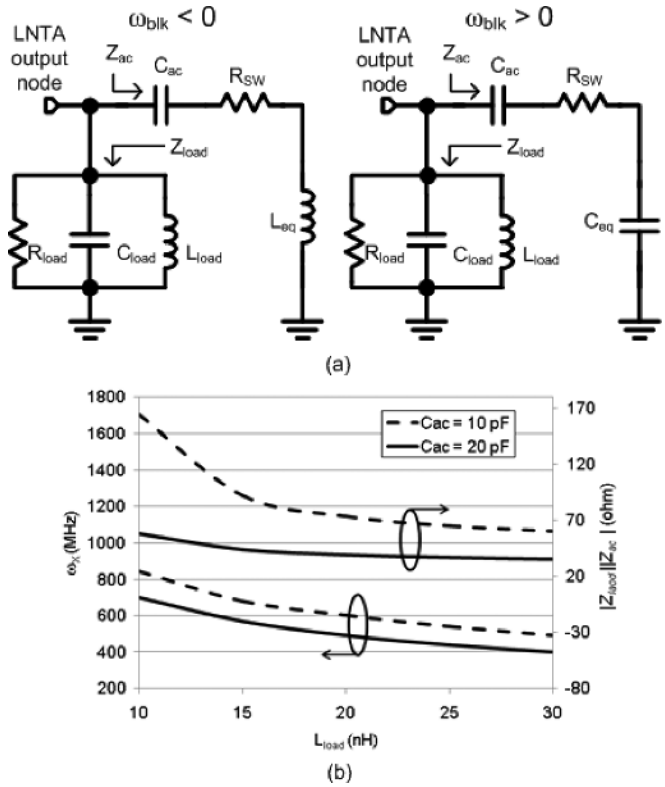


Fig. 5. (a) Equivalent model when $\omega_{\rm blk} < 0$ and > 0. (b) Simulation results of ω_X and $|Z_{load}//Z_{\rm ac}|$ ($C_{\rm load}$, $R_{\rm load}$, and $R_{\rm SW}$ are 300 fF, 600 Ω, and 6 Ω, respectively, and $\omega_{\rm LPF}$ is set to 1.6 MHz with $C_{\rm LPF}$ of 1 μF and $R_{\rm LPF}$ of 100 Ω).

respectively. The 3-dB bandwidth of the *RLC* tank in Fig. 4 is $2\omega_{\rm LPF}$. Therefore, for the OOB blocker at frequency $\omega_{\rm LO} + \omega_{\rm blk}$, where $|\omega_{\rm blk}| \gg \omega_{\rm LPF}$, the impedance of the *RLC* tank is dominated by $L_{\rm eq}$ or $C_{\rm eq}$ for negative or positive $\omega_{\rm blk}$, respectively. The equivalent circuits for both cases are shown in Fig. 5(a).

Considering the toughest case in the ETSI GSM specification for RX, i.e., $|\omega_{\rm blk}| = 20$ MHz and $\omega_{\rm LO}$ is around 900 MHz, it is assumed that $\omega_{\rm LO} + \omega_{\rm blk} \approx \omega_{\rm LO}$ in the following analysis. In Fig. 5(a), the inductor Q and, equivalently, $R_{\rm load}$ is maximized to prevent in-band signal loss. In addition, the Q-factor of the impedance $Z_{\rm ac}$ in Fig. 5(a), should also be high at $\omega_{\rm LO} + \omega_{\rm blk}$ since $R_{\rm SW}$ needs to be small to minimize the blocker voltage swing as described in the previous section. Due to the composite high-Q network, if the resonant frequency of $Z_{\rm load}//Z_{\rm ac}$, denoted by ω_X, is close to $\omega_{\rm LO}$, then a huge voltage swing can be generated at the LNTA output node by the received 0-dBm blocker signal. For demonstration purposes, Fig. 5(b) shows the simulation results of ω_X and $|Z_{\rm load}//Z_{\rm ac}|$ at $\omega_{LO} + \omega_{\rm blk}$ with different $L_{\rm load}$ and $C_{\rm ac}$. In the simulation, $\omega_{\rm LO}$ and $\omega_{\rm blk}$ are 900 and -20 MHz, respectively. As shown in Fig. 5(b), $|Z_{\rm load}//Z_{\rm ac}|$ is large when ω_X is close to $\omega_{\rm LO}$. To achieve a smaller $|Z_{\rm load}//Z_{\rm ac}|$, the chosen ω_X should be much smaller than $\omega_{\rm LO}$. For a given $C_{\rm ac}$, this can be achieved by using a larger $L_{\rm load}$.

In addition, since $C_{\rm ac}$ is directly on the blocker signal path, its size also needs to be made sufficiently large to suppress $|Z_{\rm load}//Z_{\rm ac}|$ as shown in Fig. 5(b). In fact, such choice of $L_{\rm load}$ and $C_{\rm ac}$ equivalently makes $Z_{\rm load}$ as an RF choke whose impedance is much larger than $Z_{\rm ac}$ around $\omega_{\rm LO}$. This allows both the in-band and blocker current generated by the LNTA to flow into the highly selective impedance path $Z_{\rm ac}$ without boosting the LNTA output voltage swing.

In summary, with sufficiently large $C_{\rm ac}$, the following equation is true in the design:

$$\begin{aligned} |Z_{load}| &\approx \left| \frac{\omega_{LO} L_{load}}{1 - \omega_{\rm LO}^2 L_{\rm load} C_{\rm load}} \right| \\ &\gg \left| \frac{1}{\omega_{\rm LO}} \left(\frac{1}{C_{\rm ac}} \pm \frac{4}{\pi^2 C_{\rm LPF}} \right) \right| \\ &\approx |Z_{\rm ac}| \end{aligned} \tag{7}$$

where the Q factors of $Z_{\rm load}$ and $Z_{\rm ac}$ are $\gg 1$.

C. In-Band RF Current Gain

Besides the OOB voltage swing, the in-band RF current gain, which is the ratio between mixer input current and the LNTA output current, also need to be considered in the design. For the in-band signal located at frequency $\omega_{LO} + \omega_{\rm sig}$, where $|\omega_{\rm sig}| \ll \omega_{\rm LPF}$, the impedance of the *RLC* tank in Fig. 4 is dominated by $R_{\rm eq}$ and its equivalent circuit is shown in Fig. 6(a). Based on the equivalent circuit, the in-band RF current gain $G_{\text{in-band}}$ can be easily calculated as

$$\begin{aligned} G_{\text{in-band}} &= \frac{i_{\rm out}}{i_{\rm in}} \\ &= \frac{Z_{\rm load}}{Z_{\rm load} - \frac{j}{\omega_{\rm LO} C_{\rm ac}} + R_{SW} + R_{\rm eq}} \\ &\approx \frac{\frac{j\omega_{\rm LO} L_{\rm load}}{(1 - \omega_{\rm LO} L_{\rm load} C_{\rm load})}}{\frac{j\omega_{\rm LO} L_{\rm load}}{\left(1 - \omega_{\rm LO}^2 L_{\rm load} C_{\rm load}\right)} - \frac{j}{\omega_{\rm LO} C_{\rm ac}} + R_{\rm SW} + R_{\rm eq}} \end{aligned} \tag{8}$$

where $i_{\rm in}$ and $i_{\rm out}$ are the current from the LNTA and the current into the mixer, respectively. Equation (8) is valid when the Q-factor of $Z_{\rm load} \gg 1$ and $\omega_{\rm sig} \ll \omega_{\rm LO}$. According to (7), the impedance of $Z_{\rm load}$ is much larger than $Z_{\rm ac}$ and the impedance of $C_{\rm ac}$. An optimal $G_{\text{in-band}}$ design can be made by gradually

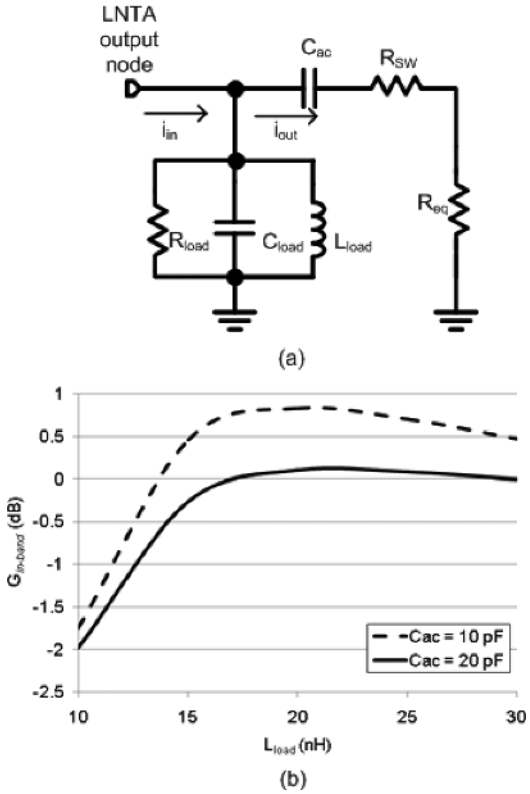


Fig. 6. (a) In-band equivalent model. (b) Simulation results of $G_{\text{in-band}}$.

reducing C_{ac} to decrease the denominator in (8). This allows for a higher in-band RF current gain with an acceptable blocker voltage swing. To demonstrate this phenomenon, the $G_{\text{in-band}}$ simulation results with different L_{load} and C_{ac} are shown in Fig. 6(b).

IV. Adaptive Power Scaling Techniques

In order to be commercially successful, the SAW-less RX must achieve high dynamic range, low RX noise, and low LO PN while operating under the same power constraint as conventional SAW-based RXs. At first, such a design seems extremely difficult given the obvious need to break the universal tradeoffs between linearity, noise, and power consumption in analog circuit design. However, careful examination of real-life channel conditions reveals that the SAW-less RX only needs to tolerate 0-dBm blockers on very rare occasions. This knowledge enables the use of self-adaptive circuits to scale the RX performance with the real-time blocker profile and drastically improve the overall power efficiency.

A. Class-AB Self-Biased LNTA

The LNTA is the first stage of a typical RX, and its main purpose is to provide low noise signal amplification to suppress the noise of the mixer and baseband stages in the RX chain. In SAW-based RX, the OOB blockers are mostly filtered before entering the RX, hence LNTA linearity is not usually a stringent design criteria. A typical narrowband design can achieve < 2 dB NF, $\text{P}_{1\text{dB}}$ of > -15 dBm with a current consumption of < 10 mA [11].

With low OOB impedance synthesized by the high-selectivity frequency-conversion interface, linearity bottleneck at the LNTA output stage is removed. However, the SAW-less LNTA input stage still needs to accommodate the 0-dBm blocker while providing sufficient g_m to suppress noise from later stages. The short-channel MOSs' g_m can be approximated by

$$g_m = \frac{(2+\theta)}{2(1+\theta)^2} K V_{\text{OD}} \tag{9}$$

where

$$\theta = \frac{V_{\text{OD}}}{\lambda}. \tag{10}$$

In (10), λ is a parameter accounting for velocity saturation and K is a constant depending on the technology and proportional to the device's width on length ratio [12]. From (9), it can be seen that higher input transistor's g_m can be achieved by simply increasing the gate–source overdrive voltage V_{OD}. What is less obvious from (9) is that the transistor linearity also improves due to the g_m approaching a large constant value with a higher V_{OD}. This fact can be explained through classical amplifier output stage theory [13]. By increasing the V_{OD} to a point where the transistor's DC bias current I_{DC} exceeds the peak blocker current, the transistor conducts current for the entire cycle of the input signal. This Class-A biasing scheme produces the least amount of distortion at the expense of high constant power consumption which is proportional to the blocker power level that must be processed by the LNTA.

To escape the unavoidable power–linearity tradeoffs in traditional Class-A biased LNA, it is essential to revisit the requirements of the ETSI specification and real-life channel conditions. By realizing the ETSI only specifies a single 0-dBm CW blocker when receiving the -99 dBm in-band signal, second- and third-order inter-modulation performance requirements (IIP3, IIP2) remain the same as conventional SAW-based RXs. Therefore, the LNTA input stage linearity improvement should be solely focused on having sufficiently high dynamic range to handle the large OOB blocker and avoid severe desensitization of the desired GSM signal.

Instead of the conventional Class-A biasing approach, an alternative method of attaining a high dynamic range input V–I stage is to exploit the exponential collector current versus base emitter voltage characteristics of bipolar transistors [14]. For MOS devices operating in the weak inversion region, the same exponential drain current versus gate source voltage exists, with the drain current given by

$$I_d = I_0 e^{V_{gs}/nV_T} \tag{11}$$

where I_0 is the drain current at the onset of strong inversion, $n > 1$ is a nonideality factor, and $V_T = kT/q$ is the thermal voltage [15]. When a large OOB jammer with amplitude v_j is present at the LNTA, the gate–source voltage can be written as the sum of the jammer and the DC bias voltage V_B as

$$V_{\text{gs}} = V_B + v_j \cos(\omega t). \tag{12}$$

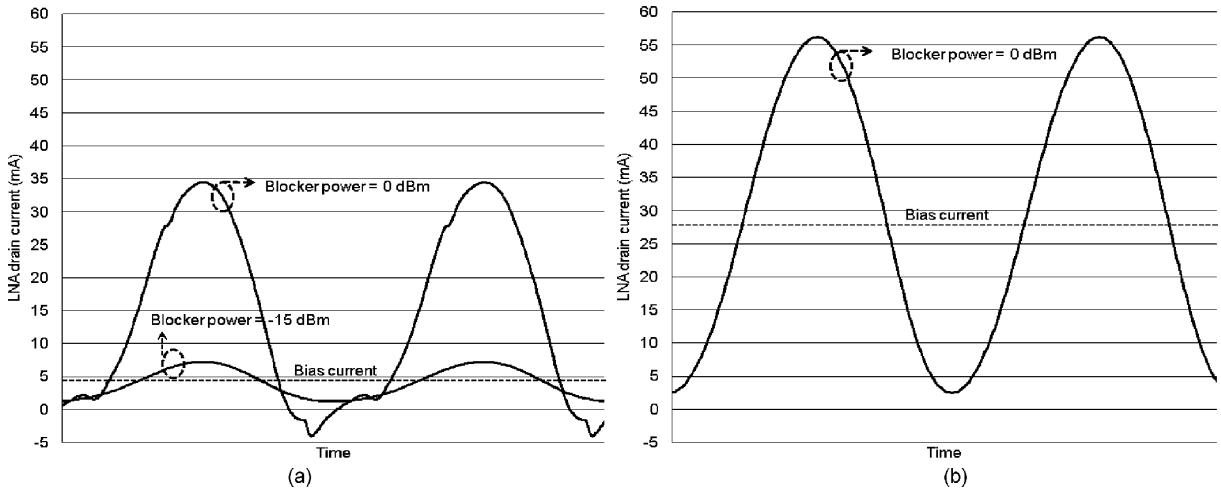


Fig. 7. Drain current waveforms for transistors operating in (a) class-AB and (b) class-A mode.

Combining (11) and (12) and writing its Taylor series expansion around V_B yields

$$I_d = I_0\left(e^{(V_B/nV_T)} + \frac{e^{(V_B/nV_T)}}{nV_T}v_j\cos(\omega t) + \frac{e^{(V_B/nV_T)}}{2(nV_T)^2}v_j^2\cos^2(\omega t) + \frac{e^{(V_B/nV_T)}}{6(nV_T)^3}v_j^3\cos^3(\omega t) + \cdots\right). \tag{13}$$

Grouping terms with the same frequencies results in

$$I_d = I_0\left[\left(e^{(V_B/nV_T)} + \frac{e^{(V_B/nV_T)}}{4(nV_T)^2}v_j^2 + \cdots\right) + \left(\frac{e^{(V_B/nV_T)}}{nV_T}v_j + \frac{3e^{(V_B/nV_T)}}{24(nV_T)^3}v_j^3 + \cdots\right)\cos\omega t + \cdots\right]. \tag{14}$$

The second bracketed term in (14) indicates that the linear gain increases with blocker power. This gain expansion effect in the V–I transfer function can be used to offset gain compression due to other devices in the signal chain, and greatly improves the overall OOB $\mathrm{P_{1dB}}$ of the RX. The improved dynamic range, in general, will translate to lower signal desensitization and higher SNR when blockers are present. In addition to the improved dynamic range, the Class-AB input stage is biased at low current levels and the average current only increases when blocker power becomes large, as indicated by the first bracketed term in (14). This is a significant advantage over traditional Class-A biased LNTAs since strong blockers are not always present under real world operating conditions. Furthermore, the Class-AB LNTA's adaptive biasing behavior is automatic and requires no time-consuming detection and control mechanisms proposed in [9] and [16], which can lead to loss of multiple GSM voice packets depending on the speed of the detection path. Therefore, properly designed Class-AB LNTA can meet the stringent SAW-less dynamic range requirements with similar average power consumption as traditional SAW filter based LNTA.

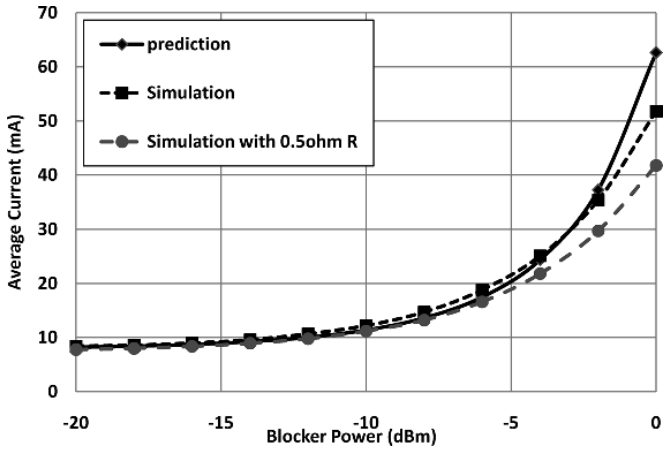


Fig. 8. LNTA input stage average current *versus* blocker power.

Fig. 7(a) shows the simulated current profile of the Class-AB LNTA under −15 dBm and 0-dBm blocking conditions. With −15 dBm OOB blocker, the LNTA is effectively working in the Class-A region and exhibits a linear g_m. Therefore, the RX does not suffer from strong even-order harmonics associated with Class-AB operation. At 0 dBm, the blocker amplitude is large enough for the LNTA to enter the Class-AB mode where the bottom half of current profile is heavily clipped and the average current is increased. For comparison, the current waveform of the same LNTA biased in the Class-A region is shown in Fig. 7(b).

Figs. 8 and 9 show the LNTA input stage average current and g_m versus blocker input power with a fixed drain voltage. The simulated I_D in Fig. 8 increases exponentially with blocker input power and is in close agreement with the values predicted by (14). The gain expansion behavior of the LNTA input stage is shown in Fig. 9. Again, the simulated g_m matches well with the value predicted by (14) and only deviates at large blocker power where higher order terms omitted in (14) starts to contribute to the overall g_m.

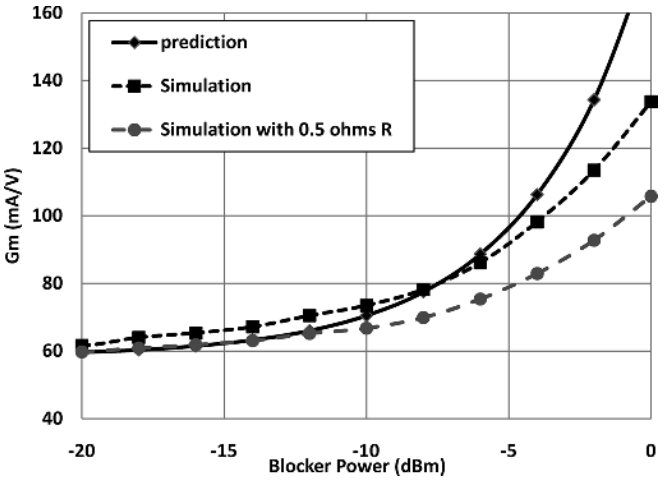


Fig. 9. LNTA input stage gm *versus* blocker power.

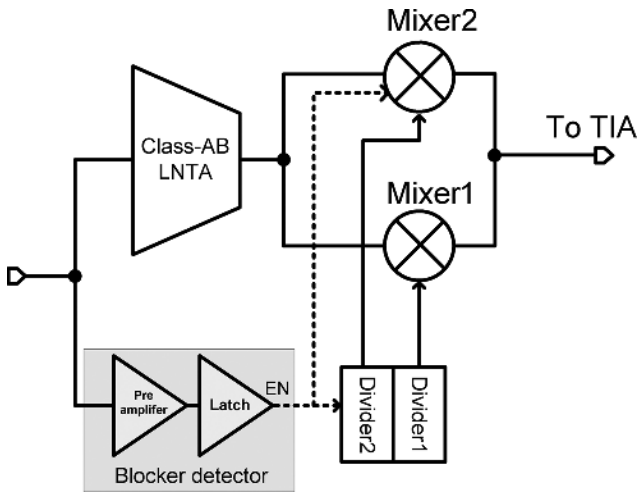


Fig. 10. Block diagram of the blocker detection technique.

Furthermore, Fig. 9 shows that the desirable gain expansion behavior of the Class-AB input stage can be reduced by DC feedback from unwanted parasitic resistance between the source node of the input transistors and ground. Even with a relatively small source-to-ground resistance of 0.5 Ω, simulated g_m at 0-dBm input power level is lower by approximately 20%. This undesirable feedback is due to the increasing average current dropping across the parasitic resistor and raising the source voltage, which then compresses both the I_d and g_m of the input V–I stage. Therefore, care must be taken in the layout to minimize parasitic resistance in the common source node of the input differential pair.

B. Blocker Detection

Similar to the LNTA, the idea of adaptively changing the circuit performance with blocker level can be used to save power in the LO chain. Hence, the use of blocker detection for LO power reduction.

Like all conventional RXs, blocker signals in a SAW-less RX are down-converted to baseband by LO PN through reciprocal mixing and degrade the SNR. With OOB blocker at 0 dBm, PN requirement is -166 dBc/Hz @ 20-MHz offset for the divider. Furthermore, in order to allow the blocker AC current from the LNTA to pass through the mixer switches without distortion, a large transistor size is chosen. Due to the stringent PN requirement and large switch capacitive loading, large current is consumed in the LO buffers. Understanding that large mixer switch size is only necessary when strong blockers are present, a blocker detector is used to determine the PN and switch size requirements depending on the real-time blocker profile.

Fig. 10 shows the block diagram of the blocker detector and its control mechanism. The first part of the blocker detector is a pre-amplifier which is a replica of the Class-AB input stage embedded in the LNTA. Triggered by large blockers, the pre-amplifier produces a detectable DC current that is compared with a fixed reference current and transformed into a control voltage through a simple latch circuit. It is important to note that the detector's Class-AB behavior does not need to match the LNA input devices', and the Class-AB induced current changes can be detected within micro seconds in the event of a blocker.

As shown in Fig. 10, to save the average power consumption, both frequency divider and mixer are divided into two equal parts, Mixer1/2 and Divider1/2 respectively. Mixer1 and Divider1 are always turned on while Mixer2 and Divider2 are controlled by the EN output of the blocker detector. When there is no blocker signal detected, EN is low and Mixer2 and Divider2 are turned off to save power. Conversely, when a large blocker is detected, EN becomes high and Mixer2 and Divider2 are turned on to increase the RX dynamic range. Since the occurrence of such large blocker is rare under real-life conditions, almost 50% of the divider power consumption can be saved by this blocker detection scheme.

V. Circuit Implementation

A. LNTA

Fig. 11 shows the differential inductive-degenerated LNTA. To attain a low-power and high-dynamic-range input V–I stage, the input transistors M_1 and M_2 are biased in the weak inversion region, as described in Section IV. The LNA is biased at 8 mA and achieves a simulated NF of 1.4 dB and OOB $\mathrm{P}_{1\ \mathrm{dB}}$ of $> +1$ dBm. The LNA performance is superior when compared with traditional Class-A amplifier designs that requires > 40 mA of DC bias current for a specified G_m of 120 mA/V and a blocking signal at 0 dBm.

The thick-oxide cascode transistors are biased at 2.3 V to leave sufficient headroom to accommodate for blocker swings in the intermediate nodes of the LNTA. At the LNTA output, the 2.5-V supply together with low OOB impedance provided by the highly selective frequency conversion interface, avoids clipping and suppresses output distortion. Finally, a small source-degeneration inductor was used to maintain a reasonable matching Q while sustaining the Class-AB behavior. The simulated matching gain is around 12 dB.

B. Blocker Detector

Fig. 12(a) shows the schematic of the blocker detector. M_{D1} and M_{D2} are the smallest unit of the input transistors in the LNTA, i.e., M_1 and M_2 in Fig. 11. The gates of M_{D1} and M_{D2}, G_{D1}, and G_{D2}, are connected to nodes A and B in Fig. 11 to sense the input blocker signal. The size of M_{D3} in Fig. 12(a)

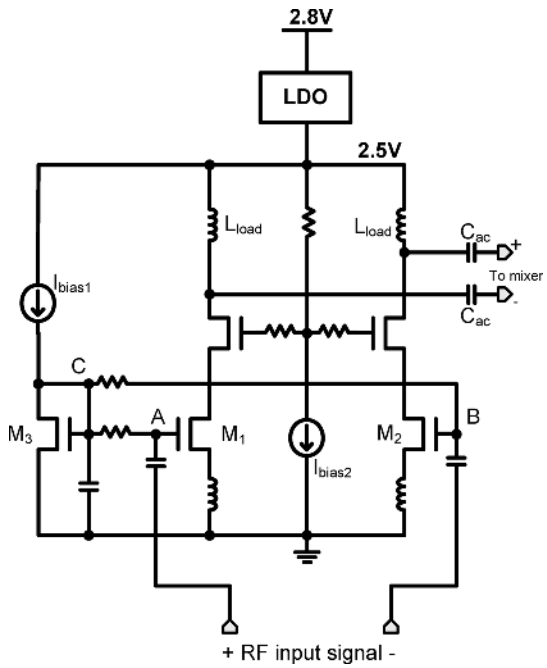


Fig. 11. LNTA schematic.

is two times $\mathrm{M_{D1}}/\mathrm{M_{D2}}$ and its gate $\mathrm{G_{D2}}$ is connected to node C in Fig. 11. $\mathrm{M_{D4}}$ and $\mathrm{M_{D5}}$ are enable switches controlled by "EN_DET" to turn on or turn off the blocker detector. $\mathrm{R_{D1}}$ and $\mathrm{R_{D2}}$ are the resistive loads and the ratio between $\mathrm{R_{D1}}$ and $\mathrm{R_{D2}}$ is 2/3. $\mathrm{C_{D1}}$ and $\mathrm{C_{D2}}$ are used to filter the high frequency parts of $\mathrm{V_1}$ and $\mathrm{V_2}$ which are sensed by the latch. The latch function is enabled when "EN_LAT" is high, and is reset when it is low.

As described in the previous subsection, $\mathrm{M_{D1}}$ to $\mathrm{M_{D3}}$ are biased in the same weak inversion region as $\mathrm{M_1}$ and $\mathrm{M_2}$ in Fig. 11. The DC current of $\mathrm{M_{D3}}$, i_2, is fixed and the summation DC current of $\mathrm{M_{D1}}$ and $\mathrm{M_{D2}}$, i_1, increases with the increase in the received blocker signal due to the Class-AB characteristic. When there is no blocker signal, i_1 is equal to i_2, so $V_1 > V_2$ due to the imbalanced resistive loads. In this situation, the "EN" output of the latch is low; Divider2 and Mixer2 in Fig. 10 are turned off. However, when the received blocker signal is higher than the -12 dBm threshold level in this design, i_1 is increased such that $V_1 < V_2$. This enables both Divider2 and Mixer2 are turned on to handle the blocker signal.

Fig. 12(b) shows the timing diagram of the blocker detection scheme. $\mathrm{M_{D1}}$ to $\mathrm{M_{D5}}$ are turned on by "EN_DET" 15 μs prior to the beginning of each GSM RX burst. After 5 μs for the settling of $\mathrm{V_1}$ and $\mathrm{V_2}$, the latch function is enabled by "EN_LAT". There are 10 μs for divider and mixer to settle before the RX burst in this design. As shown in Fig. 12(b), at the end of the RX burst, the blocker detector is reset and the cycle repeats in the next RX burst.

C. Output Load of LNTA and Frequency-Conversion Interface

The LNA load inductor L_{load} shown in Fig. 4 is implemented by the top two layers of thicker metals for higher Q factor. Furthermore, to save area and increase the inductance, the stack structure is used. As described in Section III, to suppress the output voltage swing at the LNTA output node, the resonant frequency of $Z_{\mathrm{load}}//Z_{\mathrm{ac}}$ is located at approximately 1/4 of the

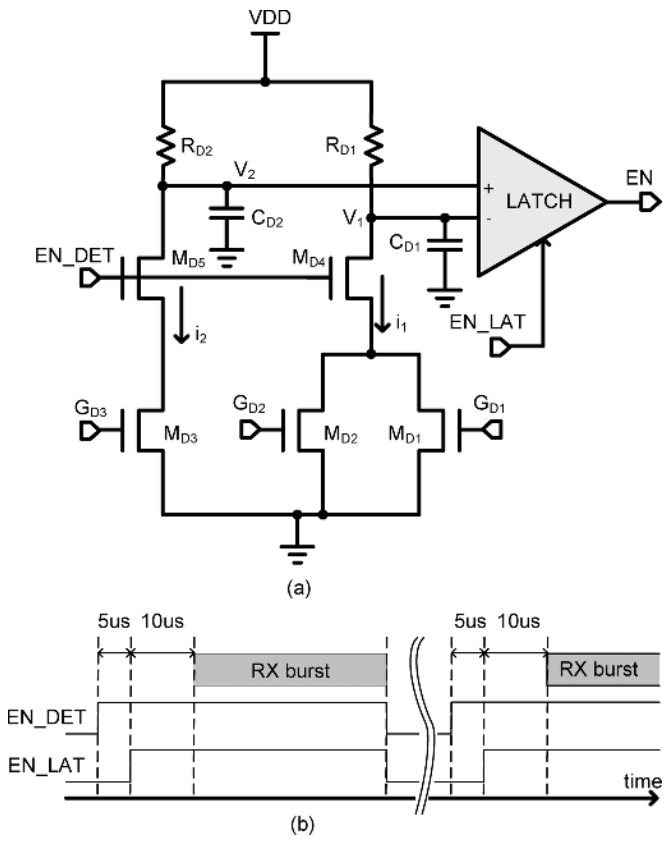


Fig. 12. (a) Blocker detector schematic. (b) Timing diagram of the blocker detection scheme.

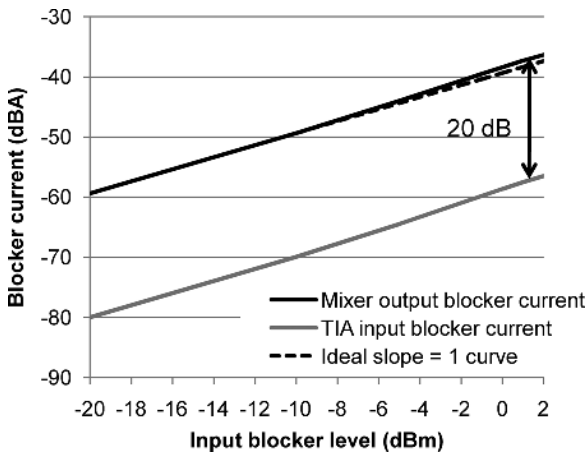


Fig. 13. LB simulation results of the mixer and LPF output blocker current versus the input blocker power at 20 MHz offset.

LO frequency, which are 230 and 510 MHz in LB and HB, respectively. In this design, with 0-dBm 20-MHz offset blocker in the LB case, the LNA single-ended output voltage swing is $\sim$ 400 mV, which is still far from the voltage swing limitation of $\sim$ 800 mV.

For the direct conversion receiver (DCR), the baseband GSM signal is located from DC to 100 kHz while the closest 0-dBm blocker is located at 20 MHz. Therefore, in this design, the pole of the LPF is set to 2 MHz which provides at least 20-dB rejection for the down-converted blocker current before entering TIA, while preserving the in-band signal. As described

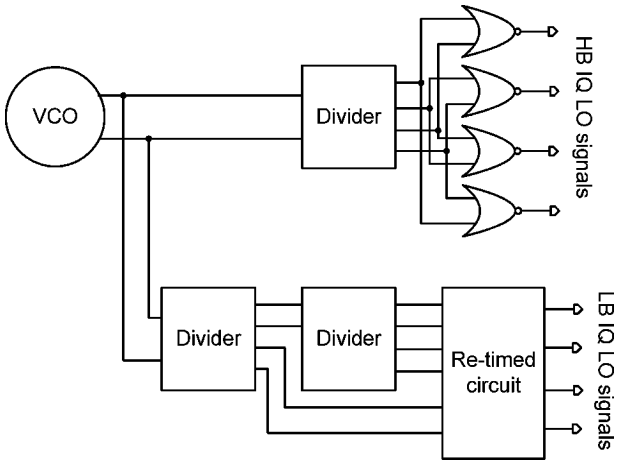


Fig. 14. Block diagram of the 25% clock generator.

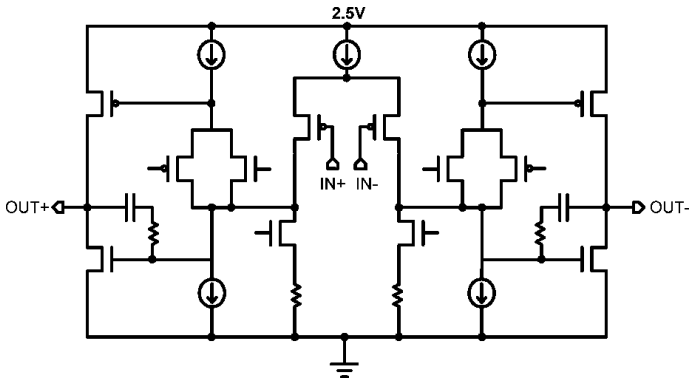


Fig. 15. Schematic of the opamp.

in Section III, $C_{\rm LPF}$ in Fig. 3(b) should be designed as large as possible to suppress the blocker voltage swing at the mixer input and output ports. However, in practice, its size is limited by the available chip area. In this design, to maximize the capacitance density, MOM capacitors are stacked on top of the accumulation-mode MOS varactors for the $C_{\rm LPF}$ implementation. Fig. 13 shows the LB simulation results of the mixer and LPF output blocker current versus the input blocker power at 20-MHz offset. It is shown that the mixer is still linear when the blocker power is 2 dBm, and the slight current expansion is from the Class-AB LNTA. Furthermore, the blocker current after LPF is only 1.15 mA when the blocker power is 0 dBm, which is a reasonable input current for TIA under normal operation.

D. 25% Clock Generator

The fully integrated fractional-N frequency synthesizer operates at twice the LO frequency and a divide-by-2 and divide-by-4 circuits are used to generate 25% duty-cycle IQ LO signals in HB and LB, respectively. The block diagrams of both clock generators are shown in Fig. 14. Each divider implements a divide-by-2 function and consists of two cross-connected D-flip-flops which are formed by clocked inverters in order to obtain large signal swing [17]. In HB, the outputs of the divider circuit have 50% duty cycle and they are applied to the NOR gates to generate the required 25% duty-cycle IQ signals. In LB, the outputs of the second divider are re-timed by the outputs of the first divider to generate the 25% duty-cycle IQ signals. Therefore, the noise from the second divider does not contribute to the final IQ signals. The re-timed circuit in Fig. 14 is implemented by AND gates.

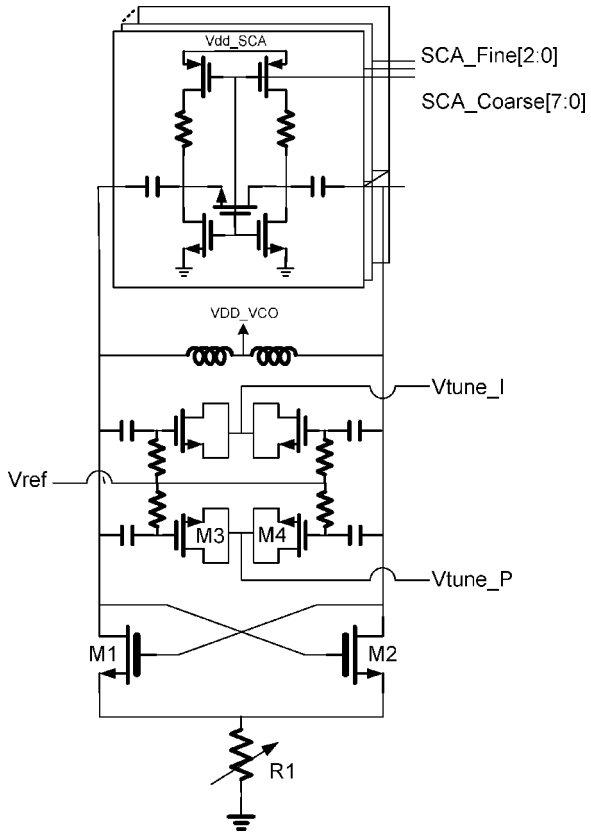


Fig. 16. Block diagram of the VCO, including dual path varactors and switched capacitor array (SCA).

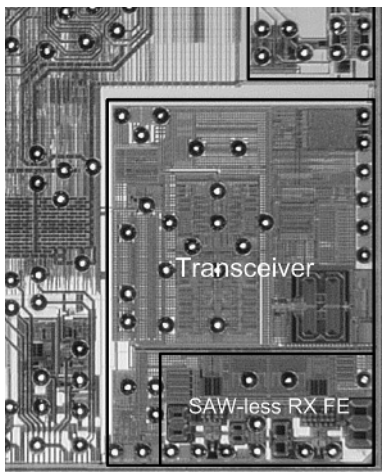


Fig. 17. Die micrograph.

E. TIA

The TIA stage is a fully differential operational amplifier connected with feedback resistors and capacitors as shown in Fig. 3(b). The resistor value is determined by the conversion gain and the *RC* low-pass corner is determined by the RX filtering requirement.

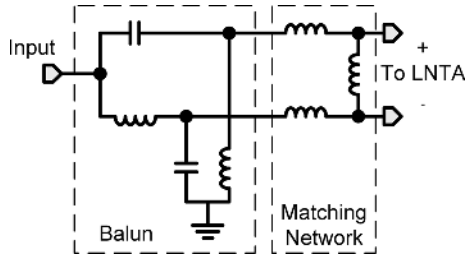


Fig. 18. Balun and matching network.

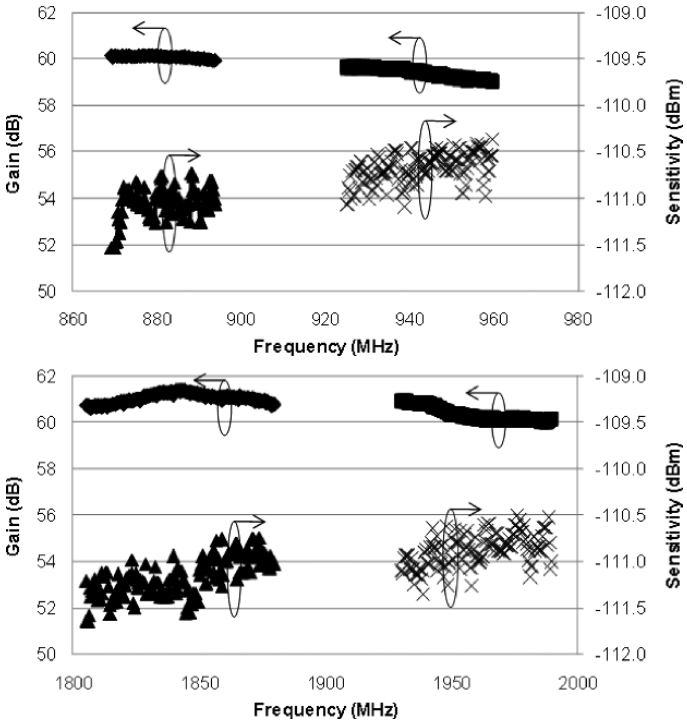


Fig. 19. RX gain and sensitivity.

The schematic of the op-amp is shown in Fig. 15. Class-AB output stage is used to maximize the dynamic range. The opamp is designed with low noise in order to avoid the noise amplification factor increasing the opamp noise contribution to the whole RX [18]. Large input transistor sizes are chosen to achieve low flicker noise and degeneration resistors are also used to suppress the noise from the nMOS load in the first stage. Special care must be taken to ensure circuit stability due to the large second pole introduced by the large capacitance from the current-mode LPF.

F. Frequency Synthesizer

To achieve excellent OOB blocker performance, the design challenges of the frequency synthesizer are to achieve low reference spur and good PN at 20 MHz away from carrier. Consider the case for a 0-dBm LB blocker at 20 MHz away from carrier, VCO PN is required to be −154 dBc/Hz around 4 GHz in order to maintain sufficient SNR at baseband. In this work, a dual-path loop filter [19] is adopted to save chip area.

1) Spur Control: To prevent low-frequency harmonics coupling to the VCO frequency, first- or second-order passive *RC*

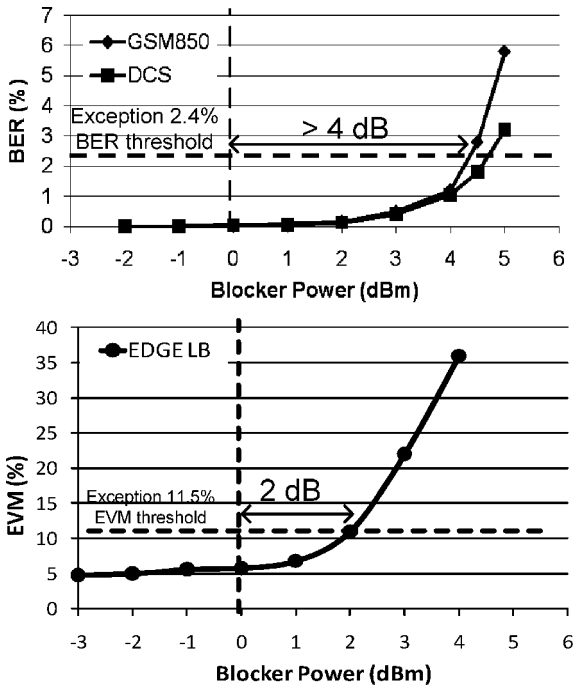


Fig. 20. RX GSM BER and EDGE EVM versus blocker power, where GSM signal power is −99 dBm and EDGE signal power is −85 dBm.

filters are applied between the LDOs and circuits of the synthesizer which can provide sufficient rejection. The locations of all capacitors and resistors are carefully placed for better isolation. The ground planes of the synthesizer are separated into high frequency and low frequency parts. Sensitive circuits such as VCO and bandgap circuit use the high-frequency ground; while others use the low-frequency ground. The metal shielding is often used to isolate sensitive nodes from active signal lines. The charge-pump linearity is improved by using smaller switch sizes and symmetric layout.

2) VCO: The VCO core circuit is shown in Fig. 16. The nMOS-only architecture is selected because it offers higher voltage headroom under a given supply voltage. Moreover, for a specified negative resistance, the nMOS cross-coupled pair is much smaller than the pMOS one; hence the nMOS-only architecture also minimizes the nonlinear junction capacitance and reduces supply pushing. In this design, a tail resistor, R1 in Fig. 16, is used to bias the VCO to avoid flicker noise up-conversion. The VCO is supplied by a voltage of 2.45 V from LDO and R1 is implemented by a programmable resistor to set the bias current. The switched capacitor array follows a conventional design [20] and all MOS devices have thick oxides to avoid reliability issues.

The inductor is one of the most important passive components in the VCO because it accounts for 70% of the total *LC*-tank loss. Moreover, it is vulnerable to magnetic coupling which may result in symmetric spurs due to the limiter transfer action. In this work, field-cancelling inductors [21] are used in order to provide rejection from the common-mode magnetic field. Since it behaves as a dipole, it also prevents coupling into other resonators in the SoC. The aspect ratio of the inductor is sized in such a way to achieve best available Q, considering mutual inductance and metal loss tradeoff. In the 65-nm process technology, the AL-RDL layer alone is used for inductor routing

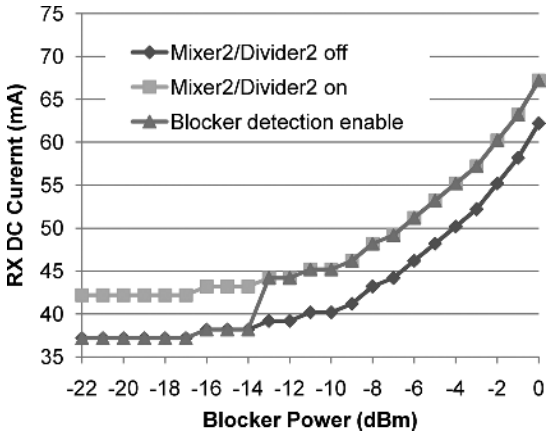


Fig. 21. RX DC current *versus* blocker power.

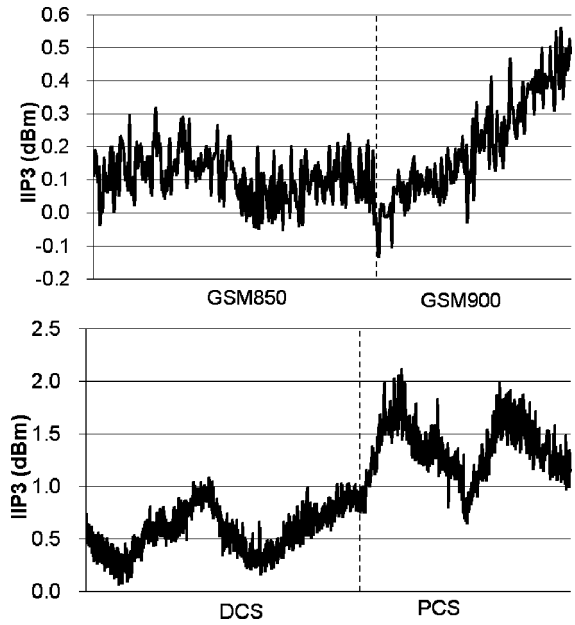


Fig. 22. Measured IIP3.

due to its lower sheet resistance. Simulated inductance is 1 nH, and Q is around 22 at 4 GHz.

VI. Measurement Results

Fig. 17 shows the die micrograph of the transceiver portion in the 65 nm CMOS SoC chip. The chip is packaged in a 179-ball FCCSP package and the total chip size is 8.6×8.1 mm^2 where the transceiver occupies a die area of 2.6×1.9 mm^2. Operating under a 3.8-V external supply, the RX and synthesizer draw 37.1 and 21.8 mA, respectively, in the continuous RX mode. The RX current increases to $\approx$ 60 mA when a 0-dBm OOB blocker is present.

To demonstrate true SAW-less operation, all measurements are performed on PCB with *L-C* lattice-type balun and matching network, as shown in Fig. 18. The inductance and capacitance are 12/3.3 nH and 2.2/1.5 pF in LB/HB, and the simulated maximum amplitude and phase imbalance in LB/HB are 1.1/1.7 dB and 1°/0.9°, respectively. When no blockers are present, the

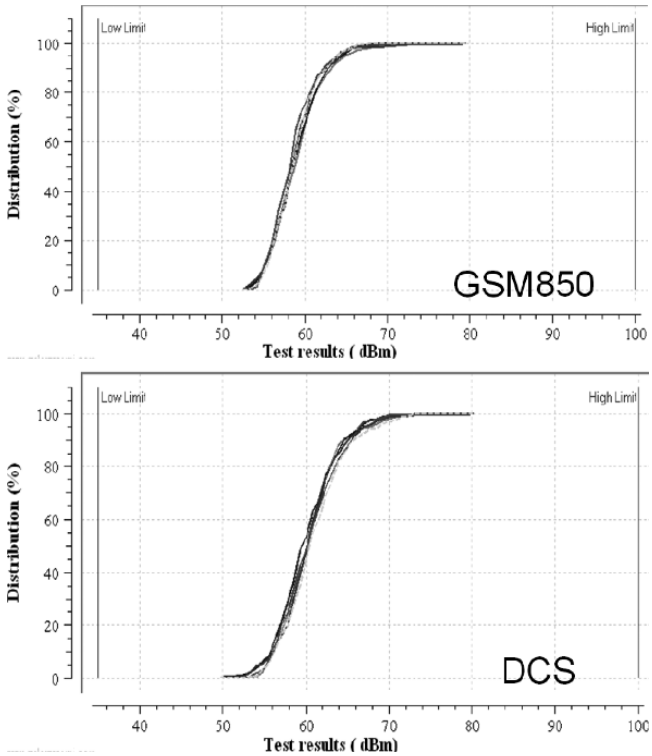


Fig. 23. Measured IIP2.

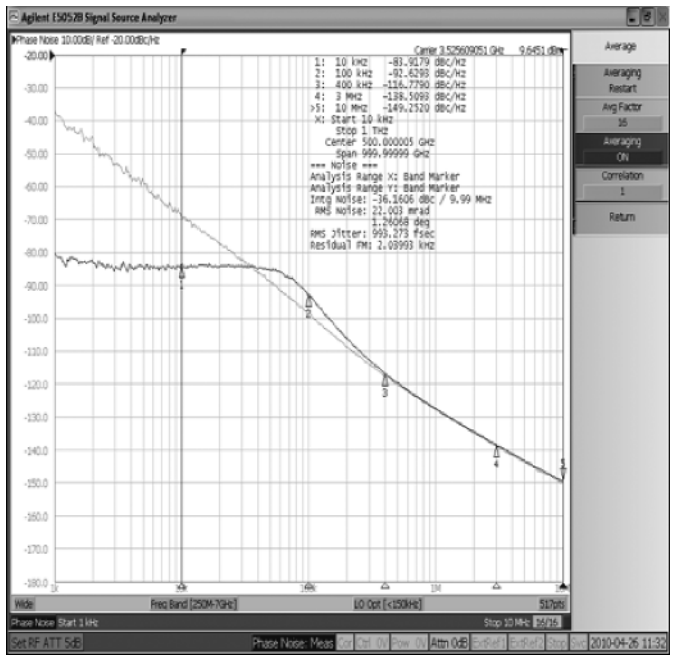


Fig. 24. Synthesizer phase noise profile.

measured RX gain and sensitivity for all channels are shown in Fig. 19. The typical gain is $\approx$ 60 dB, while the sensitivity is < -110 dBm, which is comparable to the conventional RX with SAW filters. The measured OOB $P_{1\,\mathrm{dB}}$ is $+1$ dBm and the RX's robustness to blocker interference is demonstrated in Fig. 20, where the BER remains $< 2.4\%$ for blocker powers of $\lesssim$ 4.3/4.7 dBm at 20/80-MHz offset for the GSM850/DCS

TABLE I
RX PERFORMANCE SUMMARY

	This Work		[9]	
Band Of Operation	GSM850 / GSM950	DCS / PCS	GSM850 / GSM950	DCS / PCS
RX Gain (dB)	59.6	60.7	78.4	77.8
RX Sensitivity (dBm)	-110.3 to -111.5	-110.5 to -111.7	n/A	-110 to -111
RX NF (dB)	2.7	2.9	3.3▲	3.1▲
RX NF $f_{blockoffset}$=±3MHz (dB)	5.2	6.5	8.5	7.3
RX NF $f_{blockoffset}$=±20MHz (dB)	9.5	n/A	10.9◊	n/A
RX NF $f_{blockoffset}$=±80MHz (dB)	n/A	8	n/A	11.4
RX IIP2 (dBm)	> 50	> 50	>50	>45
RX IIP3 (dBm)	0	0	-11.2	-12.4
Exception Frequencies	$3f_{LO}$, $3f_{LO}$±200k, $5f_{LO}$ / $3f_{LO}$, $5f_{LO}$, $5f_{LO}$±200k	$2f_{LO}$, $3f_{LO}$, $3f_{LO}$±200k, $3f_{LO}$±400k / $2f_{LO}$, $3f_{LO}$, $3f_{LO}$±200k, $3f_{LO}$±400k, $3f_{LO}$±600k	n/A	n/A
SX 26MHz Spur (dBc)	< -85		n/A	n/A
SX PN @ 20MHz (dBc/Hz), f_{LO}= 3.5GHz	<-154		n/A	n/A
RX Current (mA)	58.9□		55□	55□
Supply Voltage (V)	2.5	2.5	1.3	1.3

▲ high Q BPF disabled

◊ the blocker power is -11 dBm which is 11-dB lower than the ETSI specification

□ includes SX

band. Similarly, the RX EVM remains $< 11.5\%$ for blocker power $\sim$ 2 dBm when operating under MCS-9 in EDGE mode.

The blocker detection function is implemented in HB only since the HB divider consumes more power due to higher operation frequency. Fig. 21 plots the measured RX current versus the 80-MHz offset blocker power in HB. Notably, the Mixer2 and Divider2 in Fig. 10 also can be manually controlled in this design. It can be observed that the blocker detector turns on Mixer2 and Divider2 when the blocker level is larger than -13 dBm, which is 1 dB less than the prediction. The discrepancy from simulation mainly comes from the device mismatch since the smallest unit of the LNA input transistor is used for blocker detection. Therefore, one should keep enough margins to tolerate such device mismatch. As shown in Fig. 21, 4 mA can be saved when the blocker level is smaller than -13 dBm. When the blocker detection function is turned on, an additional 1 dB of blocker margin is achieved.

The IIP3 is measured with two tones located on 0.8- and 1.6-MHz offset frequencies. Fig. 22 plots the measured IIP3 at the maximum gain for all channels from GSM850 to PCS. The IIP3 is around 0 dBm which is much better than the voltage-mode RX since the G_m stage between the LNA and mixer has been removed.

The IIP2 is measured with two tones located at 6- and 6.1-MHz offset frequencies. Over 1300 chips cross five different process corners are measured. Fig. 23 plots the measured IIP2 distribution at the center channel in GSM850 and DCS. The worst IIP2 is around 50 dBm, which is 20 dB above the design requirement. Since the LPF corner in this design is 2 MHz, the two-tone voltage swing at the input and output of the mixer is suppressed, resulting in better IIP2 performance.

Without the SAW filters, the measured LB RX $2f_{\rm LO}$ and $3f_{\rm LO}$ rejections are 68 and 44 dB, respectively. A blocker around the $f_{\rm LO}$ harmonics can be down-converted to around the signal band, causing RX SNR degradation. Moreover, the close-in LO PN within the corresponding offset frequency range is also down-converted to the signal band and degrades the RX SNR further. When the BER is $> 2.4\%$, exceptions must be taken as the desired signal cannot be decoded properly. The RX requires 4/4/6/8 exceptions in the GSM850/GSM900/DCS/PCS band, which satisfy the ETSI limit of 24 exceptions per band.

The measured PN profile of the 3.536-GHz synthesizer output signal is shown in Fig. 24. The PN is -83.9, -92.6, -116.8, -138.5, and -149.3 dBc/Hz at 10-k, 100-k, 400-k, 3-M, and 10-MHz offset, respectively. Finally, the synthesizer exhibits < -85-dBc reference spur at 26-MHz offset. Aided by interference cancellation techniques [22] implemented in the digital baseband core, the reference spur results in negligible SNR degradation with blockers applied at frequencies equal to multiples of the 26-MHz reference.

The RF transceiver performance results are summarized in Table I. Although [9] does not require any external components, this work has 1.4 dB better NF in the 20-MHz blocker case when the blocker power is 11 dB larger than that in [9]. In addition, this work provides more than 6-dB NF margin in the 20/80 blocker case, which translates to greater tolerances for PCB and external component variations.

VII. Conclusion

This paper demonstrates the possibility of replacing the discrete SAW filter function with inexpensive on-chip components to reduce cost and form factor for today's cellular system. This is achieved by employing several techniques, including current-mode RX with highly selective frequency conversion interface, Class-AB self-bias LNTA, and blocker detection. In addition, careful RX system budgeting to allow maximum usage of voltage and linearity headroom for every stage translates to a fully optimized solution. The measurement results show that the overall performance, current consumption, and die area all meet or exceed that of a typical SAW-based RX. Furthermore, the device has passed the full type approval (FTA) test with margins and reached a mass-production state.

References

[1] [Online]. Available: http://en.wikipedia.org/wiki/GSM

[2] H. Darabi *et al.*, "A quad-band GSM/GPRS/EDGE SoC in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 870–882, Apr. 2011.

[3] C. H. Wang *et al.*, "A direct digital frequency modulation PLL with all digital on-line self-calibration for quad-band GSM/GPRS transmitter," in *Proc. IEEE Symp. VLSI Circuits*, 2009, pp. 190–191.

[4] B. Bakkaloglu, P. Fontaine, A. N. Mohieldin, S. Peng, and F. Dulger, "A 1.5-V multi-mode quad-band RF RX for GSM/EDGE/CDMA2K in 90-nm digital CMOS process," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1149–1159, May 2006.

[5] J. Ryynanen, K. Kivekas, J. Jussila, L. Sumanen, A. Parssinen, and K. A. I. Halonen, "A single-chip multimode receiver for GSM900, DCS1800, PCS1900, and WCDMA," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 594–602, Apr. 2003.

[6] P. Sivonen, J. Tervaluoto, N. Mikkola, and A. Parssinen, "A 1.2-V RF front-end with on-chip VCO for PCS1900 direct conversion receiver in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 384–394, Feb. 2006.

[7] D. Kaczman, M. Shah, M. Alam, M. Rachedine, D. Cashen, L. Han, and A. Raghavan, "A single-chip 10-band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with digRF 3G interface and +90 dBm IIP2," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 718–739, Mar. 2009.

[8] N. Kim, L. E. Larson, and V. Aparin, "A highly linear SAW-less CMOS receiver using a mixer with embedded Tx filtering for CDMA," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2126–2137, Aug. 2009.

[9] A. Mirzaei, H. Darabi, A. Yazdi, Z. Zhou, E. Chang, and P. Suri, "A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 1–15, Apr. 2011.

[10] A. Mirzaei *et al.*, "Analysis and optimization of current-driven passive mixers in narrowband direct-conversion receivers," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2678–2688, Oct. 2009.

[11] X. Fan, H. Zhang, and E. Sinencio, "A noise reduction and linearity improvement technique for a differential cascode LNA," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 588–599, Mar. 2008.

[12] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004.

[13] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York: Wiley, 2001.

[14] K. L. Fong, C. D. Hull, and R. G. Meyer, "A class AB monolithic mixer for 900-MHz applications," *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1166–1171, Aug. 1997.

[15] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. Boston, MA: McGraw-Hill, 1999.

[16] W. Xiong and L. E. Larson, "An S-band low-noise amplifier with self-adjusting bias for improved power consumption and dynamic range in a mobile environment," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 1999, pp. 497–500.

[17] M. D. Tsai, "Low-Noise Frequency Divider," U.S. Patent 7 719 327, May 18, 2010.

[18] M. Valla, G. Montagna, R. Castello, R. Tonietto, and I. Bietti, "A 72-mW CMOS 802.11a direct conversion front-end with 3.5 dB NF and 200-kHz 1/f noise corner," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 970–977, Apr. 2005.

[19] D. Mijuskovic, M. Bayer, T. Chomicz, N. Garg, F. James, P. McEntarfer, and J. Porter, "Cell-based fully integrated CMOS frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 271–271, Mar. 1994.

[20] P. Andreani, K. Kozmin, P. Sandrup, M. Nilsson, and T. Mattsson, "A TX VCO for WCDMA/EDGE in 90 nm RF CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1618–1618, Jul. 2011.

[21] A. Poon, A. Chang, H. Samavati, and S. S. Wong, "Reduction of inductive crosstalk using quadrupole inductors," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1756–1756, Jun. 2009.

[22] J. G. Andrews, "Interference cancellation for cellular systems: A contemporary overview," *IEEE Wireless Commun.*, vol. 12, no. 2, pp. 19–29, Apr. 2005.

Chi-Yao Yu (M'10) was born in Taipei, Taiwan, in 1978. He received the M.S. degree in communication engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2002, and the Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2008.

He has been with MediaTek Inc., Hsinchu, Taiwan, since 2008, where he is working on analog and RF IC design for wireless communications. His current research interest is ultrahigh dynamic range receivers for cellular systems.

Ivan Siuchuang Lu (M'04) was born in Taipei, Taiwan, in 1979. He received the B.E.E. degree from the University of Queensland, Brisbane, Australia, in 2001, and the Ph.D. degree from the University of New South Wales, Sydney, Australia, in 2006.

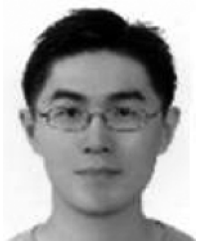
After graduation, he joined Marvell Semiconductor, Santa Clara, CA, where he contributed to transceiver design for MIMO WiFi and GPS applications. He has been with Mediatek USA, San Jose, CA, since 2009 and is currently a Member of Technical Staff. His current research interests include advanced RF CMOS transceiver architectures and circuits for wireless communication systems.

Yen-Horng Chen was born in Taipei, Taiwan, in 1977. He received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1999 and 2001, respectively.

From 2001 to 2005, he was with Industrial Technology Research Institute (ITRI) and worked on IF PGAs, filters, and AGC design for WCDMA, DAB, and UWB standards. In 2005, he joined Mediatek, Hsinchu, Taiwan, as a Technical Manager, where he developed low-noise receiver front-ends in CMOS process, digital auto-calibration for receiver impairment, receiver system planning, and analysis for GSM/EDGE standard. In 2010, he joined Mediatek, Austin, TX, where he is developing all-digital PLL and LTE transceivers.

Lan-Chou Cho was born in Taipei, Taiwan, in 1978. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2001, 2003, and 2008, respectively.

He is currently with Mediatek Inc., Hsinchu, Taiwan. His research interests include phase-locked loops, delay-locked loops, and high-speed CMOS data-communication circuits for multiple gigabit applications.



Chih-Hao Eric Sun was born in Taipei, Taiwan, in 1978. He received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2000, and 2002, respectively.

He is currently with Mediatek Inc., Hsinchu, Taiwan, working on cellular products.

Chih-Chun Tang was born in Taipei, Taiwan, in 1974. He received the Ph.D. degree from the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan, in 2002.

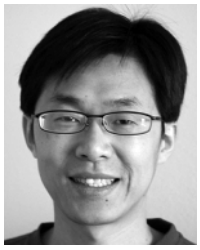
He has been with the RF Department, MediaTek Inc., Hsinchu, Taiwan, since 2002 and joined the design of GSM/EDGE RF stand-alone transceivers and SOCs. Now, he is the RF Transceiver Project Leader of 3G WCDMA.

Hsiang-Hui Chang received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1999, 2001, and 2004, respectively.

He is currently with MediaTek Inc., Hsinchu, Taiwan, where he is involved with wireless communication products. His research interests are digital-enhanced PLLs, all-digital frequency synthesizers, RF system architecture design, and digital-assisted transceiver design.

Wen-Chang Lee (M'10) received the B.S. degree in electrical engineering from the National Sun-Yat-Sen University, Kao-Hsiung, Taiwan, in 2000, and the M.S. degree in communication engineering from the National Chiao Tung University, Hsin-Chu, Taiwan, in 2002.

From 2002 to 2008, he was with VIA Technologies, Inc., Taipei, Taiwan, working on cellular and wireless-LAN RF transceivers, as a Design Lead in the GSM/GPRS/EDGE synthesizer and transmitter development. In 2008, he joined MediaTek, Hsinchu, Taiwan, focused on VCO and synthesizer in cellular applications. Since 2010, he has been with the MediaTek, Austin, TX, as a Technical Manager working on advanced synthesizer architecture.



Sheng-Jui Huang was born in Kaohsiung, Taiwan, in 1974. He received the M.S.E.E degree from National Chiao Tung University, Hsinchu, Taiwan.

From 2000 to 2005, he was with Realtek Semiconductor, where he was involved with mixed-signal circuits and line drivers for Gigabit Ethernet. In 2005, he joined MediaTek, Hsinchu, Taiwan, as a Technical Manager, where he developed high-definition audio ADC and continuous-time delta-sigma ADC for telecommunications. He currently works on synthesizer-related circuitry.

Tzung-Han Wu (S'06–M'07) was born in Taipei, Taiwan, in 1979. He received the B.S. and M.S. degrees from the Department of Electrical Engineering, National Chung-Hsing University, Taichung, Taiwan, in 2001 and 2003, respectively, and the Ph.D. degree in communication engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2007.

He worked on receiver circuits using CMOS, SiGe HBT and GaInP/GaAs HBT technologies. Currently, he is with the RFIC Design Department, MediaTek Inc., Hsinchu, Taiwan. His current research interests are in the areas of RF receivers and multi-radio SOC. He designs receiver front-ends and is the top integrator in 2G and 3G SoC products.

Dr. Wu is a member of Phi Tau Phi.

Chinq-Shiun Chiu was born in Taiwan in 1971. He received the B.S. degree from National Tsing Hua University, Hsinchu, Taiwan, in 1993, and the M.S. degree from National Taiwan University, Taipei, Taiwan, in 1995, both in electrical engineering.

He is currently a design manager with MediaTek Inc., Taiwan. His interests include analog and RF IC design for cellular transceiver and multi-radio system integration in SOC. He holds over 10 issued patents with Mediatek Inc.

George Chien (M'00–SM'10) was born in Athens, GA, in 1971. He received the B.S. degree from the University of California, Los Angeles, in 1993, and the M.S. and Ph.D. degrees from the University of California, Berkeley, in 1996 and 1999 respectively, all in electrical engineering and computer science.

In January 2000, he joined Marvell Semiconductor, Santa Clara, CA, where he worked on several generations of transceivers for WLAN and BT. In January 2008, he joined MediaTek, Inc., where he focuses on a wide range of transceivers designs from cellular to connectivity applications in SOC applications. He is currently a Director of RF design division with MediaTek, Inc., San Jose, CA. He holds over 15 issued and several pending patents and has published over ten IEEE conference and journal papers. His research interests include novel transceiver architecture and circuit designs for deep-submicron CMOS processes.

Dr. Chien was a corecipient of ISSCC Jack Kilby Award for Outstanding Student Paper in 1997. Since 2006, he has been serving on the ISSCC Technical Program Committee.