A Scalable Multiphase Buck Converter with Average Current Share Bus

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Abstract-**The paper presents a scalable multiphase synchronous buck converter which meets the tight requirements of the next generation microprocessors. Flexibility in the number of phases (1-16 phases) accommodates requirements of various applications. The converter can be easily expanded or paralleled with other Voltage Regulator Modules (VRM) through an average current share bus. The distributed control IC architecture allows for local phase current signal processing, which minimizes induced noise and facilitates layout while reducing the gate driver to power stage impedance. The experimental results are given to show the advantages of the converter.**

Keywords – VRM; scalable multiphase converter; current sharing

I. INTRODUCTION

In order to power the next generation microprocessors which require about 1V voltage and up to 100A current [1] [2], the number of phases in the interleaved multi-phase synchronous buck converter has been increasing. Some of today's designs require as many as 8 phases. Selecting the optimum number of phases is determined by many factors, e.g. output current, system efficiency, the transient requirement, thermal management, costs of capacitors, MOSFET performance, size restriction, and overall system cost. Phase selection is further complicated due to continually changing current requirements making a scalable multiphase converter necessary.

To keep system costs low, control ICs have been offered in fixed phase number options, with and without integrated drivers. Some ICs offer a programmable number of phases within a limited range at the cost of unused or redundant die area. For control ICs with integrated drivers, the long distance between the controller and power stage increases the parasitic impedance which deteriorates gate drive performance. Furthermore, current sense signals need to be routed back to the control IC which is sometimes several inches away from the sense point increasing the probability of signal distortion. The magnitude of the current signal is usually very small and requires amplification in the control IC for accurate current sharing and adaptive voltage positioning.

The circuitry needed to implement current sharing of paralleled voltage regulator modules (VRM) is usually not integrated into the control IC of the multiphase converter. For high-end microprocessor applications which require paralleling of modules, current sharing circuitry with discrete components must be added at extra cost and at a penalty of using valuable board space.

This scalable multiphase buck converter consists of a central controller directing an array of 1 to 16 paralleled buck power stages. This scalable architecture facilitates design trade-off choices of multiphase converters and minimizes design effort by allowing the addition or removal of a phase to match solution requirements. The central controller incorporates the system level functions and can be placed farther away from the power stage. The phase controller implements the functions required for power stage control including current sense amplification and MOSFET gate drive. The phase controller is placed close to the power stage to take advantage of reduced trace lengths and impedances. Current sharing among phases is achieved through an average current share loop, which ensures an even current distribution among different phases. The current share bus can also be extended to other VRMs to achieve current sharing among modules.

This paper presents the concept and block diagram of the scalable buck converter using feed-forward voltage mode control and current sharing bus. The experimental results of a four/five/six phase synchronous buck converter are given to verify the advantages of the scalable converter.

II. PRINCIPLE AND BLOCK DIAGRAM

Fig. 1 shows the simplified block diagram of the scalable buck converter, which consists of the central control IC [3] and multiple phases of synchronous buck converter controlled by phase control ICs [4]. The central controller contains the oscillator, 6-bit Digital to Analog Converter (DAC) to program the output voltage, error amplifier, fault-protection circuitry, and etc. The central controller is connected to the phase ICs through a 5-wire bus which includes a synchronization signal (RAMP), the error amplifier output (EA), a current share bus (ISHARE), a
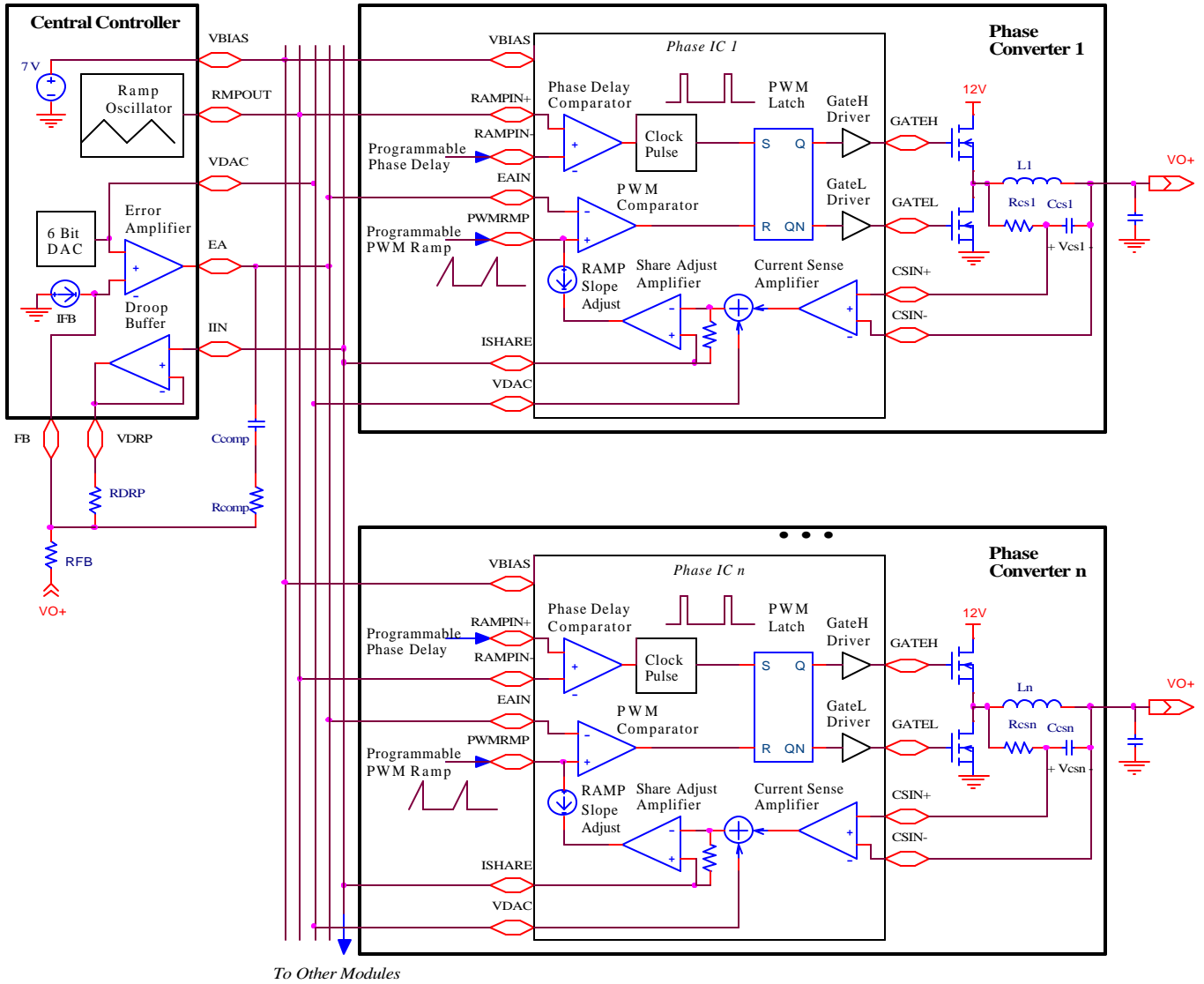
Fig. 1 Block diagram of the scalable multiphase buck converter

voltage reference (VBIAS) and the DAC voltage (VDAC). The phase controller consists of a phase delay comparator, a PWM comparator and latch, high and low side gate drivers, a current sense amplifier and a current share adjust amplifier. Because of its small size, the phase controller can be placed adjacent to the power stage, simplifying layout. Most importantly, the current signal is amplified locally thereby increasing noise immunity, adaptive voltage positioning and current sharing accuracy.

The architecture utilizes feed-forward voltage mode control which inherently has fast response to input voltage variation and provides fast output load step response due to the high speed error amplifier.

Current sharing among the distributed phase converters is achieved through an average current share loop. A voltage representing current information of each phase is connected to the share bus through a resistor. This provides an average voltage on the share bus that represents the average module current. Each phase controller's shares adjust amplifier compares the current of its phase with the average current of the share bus and adjusts the slope of the PWM ramp which in turn controls the duty cycle to minimize the difference of the current in each phase. The share bus can also be used to enable current sharing between VRMs in applications that require even higher current. The bandwidth of the current share loop is chosen to be lower than that of the voltage loop so that the two loops do not interact.

Loss-less inductor current sensing, shown in Fig. 1, is used in the phase converters due to its low implementation cost, reasonable accuracy, and efficiency savings [5]. The time constant of the resistor R_{CS} and capacitor C_{CS} across the inductor is usually chosen to match the time constant of the

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inductor L and its DC resistance R_L. The voltage across the capacitor C_{CS} is proportional to the voltage drop of the DC resistance of the inductor, and therefore V_{CS} represents the inductor current. To compensate the inductor DCR's +0.385 %/°C rate of change with temperature, the phase IC's current sense amplifier (CSA) gain has a built-in negative temperature coefficient [4]. Due to the vicinity of the distributed phase controllers to the inductors, the phase controllers provide more accurate temperature compensation for the inductor DCR change comparing to the central controller far away from the inductors.

The control IC generates a triangular waveform (RAMP) which is used to program the phase delay of the interleaved phase converters, as shown in Fig. 2. The ramp signal is connected to the non-inverting input (RMPIN+) of the phase delay comparator if phase activation is desired on the up-slope of the RAMP signal. At the inverting input (RMPIN-) of the phase delay comparator, the delay time is programmed by selecting the DC voltage which is created with a simple resistor divider connected to VBIAS pin. The RAMP generator in the control IC is also powered by VBIAS and therefore RAMP magnitude tracks VBIAS voltage, which eliminates the effect of the VBIAS voltage error on the phase delay time. Phase activation on the RAMP down-slope is easily achieved by swapping the phase delay comparator inputs.
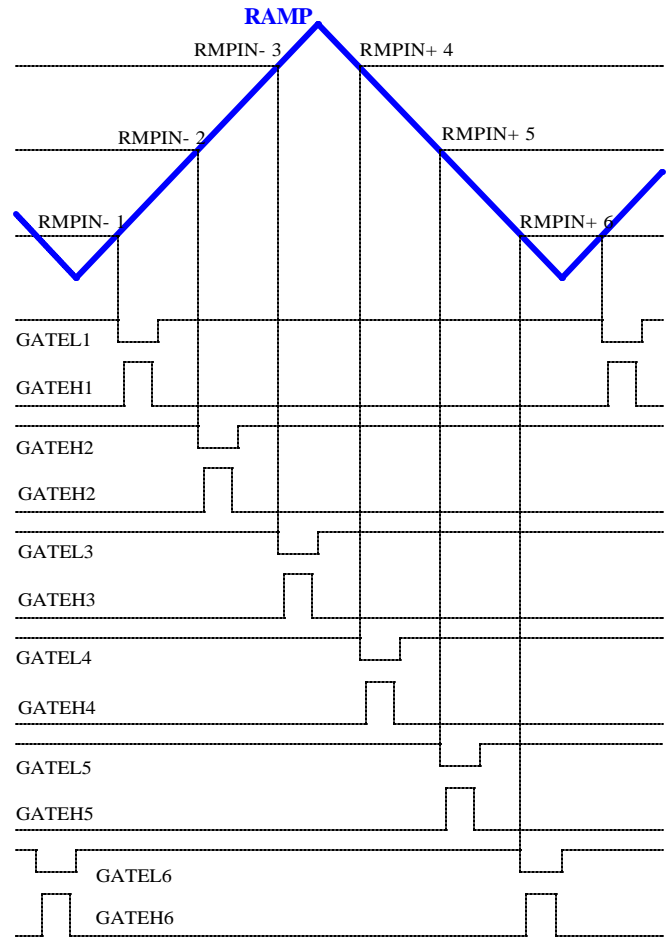

Fig. 2 Phase delay programming of a six phase interleaved converter

The advantage of this phase delay programming method is that the oscillator frequency of the central controller equals the phase switching frequency instead of the effective switching frequency (phase number times the phase switching frequency). This makes it possible for the IC to control more phases at higher frequency and provides phase delay time flexibility which is necessary in programming any number of the phases.
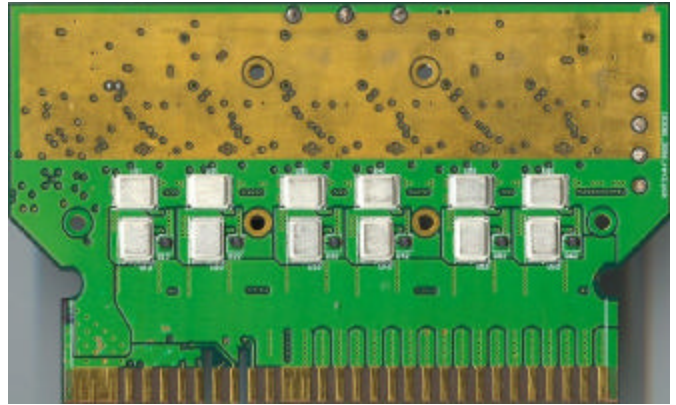
III. EXPERIMENT

Fig. 3 on the next page shows the experimental circuit of a six phase synchronous buck converter for server application. The maximum output current of the converter is 120 amperes, and the switching frequency is 300 kHz per phase. The phase number can be easily changed by enabling or disabling the phase converters, and the phase delay time is then changed according to the phase number selected.

Fig. 4 (a) and (b) show the pictures of the top side and bottom side of the six-phase VRM respectively. From left to right on the top side are phase one to phase six of the interleaved buck converter and the central controller. The heat sink is removed from the bottom side for a clear view of the DirectFet™ [6]. The gate driver voltage is provided to
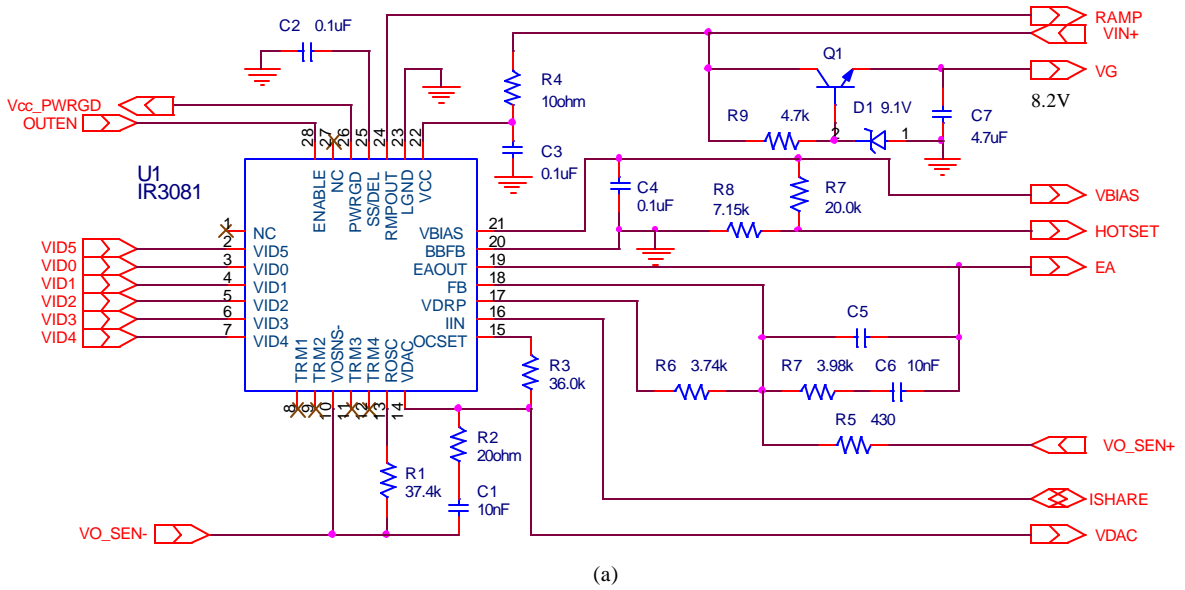
(a)

(b)

Fig 4. Voltage regulator module
(a) Top side; (b) Bottom side with heat sink removed
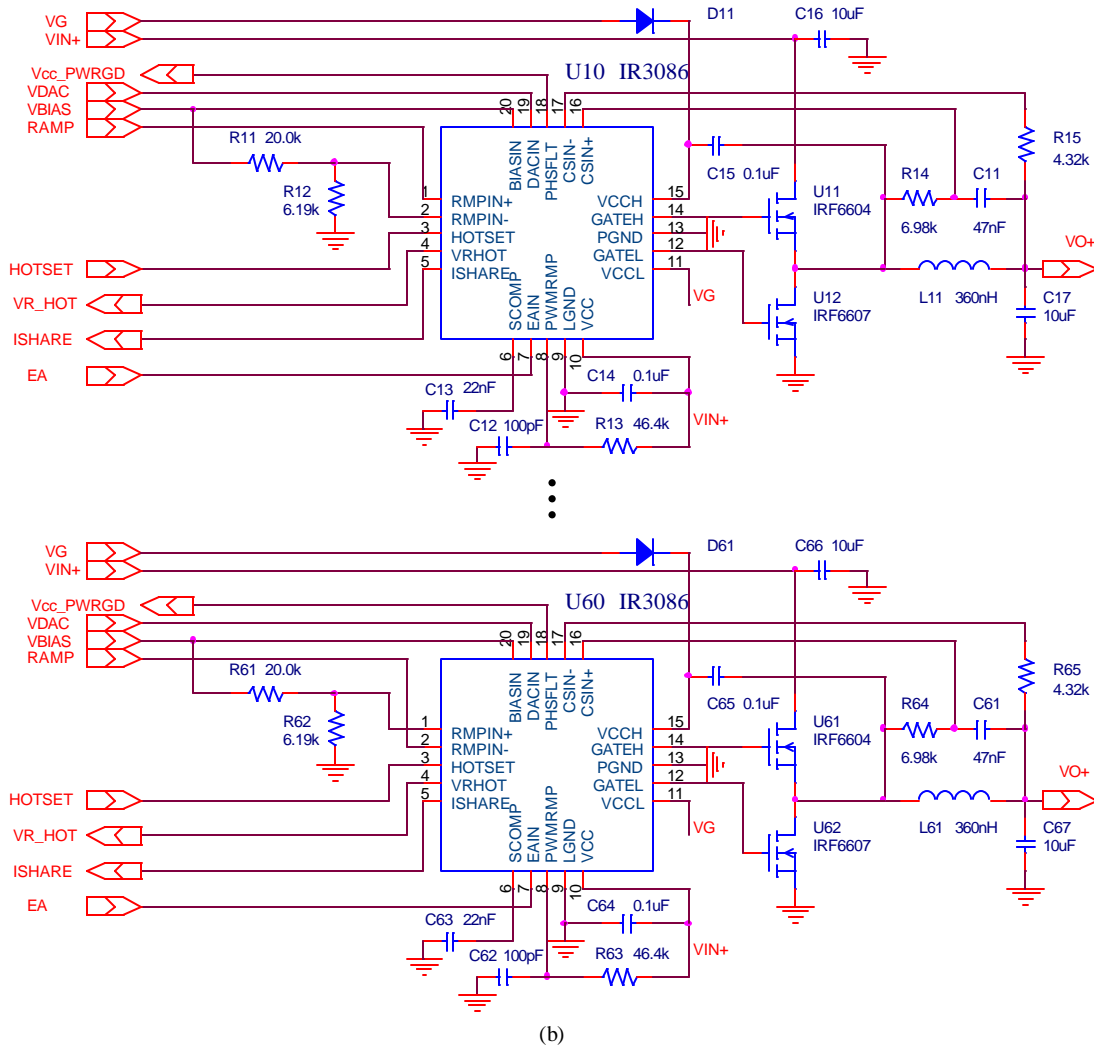

(a)

Fig. 3 Experimental circuit of the scalable buck converter
(a) Central controller   (b) Phase converters

optimize the efficiency of both control and synchronous MOSFETs. Because of their double side cooling property, the DirectFets are placed on the module's bottom side, where the heat sink is usually mounted. The new package of DirectFet reduces the $R_{DS(ON)}$ and thermal impedance dramatically making it possible to use just two MOSFETs in each phase.

Adaptive voltage positioning is used to lower the power loss of the microprocessor at heavy load and to reduce the voltage deviation during dynamic load conditions. Fig. 5 shows the output voltages at VRM and at the load, and the voltage difference is the voltage drop across the connector.

Fig. 6 shows the efficiency of the module programmed as four/five/six phases with the air flow of 400 Linear Feet per Minute (LFM). The output voltage is measured right at the module, and therefore the power loss of the VRM connector is not included. If the current is less than 30 amperes, the efficiency is higher for less phase number. When the current is above 30 amperes, the efficiency drops with reducing phase numbers, since the conduction loss of the MOSFETs dominates with this switching frequency.
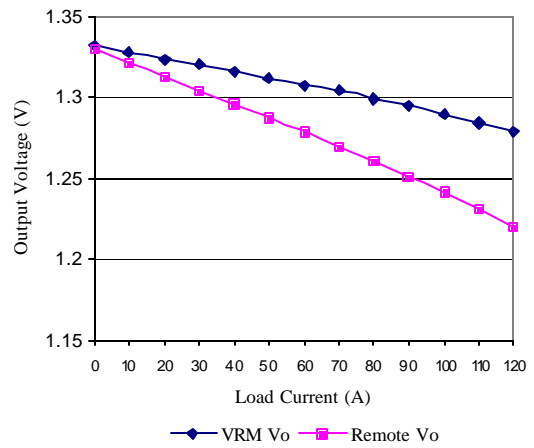

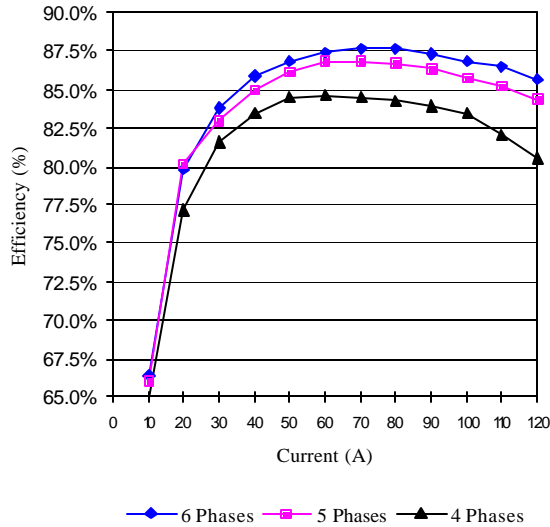Fig. 5 Output voltage at different load current

Fig. 6 Efficiency of the four/five/six phase VRM
Vi=12V, VDAC=1.35V, fsw=300kHz per phase
Air flow = 400 LFM

Fig.8 Current sharing during soft start
Ch1: Output voltage (1V/div)
Ch2-Ch4: SCOMP1-SCOMP3 (100mV/div)
Time (1mS/div)

Fig. 7 shows the current sharing performance of the six phase converter in the steady state. The difference between the average current and the phase current of any phase is within +/-0.5 amperes in the whole load range, and the maximum current sharing error at full load is smaller than 5%.

Fig. 8 shows the current sharing during soft start. The SCOMP pin voltage is pre-charged close to the threshold of the share adjust amplifier, so that the current share loop responds without any delay after the converter is enabled.
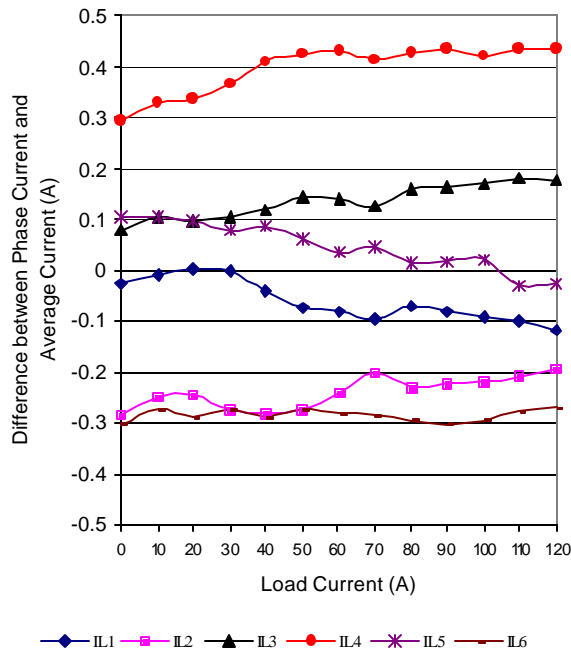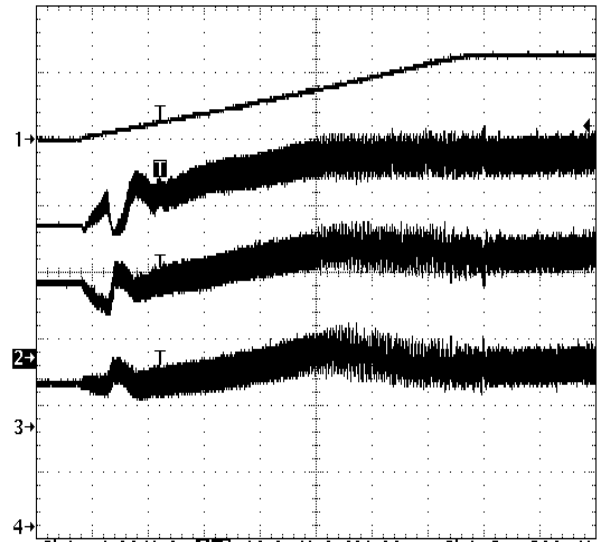
IV.   CONCLUSIONS

The scalable buck converter meets the tight requirements of the next generation microprocessors and facilitates the design trade-off of the multiphase converter. The distributed IC architecture improves the PCB layout, lowers the parasitic impedance of the gate driving paths, reduces the noise coupled to the current signal, and provides more accurate temperature compensation to the inductor DCR change. The average current share loop in the scalable converter ensures the current sharing accuracy of the distributed converters and paralleled modules. The scalable converter concept can be extended to other applications which require higher current or multiple output voltages.

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Fig. 7 Steady state current sharing of the six phase converter

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