

# Article A Self-Powered Dual-Stage Boost Converter Circuit for Piezoelectric Energy Harvesting Systems

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**Abstract:** Miniaturised piezoelectric devices are emerging energy harvesting sources that are appropriate for various implantable and wearable applications. However, these piezoelectric devices exhibit considerable internal resistance due to their internal impedance, which leads to self-start and low-energy conversion failures. This paper describes a dual-stage boost converter circuit by facilitating self-powering features and boosting the low voltage harvested by the piezoelectric devices into dc. The proposed circuit comprises conversion stages of ac-dc and dc-dc in Stages I and II, respectively. In addition, the proposed circuit does not require employing the auxiliary circuits to generate the train pulses by triggering the bidirectional switches to envelop the current being stored in Stage II and kick-start the self-powered circuit for piezoelectric energy harvesting systems. Theoretical assumptions and control strategies were tested and verified with ideal and impedance input sources. The proposed circuit could convert a low voltage of 3 V<sub>ac</sub> into 19 V<sub>dc</sub>. The maximum attained output power by the proposed circuit was 3.61 mW. The outcome depicted that the proposed circuit voltage and outperformed the existing literature circuits in terms of output voltage and power.

**Keywords:** piezoelectric energy harvesting; voltage doubler; boost converter; self-powered voltage boost converter; ripple reduction; rectifier

# 1. Introduction

The global energy demand has increased substantially in the past few decades, primarily due to the growing world population and the economic development of world-leading countries. Thus, researchers consistently develop renewable energy sources to limit the dependency on conventional energy sources. A comprehensive range of renewable energy sources is available in the environment, comprising solar [1], wind energy [2], thermal energy [3], and mechanical energy [4,5]. However, suitable energy harvesting and conversion systems are required to effectively utilise these available energy sources. One such system is piezoelectric energy harvesting, which is a mechanical vibration-based energy harvesting methodology used for harvesting electrical energy as alternating current/voltage (ac) from the ambient vibrations, which are readily available in the environment. A piezoelectric device is used to convert from mechanical energy to ac.

Apart from the device itself, a conventional piezoelectric energy harvesting system comprises three fundamental aspects: a mechanical system an electrical interface circuit [6], and a storage battery [7]. A flow diagram illustrating the piezoelectric energy harvesting system procedures is shown in Figure 1.

As the piezoelectric device is placed on a mechanical system, it harvests ac when it is subjected to excitation, while the storage devices (i.e., batteries, capacitors) require direct current/voltage (dc). Thus, the piezoelectric energy harvesting process necessitates the



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**Copyright:** © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). conversion process of ac-dc (i.e., rectification). Such conversion requires a power electronics circuit, namely, a rectifier circuit. Thus, the rectifier circuit is placed among the piezoelectric device and storage devices for rectification.



Figure 1. A conventional piezoelectric energy harvesting system.

In the literature, researchers have proposed various types of rectifier circuits, including active- and passive-based power conversion circuits [8] and power conditioning circuits for piezoelectric energy harvesting [9]. These include linear, non-linear and impedance matching circuits for overcoming the shortcomings of the conversion (i.e., ac-dc) process (such as switching losses and power conversion losses), which resulted due to the piezoelectric device's low voltage and its internal characteristics. However, the primary method is the full-bridge rectifier circuit [10], which comprises four diodes [11]. Despite its simplicity and flexibility, the full-bridge rectifier circuit possesses a significant drawback: forward voltage [12]. Thus, the output voltage ( $V_{dc}$ ) and power through the full-bridge rectifier circuit were limited [13]. However, most power electronic devices require 3.3  $V_{dc}$ . Thus, there is a necessity for a power electronic circuit that enables two features [14], namely, ac-dc and boosting low voltage into high voltage.

To address the drawbacks (i.e., the limited output voltage and power), ref. [10] proposed an H-Bridge rectifier circuit. The H-Bridge rectifier circuit comprised bidirectional switches and was proposed to transform the ac harvested by the piezoelectric device into dc by minimising forward voltage drop losses of conventional diodes in the full-bridge rectifier circuit. The intended circuit was tested successfully at high- and low-frequency vibrations. Nevertheless, the resulting outcome of the H-Bridge rectifier circuit was limited, and the boundary conditions were not well defined.

Later, to overcome this low-output voltage ( $V_{dc}$ ), [15] modified a single-stage H-Bridge rectifier circuit into a dual-stage H-Bridge rectifier circuit. The proposed circuit successfully converted the low ac harvested by the piezoelectric device into high dc voltage ( $V_{dc}$ ) by employing the switching process in its Stage II operation. The practical credibility of the proposed circuit was tested in two scenarios: the shaker and human motion tests. The results showed that the proposed circuit successfully charged a 1.2  $V_{dc}$ , 4 mA solar battery in less than 30 min. However, the circuit experienced higher power losses due to its complexity in Stage II. In addition, the proposed circuit employed auxiliary components such as Zener diodes and ICs, which led to high conversion losses.

Another study on bridgeless rectifier circuits was conducted by [16] to minimise the diode's forward voltage losses in the conventional bridge rectifier circuit. The proposed circuit employed a limited number of components to reduce the circuit's power dissipation. It was tested using a series of simulations and experimental scenarios. The outcome showed that the proposed circuit achieved 1.4 times more output power than the bridge rectifier. Nevertheless, the circuit employed an auxiliary power supply to enable the switching phenomena, which made this design impractical in real-life applications.

Another methodology for achieving maximum output power is employing a nonlinear system with external switches as an MOSFET (metal-oxide-field-effect-transistor), duty cycles, switching frequency, and passive electronic components, such as capacitors and inductors. A variety of non-linear approaches were proposed, including synchronous charge extraction [17], synchronized switching harvesting on inductors [18], a self-powered sequential switching harvesting on inductors [19], a single-pulse integrated circuits-based energy harvester [20], synchronous electric charge extraction [21], parallel sequencing switching harvesting on inductors, inductor-less dc-dc converter circuits [22], the sequential switching and synchronous charge extraction-based technique [23] and the synchronous charge extraction technique [24]. However, the prior proposed circuits embodied auxiliary circuits, such as diodes, transformers and bulky inductors, which are unsuitable for piezoelectric energy harvesting applications due to their high energy losses. Another approach, synchronised switching harvesting techniques, was proposed by [18,25,26]. Compared to the full-bridge rectifier circuit, the proposed circuit improved and enhanced the ac to high dc (i.e., output voltage). However, the proposed methodology adopted additional components: a polarity detector, an oscillator, diodes, a controller, logic gates and transformers. Due to this, the ac-dc conversion losses and power consumption across circuit elements are higher compared to the power generated by the piezoelectric device. In addition, the circuit required a high voltage to initiate the conversion process.

Later, [27] proposed a rectifier-less ac-dc conversion circuit by employing the synchronous process by using an inductor. A cold startup feature is introduced to the proposed circuit to achieve the optimised output from the proposed circuit. The circuit achieved a gleaning output power of 254  $\mu$ W at a 0.65 mV<sub>ac</sub> input voltage. However, the proposed circuitry is unsuitable, as it demands auxiliary components, such as three piezoelectric devices, three capacitors, a logic controller, an inductor and a polarity detector. Thus, the proposed circuit utilised high power and inflexibility in the PEH applications.

While the piezoelectric device generates low voltage, and the conventional full-bridge rectifier includes forward voltage issues. Most power electronic applications require  $3.3 V_{dc}$ . The previously published literature highlighted that most researchers focused on rectification and boosting in their proposed circuits, which results in high power consumption and stress between the switches and parasitic components. In addition, most literature circuits require auxiliary electronic components such as polarity indicators, duty cycles, logic gates and controllers [28] to operate the circuit effectively. Therefore, a more suitable electronic circuit needs to fill the previously stated literature gap linked to boosting the low ac voltage harvested by the piezoelectric device into high dc, which results in less power consumption, less stress between the switches and no utilisation of parasitic components during the switching process.

Therefore, to avoid these drawbacks, the authors developed the two-stage conversion process circuit by garnering the combinations of the conventional voltage doubler [18,26,28,29] and the literature switching circuits [27,29,30].

The proposed dual-stage boost converter circuit employs minimal components to reduce conversion losses through a two-stage operation system. Stage I involves a voltage doubler [18,26,28,29] circuit for ac-dc conversion, while Stage II involves a dc-dc step-up voltage converter for voltage amplification. Other key benefits of the dual-stage boost converter circuit are highlighted below:

- 1. The proposed circuit implemented a single MOSFET switch. This reduced stress in the switching process, thus achieving a higher output voltage (V<sub>dc</sub>) and power.
- 2. As highlighted in the literature, it is developed without employing complex, extraneous circuits and polarity indicators, which leads to lower conversion losses and complexity.

A comprehensive description of the dual-stage boost converter circuit is discussed in the subsequent sections.

# 2. Piezoelectric Energy Harvesting Circuits

This segment describes the inner features of the mechanically vibrated piezoelectric device employed in the piezoelectric energy harvesting system. Subsequently, the theoretical analysis and operations of both the voltage doubler and proposed dual-stage boost converter circuits are also explained.

### 2.1. Internal Circuit of a Piezoelectric Device

When a piezoelectric device is mechanically excited, it harvests AC voltage ( $V_{ac}$ ), comprising positive and negative half-cycles, across its electrodes. This piezoelectric device can be considered a sinusoidal current source parallel to its internal capacitor ( $C_P$ ) and resistor ( $R_P$ ). This is graphically represented in Figure 2a. Alternatively, it can also be demonstrated as a voltage source with the internal capacitor ( $C_P$ ) and resistor ( $R_P$ ) in the series configuration [31,32].



**Figure 2.** (**a**) Piezoelectric device as a current source and, (**b**) The voltage and current output of the piezoelectric device.

As it is considered a current source, it has to charge and discharge its internal capacitor before the piezoelectric device power flows through the electrodes. The representation of the current source and associated waveforms when the piezoelectric device is mechanically excited is represented in Figure 2. During the charging duration of the internal capacitor, no output is expected across piezoelectric device electrodes. This region is called a non-harvesting region, while the remaining period is called a harvesting period. Since the ac includes both half-cycles, the abovementioned charging and discharging procedures occur in both half-cycles. The non-harvesting region is denoted in the intervals of 1 and 3 in the time periods of  $t_{0-1}$  and  $t_{2-3}$ , whereas the harvesting period is denoted in the intervals of 2 and 4 in the periods of  $t_{1-2}$  and  $t_{3-4}$  in both half-cycles, respectively [15,18,32,33]. The complete working operation of the piezoelectric device in both half-cycles is explained in Table 1.

The harvested piezoelectric device's current ( $i_{ac}$  (t)) due to mechanical excitations can be expressed as:

$$i_{ac}(t) = I_{ac} \sin(\omega t)$$
(1)

where  $\hat{I}_{ac}$  is the magnitude of the harvested current,  $\omega$  is the angular frequency, while t represents the time period.

Electronic Cincuito	Mode 1: Positive Half-Cycle		Mode 2: Negative Half-Cycle		
Electronic Circuits	Interval 1	Interval 2	Interval 3	Interval 4	
Piezoelectric device	When $t_o < t \le t_1$ • $C_P$ : Charging • $C_L$ : Not charging		When $t_2 < t \le t_3$ • $C_P$ : Charging • $C_L$ : Not charging	When $t_3 < t \le t_4$ • $C_P$ : Discharging • $C_L$ : Charging	
Voltage doubler	$ \begin{array}{ll} \mbox{When } t_o < t \leq t_1 \\ \bullet & C_P : \mbox{Charging} \\ \bullet & D1 : \mbox{OFF} \\ \bullet & D2 : \mbox{OFF} \\ \bullet & C_L : \mbox{Not charging} \end{array} $	$ \begin{array}{l} \mbox{When } t_1 < t \leq t_2 \\ \bullet  C_P : \mbox{Discharging} \\ \bullet  D1 : \mbox{ON} \\ \bullet  D2 : \mbox{OFF} \\ \bullet  C_L : \mbox{Charging} \end{array} $	$ \begin{array}{ll} \mbox{When } t_2 < t \leq t_3 \\ \bullet & C_P : \mbox{Charging} \\ \bullet & D1 : \mbox{OFF} \\ \bullet & D2 : \mbox{OFF} \\ \bullet & C_L : \mbox{Not charging} \end{array} $	$ \begin{array}{ll} \mbox{When } t_3 < t \leq t_4 \\ \bullet & C_P : \mbox{Discharging} \\ \bullet & D1 : \mbox{OFF} \\ \bullet & D2 : \mbox{ON} \\ \bullet & C_L : \mbox{Charging} \end{array} $	

Table 1. Working intervals of a piezoelectric device and voltage doubler.

#### 2.2. Voltage Doubler Circuit

A voltage doubler circuit [18,18,26,28,29] and its associated current and voltage waveforms are illustrated in Figure 3. During intervals 1 and 3, the internal capacitance of the piezoelectric device gets charged in each half-cycle (positive and negative), and no current is conducted towards the load capacitor ( $C_L$ ). Hence, the voltage doubler circuit is OFF, which can be observed as the shaded region (Figure 3b).

However, once the internal capacitance is fully charged, the current  $i_{ac}$  (t) starts flowing towards the load capacitor ( $C_L$ ) and starts charging it. During this interval, the voltage doubler starts conducting, which can be observed as the non-shaded region in intervals 2 and 4 (Figure 3b).

As a result of the voltage doubler's operation, the capacitor ( $C_L$ ) gets charged. The working operation of the voltage doubler circuit in both half-cycles can be observed in Table 1.



Figure 3. (a) A voltage doubler circuit and, (b) The associated current and voltage waveforms.

### 2.3. Operation Modes of the Dual-Stage Boost Convereter Circuit

In this research, a dual-stage boost converter circuit is proposed to alleviate the drawbacks of traditional circuits. The proposed circuit in Figure 4a is designed to function in two stages (I & II) and includes four modes. Stage I involves the operation of the voltage doubler circuit for ac-dc conversion, while Stage II comprises a dc-dc step-up voltage converter to boost the stored dc voltage ( $V_{dc}$ ) in C<sub>3</sub> in Stage I. As the dual-stage boost converter circuit is the continuation of the voltage doubler circuits are expected to be the same. As a result, the working operation of Modes 3 and 4 (Stage II) is only described in this section. It should be noted that the operations of Modes 3 and 4 (Stage II) start when Stage I's operation fully charges the capacitor (C<sub>3</sub>).

Stage II comprises two modes of operation, 3 and 4. Mode 3 starts working when the MOSFET switch  $(M_1)$  is switched ON, while Mode 4 begins when the MOSFET switch  $(M_1)$  is switched OFF. The complete working operation in both modes is depicted as Figure 4b,c, respectively.



**Figure 4.** (**a**) Proposed dual-stage boost converter circuit, (**b**) When the MOSFET switch (M<sub>1</sub>) is ON, (**c**) When the MOSFET switch (M<sub>1</sub>) is OFF.

# **Mode 3:** (When the MOSFET switch $(M_1)$ is ON)

Initially, the stored voltage in the capacitor ( $C_3$ ) passes through the inductor ( $L_1$ ) and flows towards the base (B) of the transistor ( $Q_1$ ) via the coupling capacitor ( $C_4$ ). It is worth noting that the transistor  $Q_1$  behaves as a voltage amplifier that amplifies a low voltage at the base (B) terminal to a higher output voltage at the collector (C) terminal.

This collector output triggers the gate (G) terminal of the MOSFET ( $M_1$ ) and consequently turns on  $M_1$ . At this point, the accumulated voltage in the capacitor ( $C_3$ ) flows through the inductor ( $L_1$ ), leading to a gradual increase in the inductor ( $L_1$ ) current from zero to peak because the inductor resists a rapid change in current. The diode ( $D_4$ ) is reverse-biased during this time, and no current flows to the load capacitor ( $C_L$ ). Figure 4b illustrates the current flow during Mode 3, when the  $M_1$  is in the ON state.

# **Mode 4:** (When the MOSFET switch $(M_1)$ is OFF)

When the  $L_1$  is fully saturated in this Mode, it stops the current flow towards the transistor ( $Q_1$ ) and turns the  $M_1$  OFF. Thus, the stored current in the  $L_1$  is freewheeled via the diode ( $D_4$ ) and starts charging the load capacitor ( $C_L$ ). Because the capacitor resists a rapid change in voltage, it charges slowly from zero to peak value. Figure 4c demonstrates the current flow during Mode 4, when the  $M_1$  is in the OFF state. A brief operation of Modes 3 and 4 is shown in Table 2.

It is worth emphasising that Stage II does not necessitate an auxiliary power source to trigger the dc-dc step-up voltage converter. Thus, switching pulses, logic gates, and integrated circuits [28] are not required to operate the proposed circuit's MOSFET switch ( $M_1$ ).

Dual-Stage Boost Converter Circuit	Mode 3	Mode 4	
Stage II	M <sub>1</sub> : ON L <sub>1</sub> : Charging D <sub>4</sub> : OFF C <sub>L</sub> : Discharging	M <sub>1</sub> : OFF L <sub>1</sub> : Discharging D <sub>4</sub> : ON C <sub>L</sub> : Charging	

Table 2. Working modes of Stage II.

As the proposed research emphasises, the piezoelectric energy harvesting systems, regarding the rectification process, the output voltage  $(V_{dc})$  and the power through the proposed circuit, are chosen to validate its practical credibility. Additionally, the calculated output power of the proposed circuit is compared with an existing published literature circuit. It should be noted that the prime objective of the proposed and previously published energy harvesting circuits is to extract a higher output voltage  $(V_{dc})$  and power. As a result, the output voltage  $(V_{dc})$  and power are only shown in this study. The average input power  $(P_{ac})$  harvested by the vibrating piezoelectric device was calculated as [18,27,28]:

$$P_{ac} = \frac{V_{Pk}}{\sqrt{2}} \cdot \frac{I_{Pk}}{\sqrt{2}} \cos \phi$$
(2)

where  $I_{Pk}$  and  $V_{Pk}$  are the peak current and voltage, while  $\varphi$  is the phase angle between the current and voltage in the piezoelectric device.

Moreover, the output power ( $P_{OUT}$ ) of the dual-stage boost converter circuit was calculated by multiplying the value of current ( $I_L$ ) through the load resistor ( $R_L$ ) and voltage ( $V_L$ ) across the load capacitor ( $C_L$ ):

$$P_{OUT} = V_L \times I_L \tag{3}$$

#### 3. Simulation Study

This simulation study was conducted to investigate the theoretical validation of the dual-stage boost converter circuit. LTSpice [15,18,18,22,34] software was employed in this study. Using LTSpice, an ideal ac voltage source is selected as an input and applied to the boost circuit. This input is chosen to emulate the piezoelectric device's output for testing the proposed circuit. However, later, the ideal ac voltage source was exchanged with the piezoelectric device in the experiments.

Additionally, to validate the performance capability of the proposed circuit, both ideal and piezoelectric device inputs were chosen. The acquired results from LTSpice using an ideal ac voltage source were considered proof of the concept. In LTSpice, a 5 V, 50 Hz sinusoidal waveform was chosen as the input ideal ac voltage source. The simulation model of the proposed circuit at 5 V<sub>ac</sub> and a 50 Hz frequency is depicted in Figure 5.

The adopted electronic components and their parameters for the proposed circuit are described in Table 3.



Figure 5. Simulation model of the dual-stage boost converter circuit.

Table 3. Components Table.

Part	Description			
1 dit	Туре	Reference		
V <sub>ac</sub>	Voltage source	5 V, 50 Hz		
R <sub>1</sub>	Resistor	75 ΚΩ		
R <sub>2</sub>	Resistor	200 Ω		
R <sub>L</sub>	Load Resistor	100 Ω		
C <sub>1</sub> -C <sub>2</sub>	Capacitor	2.2 uF		
C <sub>3</sub>	Capacitor	330 pF		
C <sub>L</sub>	Load Capacitor	500 uF		
$D_1-D_4$	Schottky diode	1N5819		
M <sub>1</sub>	N-MOSFET	BSZ0920NS		
Q1	NPN-Transistor	2N3904		
L <sub>1</sub>	Inductor	4.7 uH		

Figure 6 demonstrates the adopted ideal ac voltage source. A comprehensive zoom-in view of the ON and OFF periods of the MOSFET switch ( $M_1$ ), as discussed in section II, is illustrated in Figure 7. As a result of MOSFET switching, the inductor gets energised and de-energised, which is depicted in Figure 8. In addition, the charging and discharging of load capacitors ( $C_L$ ) are illustrated within the context of Figure 9.



Figure 6. Ideal ac voltage source.



Figure 7. ON and OFF period of the MOSFET switch (M<sub>1</sub>).



Figure 8. Energising and De-energising process of the inductor (L<sub>1</sub>).



Figure 9. Charging and discharging process of the load capacitor (C<sub>L</sub>).

# 4. Experimental Study

In both testing scenarios (at a constant voltage (Test 1) and a constant frequency (Test 2)), an MFC-M2814-P2 patch (37 mm  $\times$  17 mm  $\times$  0.180 mm, internal capacitance: 30.79 nF) was used as a piezoelectric device. The piezoelectric device patch was glued on the surface of an aluminium cantilevered beam (Dimensions: 205 mm  $\times$  20 mm  $\times$  1 mm) at the fixed end, while two permanent magnets were coupled on the free end, acting as a proof mass. A voltmeter and ammeter [CD 771] were used to measure the output voltage (V<sub>dc</sub>) and current, respectively.

To generate an input ac voltage ( $V_{ac}$ ) from the piezoelectric device, a function generator (Agilent 33210A) was utilised, which was attached to the power amplifier (2706, B&K Agilent). This combination boosted the ac voltage ( $V_{ac}$ ) from the piezoelectric device before applying it to the mechanical shaker (APS-113). This mechanical shaker induced harmonic vibrations based on the given input amplitude and frequency to shake the cantilevered beam incorporated with a piezoelectric device. The frequency and amplitude at which the piezoelectric device harvested mechanical vibrations were collectively adjusted through the function generator and power amplifier. When the harvested ac voltage ( $V_{ac}$ ) from the vibrating piezoelectric device was supplied to the dual-stage boost converter circuit, it conducted Stage I (ac-dc) and Stage II (dc-dc) operations.

In Tests 1 and 2, the harvested AC voltage ( $V_{ac}$ ) from the piezoelectric device through the proposed circuit was investigated using varying input parameters, as highlighted in Table 4. In Test 1, the proposed circuit was tested at a constant input voltage under varying frequencies. In Test 2, the proposed circuit was analysed at a constant frequency under a variable input voltage. The generated output voltage ( $V_{dc}$ ) through the dual-stage boost converter circuit was stored in  $C_L$  in both testing scenarios. In addition, each load resistor ( $R_L$ ) was connected in parallel, and the output was measured using a multimeter. An experimental setup of the proposed circuit is depicted in Figure 10.



1. Function generator, 2.Amplifier, 3.Mechanical shaker, 4. PD, 5.Cantilevered Beam, 6.Proof Mass, 7.DSBC circuit, 8.Oscilloscope, 9. Ammeter and Voltmeter

Figure 10. Experimental setup of the proposed circuit.

Table 4. Testing Sources.

Sources of Excitation	Test Scenarios	Frequency (Hz)	Input Voltage (V <sub>ac</sub> )	Type of Piezoelectric Device	Load Resistors (KΩ)
Mechanical Shaker	Test 1	1, 2, 3, 4, 5 10, 20, 30, 40, 50	5 3	MFC	$\begin{array}{l} R_1 = 100 \\ R_2 = 300 \\ R_3 = 620 \\ R_4 = 910 \end{array}$
	Test 2	1, 2	1, 2, 3, 4, 5	-	

#### 4.1. Test 1: Varying Excitation Frequency under a Constant Input Voltage

The output voltage ( $V_{dc}$ ) and power obtained from Test 1 are highlighted in Figure 11a,b, respectively. The dotted line represents the voltage doubler circuit, while the solid line indicates the dual-stage boost converter circuit. The output voltage ( $V_{dc}$ ) and power from both the proposed and voltage doubler circuits are compared under varied input frequencies (10–50 Hz) and load resistances ( $R_L$ ).

By analysing Figure 11a, it can be regarded that the output voltage ( $V_{dc}$ ) increases substantially by increasing the value of load resistances from 100 K $\Omega$  to 910 K $\Omega$ . Irrespective of the excitation frequency, the proposed circuit yielded a higher output voltage ( $V_{dc}$ ) than the voltage doubler circuit under a constant input voltage (3  $V_{ac}$ ). It is to be noted that the proposed circuit achieved a higher output voltage ( $V_{dc}$ ) at a higher load resistance ( $R_L$ ).

Initially, a 3  $V_{ac}$  input voltage was given to the proposed circuit at an excitation frequency of 10 Hz. Consequently, Stage I conducted ac-dc conversion, and the output voltage ( $V_{dc}$ ) was stored in the capacitor ( $C_3$ ) (Figure 4a). It should be noted that Stage II does not operate unless Stage I fully charges the capacitor ( $C_3$ ). When it is fully charged, it stimulates the current flow in Stage II.



Figure 11. Outcomes of Test 1 at 3 Vac: (a) Output voltage (Vdc) and (b) Output power.

The stored charge in the  $C_3$  passed through the  $L_1$  and flowed towards the base of the transistor ( $Q_1$ ) through the coupling capacitor ( $C_4$ ). This transistor ( $Q_1$ ) behaved as a Common Emitter voltage amplifier, amplifying any input voltage at the base terminal to a higher output voltage at the collector terminal. This output at the collector terminal triggered the MOSFET's switch ( $M_1$ ) gate terminal, allowing for the current flow source from the drain and energising the inductor ( $L_1$ ).

Once the inductor  $(L_1)$  is fully saturated, it stops the current flow to the transistor  $(Q_1)$ . Consequently, the MOSFET switch  $(M_1)$  turned OFF. Thus, the stored charge in the inductor  $(L_1)$  forward-biased the diode  $(D_4)$  and started charging the load capacitor  $(C_L)$ . Afterwards, each load resistor from  $R_1$  to  $R_4$  was connected in parallel with the load capacitor  $(C_L)$ , and the respective output voltages  $(V_{dc})$  were measured.

Later, the remaining excitation frequencies (20–40 Hz) were applied under a similar input voltage (3 V<sub>ac</sub>), and the resulting output voltage (V<sub>dc</sub>) for each load resistor (R<sub>L</sub>) (R<sub>1</sub>–R<sub>4</sub>) was measured (Figure 11a). In addition, the output power was calculated using Equation (3) by measuring the voltage (V<sub>L</sub>) across the load capacitor (C<sub>L</sub>) and the current through the load resistor (R<sub>L</sub>). Figure 11b shows the output power under various excitation frequencies and a fixed input voltage. It is noted that the output power shows a different trend as compared to the output voltage (V<sub>dc</sub>) at various load resistances (R<sub>L</sub>). This is because the harvested current through each load resistor (R<sub>L</sub>) was different. Thus, the calculated output power was dissimilar.

By further examining Figure 11, it can be observed that the excitation frequency substantially impacts the proposed circuit's overall performance. The output voltage ( $V_{dc}$ ) and power were elevated at higher frequencies. The output voltage ( $V_{dc}$ ) and power at different excitation frequencies (10–50 Hz) with a constant input ac voltage ( $V_{ac}$ ) are depicted in Figure 12a,b, respectively. It should be noted that the proposed circuit yielded a higher output voltage ( $V_{dc}$ ) and power under higher excitation frequencies. This is due to the reason that, at higher frequencies, the capacitive reactance of the piezoelectric device decreases. As a result, the piezoelectric device generates a higher ac voltage ( $V_{ac}$ ), leading to a higher output voltage ( $V_{dc}$ ) and power.

It should be noted that the prime goal of this research is to validate the performance of the proposed circuit to track the optimal points and power dependency on the frequency under varying load resistances and the attainment of the maximum output voltage ( $V_{dc}$ ) and power at a frequency of 50 Hz at 3  $V_{ac}$ .



**Figure 12.** Outcomes of Test 1 at various excitation frequencies: (a) Output voltage ( $V_{dc}$ ) and (b) Output power.

# 4.2. Test 2: Varying Input Voltage under a Constant Excitation Frequency

In this testing scenario, the dual-stage boost converter and the voltage doubler circuits were further analysed under varying input voltages ( $V_{ac}$ ). The frequency was kept constant at 1 Hz. The vibrating piezoelectric device's ac voltage ( $V_{ac}$ ) was chosen from 1  $V_{ac}$  to 5  $V_{ac}$ . A voltmeter was utilised to measure the harvested  $V_{ac}$  from the vibrating piezoelectric device before applying it to the proposed circuit. A detailed summary of the different investigated parameters is reported in Table 4. Figure 13a,b represent the results of the output voltage ( $V_{dc}$ ) and power from Test 2. The dotted line represents the voltage doubler circuit, while the solid line signifies the proposed circuit.



Figure 13. Outcomes of Test 2 at 1 Hz: (a) Output voltage (V<sub>dc</sub>) and (b) Output power.

Initially, 1 V<sub>ac</sub> from a vibrating piezoelectric device was applied across the proposed circuit. As the input ac voltage (V<sub>ac</sub>) was more significant than the threshold voltage of the transistor (Q<sub>1</sub>) and MOSFET (M<sub>1</sub>) switches, the proposed circuit started functioning, as explained in section IV-B. This resulted in achieving 0.36 V<sub>dc</sub>, which was stored in the load capacitor (C<sub>L</sub>). Similarly, when 3 V<sub>ac</sub> and 4 V<sub>ac</sub> were applied to the proposed circuit, 3.64 V<sub>dc</sub> and 5.35 V<sub>dc</sub> were achieved and stored in the load capacitor (C<sub>L</sub>). It should be noted that a higher output voltage (V<sub>dc</sub>) was achieved at a higher ac voltage (V<sub>ac</sub>) because when the applied ac voltage (V<sub>ac</sub>) increased, the drain to the source resistance path in the mosfet switch decreased [15,15,20,28,30]. Figure 11a illustrates the output voltages (V<sub>dc</sub>) from both circuits under various input ac voltages (V<sub>ac</sub>). It can be observed that the proposed circuit yielded a higher output voltage (V<sub>ac</sub>).

Next, the output power was measured at the load capacitor ( $C_L$ ) using Equation (3). The relation between the input ac voltage ( $V_{ac}$ ) and the output power at a 1 Hz excitation frequency is depicted in Figure 13b. A higher output power was accumulated at the load capacitor ( $C_L$ ) with an input voltage of  $4V_{ac}$ , while the least power was detected at 2  $V_{ac}$  at the load capacitor ( $C_L$ ) using the proposed circuit. It can be noticed that, at higher input ac voltages ( $V_{ac}$ ), the resistance in the drain to the source path of the MOSFET switch ( $M_1$ )

was decreased. As a result, a higher output voltage ( $V_{dc}$ ) is gathered in the load capacitor ( $C_L$ ), thus increasing the output power.

It was observed that the output voltage ( $V_{dc}$ ) increased with the enhancing load resistance (100–910 K $\Omega$ ). The highest output voltage ( $V_{dc}$ ) is obtained at 910 K $\Omega$ , while the lowest was observed at 100 K $\Omega$ . The behaviour was persistent for all input AC voltages ( $V_{ac}$ ) and complied with Ohm's law (Figure 13a). On the contrary, the behaviour of the output power with the increasing load resistance was different (Figure 13b). This might be due to the reason that the current flowing at different load resistors is different. Thus, the calculated output power was not consistent.

By further examining Figure 13, it is highlighted that the extent of the applied input ac voltage ( $V_{ac}$ ) substantially impacts the proposed circuit's overall performance. At a higher  $V_{ac}$ , the output voltage ( $V_{dc}$ ) and power became higher as well. The output voltage ( $V_{dc}$ ) and power at different input voltages ( $1 V_{ac}$ -5  $V_{ac}$ ) over a 1 Hz excitation frequency and at a 100 K $\Omega$  load resistor are depicted in Figure 14a,b, respectively.



**Figure 14.** Outcomes of Test 2 at various excitation frequencies: (a) Output voltage (Vdc) and (b) Output power.

It is worth mentioning that the proposed circuit outperformed the voltage doubler circuit, where the output voltage ( $V_{dc}$ ) and power generated by the proposed circuit are higher than the voltage doubler circuit in all scenarios. Considering that the principal objective of this study is to enhance the output voltage ( $V_{dc}$ ) and power, this is accomplished by using the proposed circuit. Table 5 lists the generated output power of similar circuits published in the previous literature.

It was found that the proposed circuit outperformed various previously published literature circuits regarding the output voltage and power.

Circuit Sources	No. of Piezoelectric Devices	Input Voltage (V <sub>ac</sub> )	DC Voltage (V <sub>dc</sub> )	Output Power (µ/mW)	External Power Supply
[35]	1	1.2	-	30 µW	YES
[36]	3	20	-	33 µW	YES
[15]	1	5	-	22 μW	NO
[27]	3	3.5	-	254 μW	YES
Proposed circuit	1	3	19	3.61 mW	NO

Table 5. Comparison of outputs of the circuits available in the previously published literature.

# 5. Conclusions

In this research, a self-powered dual-stage boost converter circuit was proposed and thoroughly studied to boost the low ac voltage generated by the piezoelectric device into dc in piezoelectric energy harvesting systems. The dual-stage boost converter circuit integrated a voltage doubler and a dc-dc boost converter as two stages (I & II) to function in both ac-dc and dc-dc conversion processes. In addition, it avoided the need for an expensive auxiliary circuit for effective operations. Due to using a single MOSFET, it reduced the stress across the switching process. In addition, the practical capability of the dual-stage boost converter circuit was verified using simulation and laboratory-based experiments. The proposed prototype converted a 3  $V_{ac}$  and 50 Hz input ac voltage ( $V_{ac}$ ) to 19  $V_{dc}$  and achieved an output power of 3.61 mW under Test 1. Moreover, it converted a 5  $V_{ac}$  and 1 Hz input ac voltage ( $V_{ac}$ ) to 10.9  $V_{dc}$  and achieved an output power of 0.396 mW under Test 2. The proposed circuit is proven to be exceptional compared to the existing literature circuits. The proposed circuit is suitable for the efficient energy conversion of vibrating piezoelectric devices for low-power portable/wireless devices. It is noted that the proposed circuit is limited to low-voltage applications only. For ultra-low voltages, the proposed prototype is not suitable, as the input voltage will be dissipated across circuit components, and there will be no output at the load. For future work, the modification of the dual-stage boost converter circuit to incorporate the non-linear process is recommended.

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