A Self-Tuning Resonant-Inductive-Link Transmit Driver Using Quadrature Symmetric Delay Trimmable Phase-Switched Fractional Capacitance

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***Abstract*— The efficiency of inductively coupled power transfer systems is increased when high-Q inductor–capacitor circuits are used, maximizing the magnetic field strength at the transmitter for a given drive amplitude. Such circuits require precise tuning to compensate environmental effects and component tolerances, which modify the resonant frequency. A single zero-voltage-switched fractional capacitance may be used to accurately tune the circuit to resonance, reducing implementation costs compared with classical tuning techniques. However, integration into a chip presents challenges, which must be addressed, such as operating with large voltage excursions and compensating for high-voltage driver delays. We describe here the operation of a self-tuning LC resonant circuit driver using a symmetrically switched fractional capacitance. An architecture for a fully integrated system for operation at 75 kHz–2.6 MHz is presented. Implemented in a 0.18-μm 1.8–50 V CMOS/laterally diffused MOSFET(LDMOS) technology, the integrated circuit uses high-voltage interfaces for capacitance switching and sampling inputs and includes digital phase trimming to compensate propagation delays in large driver devices. Correct operation of the self-tuning functionality is verified across the available frequency range, with results presented for static and dynamic tuning responses.**

***Index Terms*— Automatic tuning, inductive coupling, phase compensation, radio-frequency identification systems (RFID), resonant circuits, wireless power.**

I. Introduction

INDUCTIVELY coupled systems are becoming increasingly common in a wide range of applications; at one end of the scale, wireless charging systems are focused on power transfer, sometimes at very high levels [1]. A typical link topology is shown in Fig. 1. While much recent work has focused on receivers [2], [3], less consideration has been given to the transmit function. In radio-frequency identification systems (RFID), the magnetic field must create a large enough electromotive force to activate the receiver's rectifiers and provide sufficient power for the digital circuitry at the same time as transferring data, while some actively powered security systems merely demand that a remote receiver can detect the transmitted magnetic signal. Although the operational demands and power levels can vary considerably, a common feature is the need for the efficient generation of the magnetic field from the transmitter, leading to better power transfer and more tolerance of the separation distance between the transmit and receive sections.

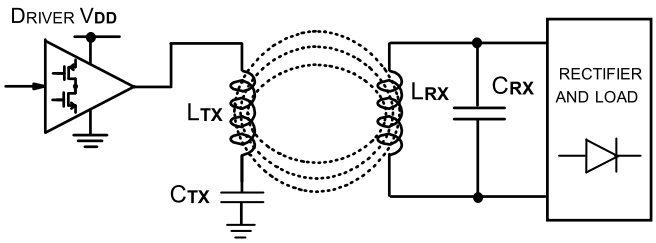

Fig. 1. Typical inductive coupling link topology.

Increasing the current in the transmit antenna coil can be achieved by simply using a larger drive voltage level, but there are practical restrictions on this strategy. The transmitter side power levels may be well limited and, in some applications such as automotive security or near-field communications, may be restricted by battery supplies. Hence, adopting a step-up voltage conversion to supply a driver is to be avoided. A better approach is to reduce the losses in the antenna coil and make the antenna coil resonant with a high quality factor (Q), so that a large circulating current can be achieved with a lower drive voltage.

High-Q antenna circuits are beneficial for several reasons. In addition to reducing the driver voltages and improving overall efficiency, the inherent filtering allows a high-efficiency switching driver to be used while reducing harmonics in the current waveform. However, the consequent associated narrow bandwidth of the antenna circuit now requires very precise tuning to maintain resonance. If the transmit frequency is fixed, any tuning technique must take into account not only of manufacturing tolerances and temperature effects, but also detuning due to a varying receiver load and possibly motion of nearby ferromagnetic structures.

This problem may be partially sidestepped in some applications by varying the excitation frequency [4]–[6], but this may not be permissible due to band allocation restrictions. Even if the excitation frequency can change enough to compensate for detuning of the transmitter, this approach transfers the tuning problem to the receiver, which in reality may be more challenging. It is common for the receiver to be a very low

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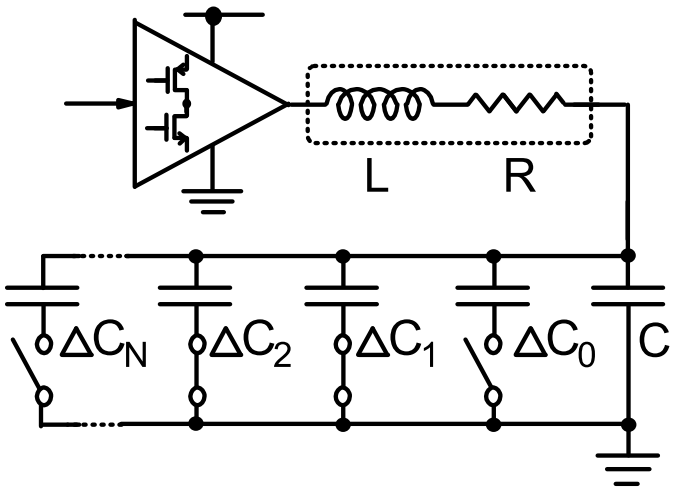

Fig. 2. *LC* resonant circuit tuning with weighted-capacitor array.

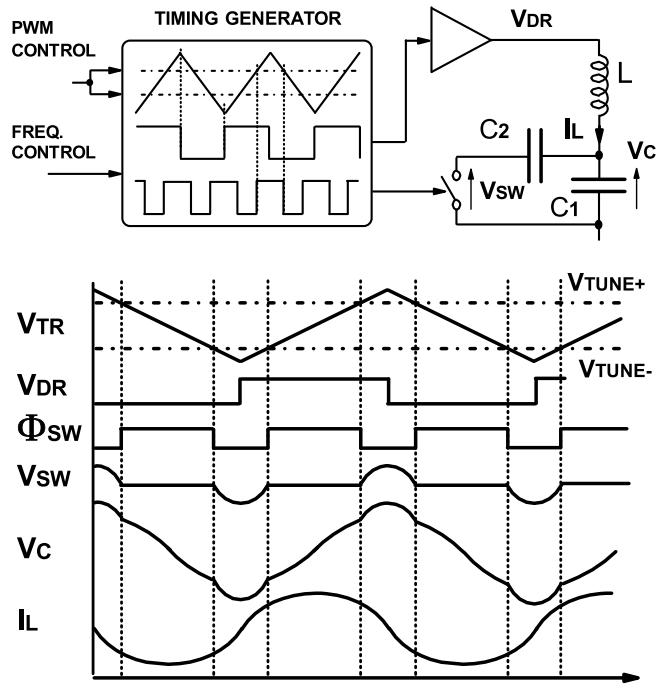

Fig. 3. Ideal timing generation for zero-voltage switched fractional capacitance tuning.

power, low-complexity system with no tuning capabilities and hence to use a fixed nominal antenna resonant frequency with a modest Q factor to give a satisfactory response despite the impacts of tolerances and environmental effects. The tuning resolution available for the transmit *LC* circuit must, therefore, be sufficiently precise to guarantee that the circuit may be tuned to within a defined bandwidth, for example, within the -3 dB points. As the Q factor is increased, the required tuning resolution is also increased.

Tuning the transmit antenna coil to resonance is simple in concept, but familiar small signal techniques using varactors are not realistic. With a high-Q factor, the tuning circuitry must remain functional with potentially large voltages (from a few V to kV) and currents (mA to many A) even with relatively modest excitation voltages. A conventional technique for inductive power systems is to use multiple external capacitors, typically with binary weighted values, selected by means of large solid-state switches [4], [7], or even electromechanical relays. The number of selectable capacitor elements needed depends on the Q factor, component tolerances, and the impact of environmental effects (which can include detuning due to ferromagnetic elements as well as the temperature). A typical system could require five or more selectable capacitors and associated HV switches (see Fig. 2), plus additional IC pins, adding significantly to system cost and volume.

An alternative tuning approach common at RF is to intermittently connect a capacitance to the *LC* circuit [8] with a defined switching duty cycle (as shown in Fig. 3), such that the time-averaged fractional capacitance creates a modified resonant frequency. A wide tuning range can be obtained in this way, determined by the ratio between the values of C_1 and C_2. When this technique is used at gigahertz frequencies, synchronism between the oscillation itself and the switching control signal is not realistic, and the switching rate is normally set significantly below the resonant frequency, with phase-noise shaping applied to the timing.

In addition to being able to tune such a large-signal *LC* circuit, there remains the problem of how to determine that the circuit has been adjusted to resonance. Conventionally, some circuitry is used to monitor either voltage or current, while the tuning system searches for a maximum response. Such arrangements typically require the system to go off-line while the tuning is set.

This paper is organized as follows. We first describe how the switched fractional capacitor tuning technique can be made to operate with zero-voltage switching with a negligible increase in losses compared with a conventionally tuned system. We then explain that by imposing these switching conditions, we can provide a direct means of sensing the resonant condition without the need for off-line adjustments and show how this can be used to provide simple closed-loop tuning control. We then identify some limitations of the ideal arrangement and describe an improved architecture to meet the practical constraints of a CMOS IC implementation. Circuits are presented that allow sensing of large voltages within the *LC* resonant circuit, and can compensate for delays in large-signal switching. Experimental results are shown in a demonstration design, comparing the static tuning performance with a weighted-capacitor tuning system of equivalent specification, as well as looking at the dynamic tuning response of the system to changes in operating frequency, exercising transient detuning behavior.

II. Zero-Voltage-Switched Fractional Capacitor Tuning

In order to minimize transient losses and harmonics, the capacitor switch should ideally be closed when the voltage across it is exactly zero. This minimizes the energy dissipated in the loss resistance of the switch upon closure and minimizes transients in the circuit. When the switch opens, the current into one capacitor is interrupted, but there remains a path

into the un-switched part of the available capacitance, and so the inductor current remains continuous at all times. With a commensurately low-resistance switch, a high-Q factor can be easily maintained, and there is a design freedom to ensure that resistive losses are less or no worse than in a system using near-static switches for the selection of fixed tuning capacitors. A further benefit is that the circulating current I_L (and hence the magnetic field) remains essentially sinusoidal despite the periodic modification in the resonant frequency, and thus, the radiated harmonic content is minimized.

While difficult at radio frequencies, the required synchronous switch timing becomes quite practical for most common inductive power systems, and similar approaches have been investigated [9] in order to improve active rectifier efficiencies in receiver functions. In order to achieve zero-voltage switching across the available tuning range, the capacitor switching action must be symmetrical with respect to either the zero crossing of the inductor current, or with respect to the peaks and troughs of the capacitor voltage waveform V_C (see Fig. 3) [10]. At resonance, the timings of both of these conditions are precisely known with respect to the excitation waveform, and so the ideal switch control signal may be derived directly from the drive source. In the case of a square excitation signal for a simple switching driver, the opening and closing instants (Φ_{SW}) will be equally disposed around the excitation transition edges (V_{DR}), as shown in Fig. 3. The LC circuit drive and capacitor switch control may be generated by a variety of means; Fig. 3 shows a simple analog implementation and associated waveforms that serves to illustrate the operation. In this example, the symmetrical capacitor switching is enforced by deriving both the drive V_{DR} and the switch control Φ_{SW} from a triangular waveform V_{TR} in a manner similar to a classical pulsewidth modulation scheme. The square drive polarity corresponds with the triangle ramp direction, while the capacitor switching is controlled by comparing the triangle wave with a dc tuning reference and its inverse (V_{TUNE+} and V_{TUNE-}). These values are spaced symmetrically around the mid-point of V_{TR} so that the positive and negative switching excursions of V_{SW} have equal duration, minimizing even-order harmonic content added to the oscillatory current. It is, thus, easily possible to adjust V_{TUNE+} and V_{TUNE-} so that the duty cycle of the fractional capacitor switching leads to an average resonant frequency matching that of the excitation, and a peak in the inductor current magnitude will be observed at the optimum tuning.

A. Resonance Detection for Self-Tuning

For most inductive power transfer systems, the effects of the installation environment and varying load conditions make some form of self-tuning in service essential, and hence, some method for detecting resonance is required. Two methods are commonly employed; the first is to seek a maximum in either the capacitor voltage or inductor current, possibly requiring a sense resistor, but this will degrade the Q factor. This approach is sensitive to changes in amplitude caused by loading the LC circuit with a receiver circuit, and hence, system operation must be periodically suspended to allow a sweep of the tuning settings to take place in order identify the maxima and then optimize the resonance condition.

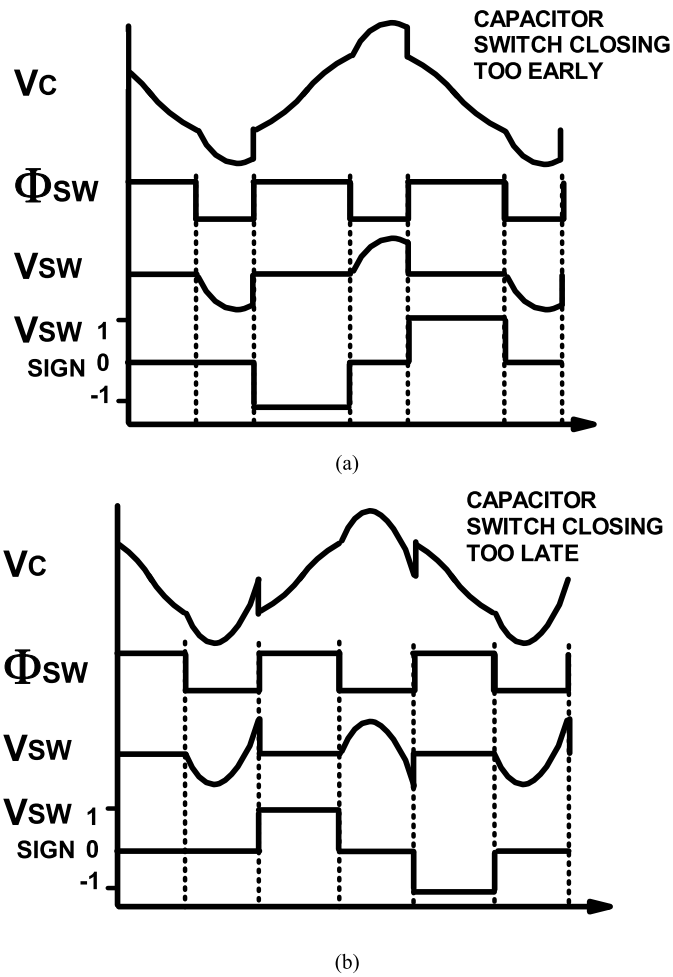

Fig. 4. Resonance error detection. (a) Switch closure instant occurring too early. (b) Switch closure instant occurring too late.

The second approach is to observe the phase of the oscillation in the LC circuit relative to the drive signal. At resonance, the current is in phase with the drive, while the capacitor voltage has a 90° lag. While this approach is less sensitive to amplitude variations, it requires that the phase can be accurately measured to ensure that tuning is accurate. Obtaining these signals is not without difficulty; the capacitor voltage may be very large compared with voltage limits for an IC implementation, while extracting the inductor current will require an undesirable shunt resistor.

These drawbacks may be circumvented by using signals available when zero-voltage switching is used with the fractional capacitor tuning arrangement. The resonant condition can be observed directly from the voltage excursions apparent across the capacitor switch.

For zero-voltage switching at resonance, it is required that the switch timing is symmetrical about the capacitor voltage maximum, and excursions should terminate at zero voltage, as shown in Fig. 3. Thus, a non-zero voltage across the switch just before closure indicates a tuning error, and furthermore, as shown in Fig. 4, the sign of this voltage indicates the

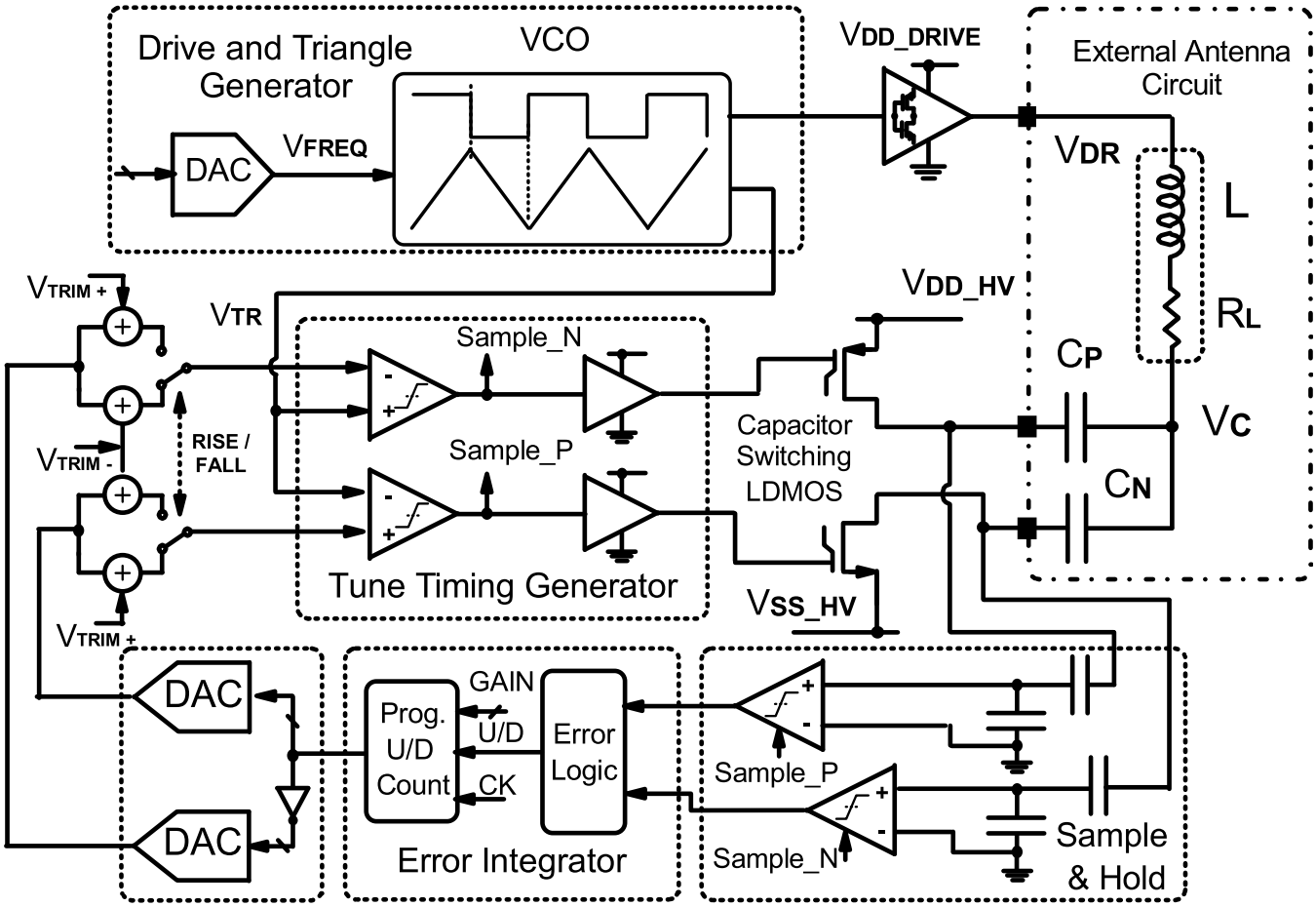

Fig. 5. Top-level system architecture for IC implementation.

direction of the error. This condition can be sampled each half cycle and integrated over time to provide a correction signal. Closing a simple feedback loop allows the setting of $V_{\mathrm{TUNE+}}$ and $V_{\mathrm{TUNE-}}$ such that the error will be minimized, so that the system will operate precisely at resonance and automatically adapt to changes caused by detuning effects [11].

The ability to monitor the resonant condition from the switch voltage excursions twice during each cycle allows continuous tracking and correction, eliminating any need for interrupting normal operation of the system. The zero-voltage switching method of tuning and resonance detection is also insensitive to variations in the amplitude of oscillation in the *LC* circuit, since only the sign of the voltage is needed to determine the resonant condition. This is particularly important at the lower end of the tuning range, as the switch voltage excursions may have low amplitude at this point.

III. Tuning System Architecture for IC Implementation

The basic fractional capacitance tuning architecture provides several challenges when considering a fully integrated solution, even if a "smart power" process is employed. The driver devices themselves are not generally a problem, as the voltages will be relatively low. However, the ideal tuning system [10] requires a bi-directional switch function that can provide not only an ON-resistance low enough to maintain the Q factor, but is also be able to sustain large positive and negative voltages. The large switch devices needed are also likely to incur significant delay with respect to the ideal timing controls. Furthermore, sensing the voltage across the switch and sampling the sign at a defined instant require fast, high-gain circuits able to withstand large voltages.

The process available was a 1.8–50 V CMOS/Laterally Diffused MOSFET technology, allowing the integration of the excitation and drivers, timing circuits, as well as the fractional capacitor switches. For die area and cost reasons, the nominal maximum inductor current was set to 100-mA rms allowing for a moderate power transfer level. The design was optimized for operation in the 125-kHz region commonly used by contactless security and wireless charging systems, with a maximum operating frequency up to 2.6 MHz. Although clearly desirable to cover some of the higher frequency bands, the additional design work required in the technology used was deemed beyond the time and budget available for the project.

The overall architecture of the integrated system is shown in Fig. 5.

A. Capacitor Switching in IC Implementations

The ideal HV low-resistance transmission gate required in the basic tuning concept [11] is clearly impractical in a readily

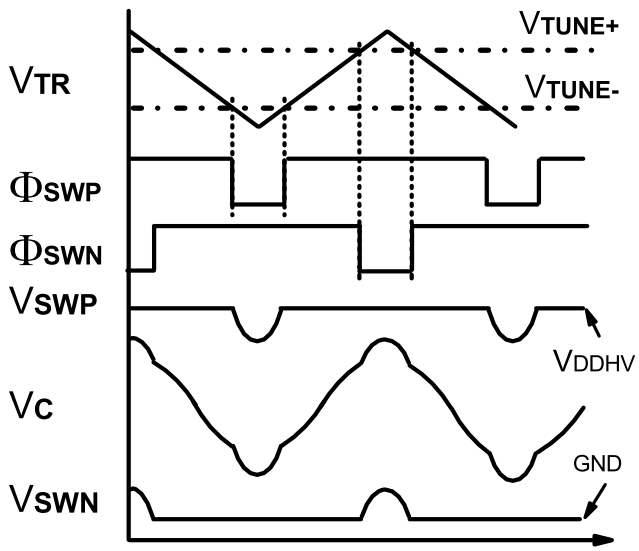

Fig. 6. *LC* circuit waveforms with unipolar switches.

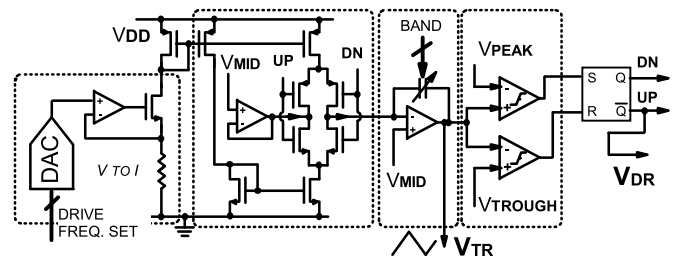

Fig. 7. Up/down current integrator oscillator for triangle generation.

available smart power process, and it is therefore necessary to restructure the switching architecture. The single switched fractional capacitor can be split into two equal capacitors, each with its own independent switch, and each switch constrained to operate only on alternate half-cycles of the capacitor voltage. By opening each switch only during alternate half-cycles, we can limit the open-circuit voltage excursions to only one direction. Hence, an HV N-LDMOS switch can be used for the positive V_{SW} excursions, with its source node connected to a separate ground supply V_{SS_HV}, so that at resonance, when the N-LDMOS turns off, the drain voltage is always positive. Similarly, an HV P-LDMOS switch with its source connected to a separate HV supply V_{DD_HV} can be used for the negative V_{SW} excursions. The value of V_{DD_HV} effectively determines the maximum peak value of V_{SW} at which the drain diffusions will experience forward bias into the local bulk.

When not precisely at resonance, reverse voltages can appear across the LDMOS switches, leading to conduction in the protection diodes. However, this is not, in practice, very significant, since the self-tuning system only requires polarity information, and the forward voltage of the diodes still provides sufficient input to the control loop to ensure that the system can return to resonance.

The dimensions of the LDMOS switches are chosen to ensure that the resistive losses seen are sufficiently low compared with those in the inductor that the desired Q factor can be achieved. For moderate antenna currents, this can be realized with fully integrated LDMOS devices, but for larger currents, it is likely that external discrete HV switches will be more practical.

Note that two switch control signals are now required as per Fig. 6, but the functionality is essentially the same as the ideal concept [11]. Furthermore, since only one unipolar switch is open at any given time, there will always be a path for the inductor current to remain continuous without the need for a third un-switched capacitor. Using two equal capacitors C_P and C_N in this way places a limit on the minimum to maximum capacitance ratio of ideally 1:2, with a corresponding adaptive tuning range ω_{max}:ω_{min} of approximately 1.4:1. This is, however, a sufficient range for most practical tuning requirements in a given application.

Ideally, capacitors C_P and C_N should be identical, but, in practice, manufacturing tolerances must be accounted for. To ensure zero-voltage switching on both positive and negative excursions, an ideal system could use two separate tuning control loops to provide precise timing for each switch. However, for realistic tolerances, this is unlikely to be needed. Experimental measurements at 110 kHz with Q of 30 using the single averaged feedback loop showed a drop in the amplitude of the peak voltage V_{SW} of less than 1 dB with respect to ideal conditions, even with a capacitor mismatch of 20%.

B. Timing Generation

The target operating range of the demonstration IC is 75 kHz–2.6 MHz, covering common RFID, security, and wireless charging systems. This frequency range is divided into eight bands, with sufficient overlap between bands to ensure that the tuning system can cover practical tuning requirements continuously without the need to switch bands (as the latter would lead to the system stopping momentarily). In order to achieve a sufficiently high tuning resolution, timing generation is implemented in analog circuitry, since a fully digital approach would require operation beyond the capabilities of the CMOS/LDMOS process used. The V_{DR}, Φ_{SWP}, and Φ_{SWN} tuning signals are derived from an analog triangle wave V_{TR}, which is generated by a conventional current integrator oscillator, incorporating a digital frequency control input. The integration current is set using a thermometer digital-analogue converter (DAC) driving a V-to-I function, providing the fine frequency control. Coarse frequency band control is achieved by the digital selection of the integration capacitors (see Fig. 7).

The peaks and troughs of the integrator output V_{TR} are detected with continuous-time comparators; an reset-set (RS) latch then sets the ramp direction. This latch also produces the excitation signal V_{DR} for a simple class D driver, so that the *LC* circuit may be driven directly from the IC. A separate variable supply V_{DD_DRIVE}, allows the excitation level to be adjusted for different antenna circuit Q factors. The driver itself was not a key focus of this paper and was deliberately made quite simple, although the high-Q of the antenna coil circuit means that asymmetry and even-order harmonics are heavily suppressed in the current waveform.

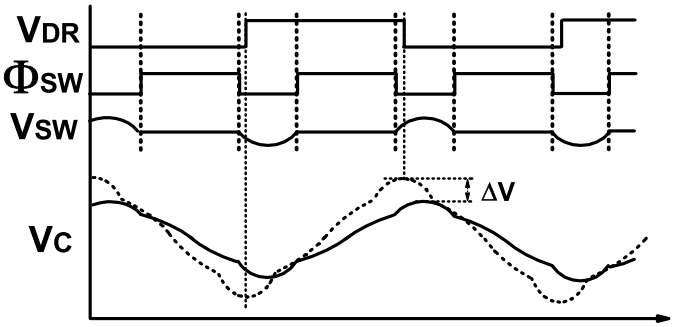

Fig. 8. *LC* circuit voltage amplitude reduction caused by capacitor switching phase offset.

V_{TR} is also used to generate the capacitor switch timing signals Φ_{SWP} and Φ_{SWN}. The analog tuning control signal and its inverse V_{TUNE+} and V_{TUNE-} are generated from a pair of 8-bit thermometer DACs, connected in series and referred to the same reference values as the triangle peak and trough levels. This allows the symmetry of the capacitor switch signals to be easily maintained. The design linearity and the guaranteed monotonicity of the architecture help to ensure that the closed tuning control loop is not unstable at any point in the tuning range. The magnitude of the triangle signal V_{TR} is set to have relatively large-signal swing at 1–4 V, thus relaxing the offset error requirements of the continuous-time comparators (predicted 1-σ offset of less than 3 mV) and the resolution of the controlling thermometer DACs.

C. Effect of Timing Offset and Phase Trimming

Under ideal conditions, it is assumed that the opening and closing of the capacitor switches using Φ_{SW} is symmetrically spaced in time around the rising and falling edges of V_{DR}. In practice, the control circuitry for the driver and capacitor switch FETs will incur a finite propagation delay due to each stage of the associated buffers and to the significant capacitances at the gates of the large HV FETs.

Any systematic offsets in the continuous-time comparators used to operate the capacitor switches will be manifest as additional timing errors. If the combined effects of these delays are not properly accounted for, the symmetrical switching criteria will not be met and ideal resonance will not be achieved, even though zero-voltage switching may be possible. Fig. 8 shows the effect of non-symmetrical switching in an ideal fractional capacitance tuning system (as shown in Fig. 3). V_C aligns with the V_{SW} excursions, creating a non-ideal quadrature phase. The ideally tuned V_C waveform is shown in dotted form for comparison. There is a reduction ΔV in the amplitude of V_C caused by the timing offset, and hence, the magnitude of the inductor current I_L will also be reduced.

In order to compensate for phase delay in the drivers of the *LC* circuit and capacitor switches, the opening and closing instants must have some small degree of independent trimming relative to the excitation phase. This is achieved in the IC architecture by modifying replicated versions of V_{TUNE+} and V_{TUNE-} so that separate comparisons may be made against V_{TR} on the rising and falling edges, thus adjusting the phase position of Φ_{SWP} and Φ_{SWN} relative to V_{DR}. Fig. 9 (left) shows an example of phase lead: the opening of the switches is brought forward by moving V_{TUNE} closer to the mid-point of V_{TR}, while the closure is delayed by moving V_{TUNE} further to the peaks and troughs. Fig. 9 (right) shows the opposite case where a phase lag is added for a scenario where an external driver is used, hence requiring that the switching of C_N and C_P is delayed to maintain accurate tuning.

This approach to phase trimming is easily implemented by adding an offset value to the digital tuning setting (see Fig. 10). A second pair of output taps is added to the thermometer DAC strings to create the additional trimmed V_{TUNE} voltages. The voltage comparison result selected is determined from whether V_{TR} is on a rising or falling slope. Note that the phase trim value applied with this method is quite deterministic, since it is derived directly from the operating frequency (i.e., a fixed proportion of the period of the triangle signal V_{TR}), and not from an independent analog time delay function (with associated process, voltage and temperature (PVT) variations). This method of phase trim does, however, incur a small reduction in the available tuning range, since the imposed offsets in the V_{TUNE} levels reduce the available range of the comparison against the triangle reference V_{TR}.

D. Switch Voltage Excursion Sign Sampling

A sense-sample function is integrated into the system in order to allow the observation of the sign of the capacitor switch voltages V_{SWP} and V_{SWN} immediately before closure. Since these switch voltage excursions can easily exceed the safe limits for the internal circuitry, a thick-oxide capacitive divider is used to attenuate V_{SW} down to V_{SWA} (see Fig. 11). Each switch has a corresponding capacitive divider to allow the switch excursions to be sampled independently. In this design, the maximum switch voltage at the high frequency end of the tuning range was expected to be of the order of 20 V. Since only the signs of these inputs are required, the precise attenuation factor is not critical and has two ranges affected by the selection of an additional component of $C_{SB_N/P}$. The attenuated signal used for tuning sign detection is still relatively large (up to ~3 V) and so comparator offsets are not a major issue.

While each of the capacitor switches is in its closed state, its corresponding capacitive divider is reset to the reference potential $V_{DD}/2$, provided by a simple buffered potential divider. This prevents a gradual drift in the dc pedestal at the comparator input by ensuring that the comparator input is referred to the switch-closed condition at the start of each excursion (see Fig. 12).

The sampling signals $\Phi_{SMP/N}$ are derived from the capacitor switching signal outputs from the timing generation circuits $\Phi_{SWP/N}$. The level shifts and the LDMOS gate drive circuits add a significant but relatively stable delay, which means that in order for the sampling to occur just before the switch will close, a small additional delay is needed in the sampling signals. This is implemented with a simple delay line, sized accounting for the effects of PVT variations. Once the sampling signals (Φ_{SMP} and Φ_{SMN}) have risen and the error data

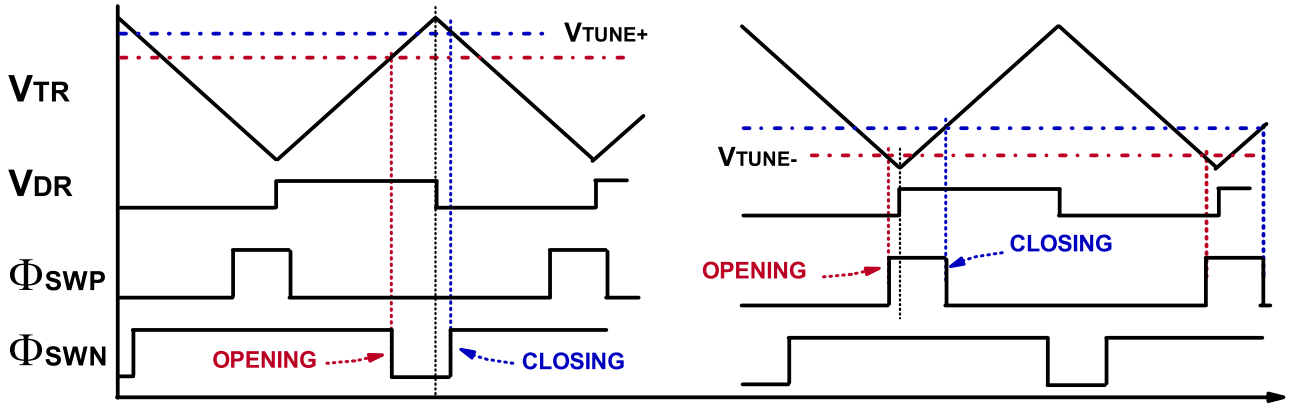

Fig. 9. Phase trim system operation. Left: lead added to switch control signals (only positive sense references shown) compensating for capacitor switch delay. Right: lag added to switch control signals (only negative sense references shown) to compensate for drive delay.

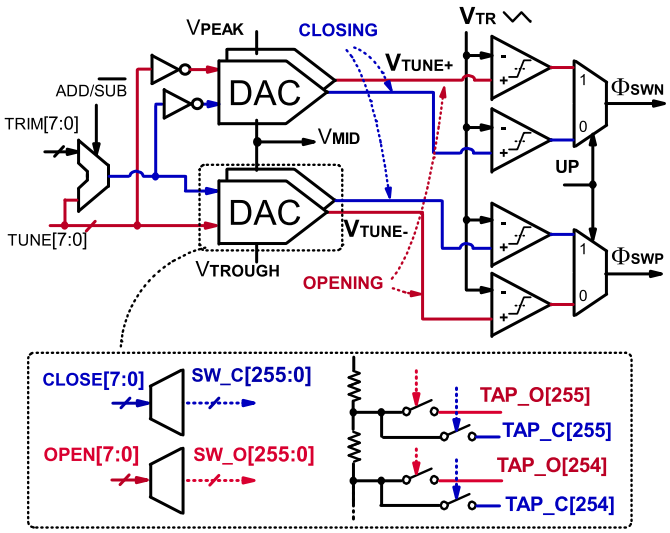

Fig. 10. Dual-tap thermometer DAC and switch control comparator architecture (with phase trim functionality).

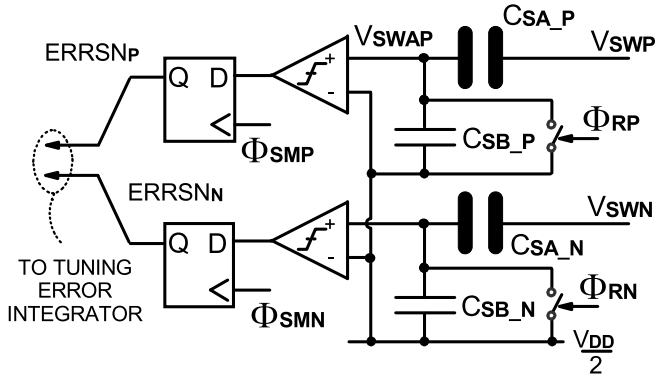

Fig. 11. Switch voltage excursion sampling circuit.

are sampled ($ERRSN_P$ and $ERRSN_N$), the capacitive dividers can be reset (Φ_{RP} and Φ_{RN}), and the HV switch can be closed. The length of the relative delay is negligible at the frequencies of operation and hence does not noticeably degrade the tuning accuracy.

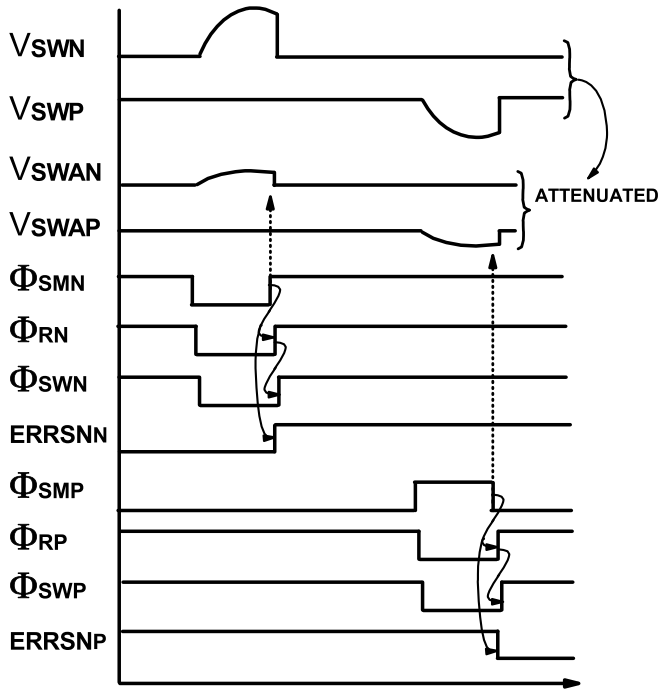

Fig. 12. Switch voltage excursion sampling timing example.

E. Self-Tuning Error Integrator

The sampled error data are then integrated to generate the feedback tuning control setting (see Fig. 13). A digital up/down counter is used for this function, since the error data are already in digital format. Furthermore, the integration time constant required for the self-tuning is quite large compared with the operating frequency, and hence, an analog integrator would consume significant area due to the large on-chip capacitors required. The error signals from the positive and negative excursions $ERRSN_P$ and $ERRSN_N$ are combined to give an *enable* and *up/ndown* instruction for a 10-bit counter. If the detected sign data for the opposite excursions are in conflict, then the digital integrator is not updated, i.e., *enable* $= 0$. Otherwise, the counter is incremented or decremented according to *up/ndown*. The counter is clocked synchronously from the

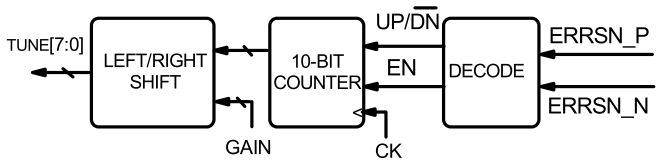

Fig. 13. Digital integrator architecture.

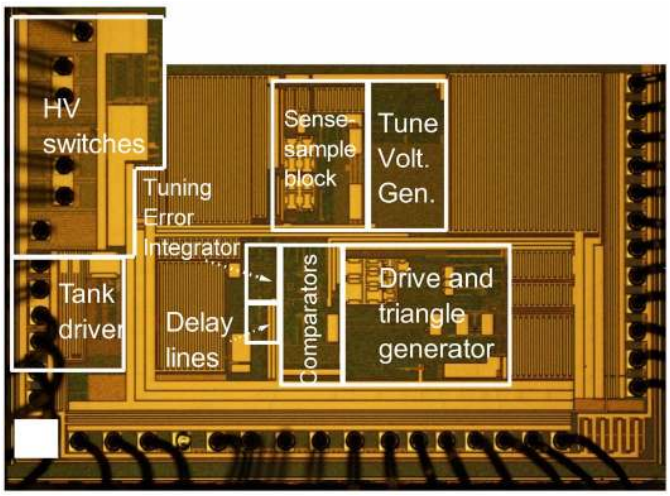

Fig. 14. System die micrograph, showing primary blocks.

peaks and troughs of V_{TR} so that the tuning feedback loop is updated synchronously twice per cycle.

To provide a variable integrator gain, the output of the counter is windowed with a left/right shifter to adjust the effective gain of the integrator block, permitting the settling time to be traded against steady-state ripple in the tuning control. This approach allows for a large gain range to be obtained. Given that the integrator is a counter always clocked at twice the drive frequency, the integration gain is most logically expressed in terms of the increment/decrement in tune setting per clock cycle. The designed gain range in this system is from x0.25 (i.e., able to sweep the entire tuning range in 512 cycles of V_{TR}) to x32 (i.e., sweeping the tuning range in four cycles).

The integrator output bus *tune[7:0]* is connected to the tuning voltage DACs, closing the self-tuning control loop. Note that there will always be some residual ripples in the tuning over time due to the quantizing of the feedback. In this design, the DACs used are only 8 bits, leading to quite easily visible tuning ripple.

IV. Experimental Results

The IC was fabricated in a 0.18-μm 1.8–50 V CMOS–LDMOS process. The die area was 3.17 mm^2 and was mounted for testing in a plastic quad flat package (QFP). Dual bonds were used for the driver and capacitor switch connections, as well as the associated HV supplies. Power for this demonstrator was provided from external regulated supplies at 1.8, 5, and 20 V; internal digital parameters were set by means of external control. Fig. 14 shows a micrograph of the die, with the primary blocks highlighted and metal fill capacitors located in between. The dc power consumption of the excitation, timing, and tuning system is 79 mW, but excluding the antenna coil driver supply. The main antenna circuit power will normally dominate the total consumption and is heavily dependent on the application and the antenna circuit's passive components, and thus should be considered separately. Table I shows a comparison of power overhead of the implemented tuning system, compared with that of recent commercial inductive link transmitters operating at similar frequencies (also excluding the antenna drive). A direct comparison is difficult, as the commercial parts contain modulation/demodulation and housekeeping functions, but do not include a self-tuning system. However, it can be seen that the power overhead of the latter is generally comparable.

TABLE I
Comparison of This System and Commercially Available Inductive Link Transmitter Systems

	This work	Melexis MLX90109 [12]	M. Dudde BG744CI [13]	EM. Micro EM4095 [14]
Power Overhead (mW)	79	9	67.5	25
Self-tune functionality	Yes	No		
Data modulation	No	Yes		

A. Steady-State Tuning Behavior

Fig. 15 shows measured steady-state tuning conditions with the IC operating in the 110-kHz region while driving an air-cored loop antenna with an inductance of 1.3 mH and an in-circuit Q of approximately 30. The lower end of the tuning range is shown in Fig. 15(a), where the capacitor switch open-state excursions V_{SWP} and V_{SWN} are small (i.e., less than 2-V peak). By contrast, the upper end of the tuning range is shown in Fig. 15(b), where the V_{SWP} and V_{SWN} excursions track the shape of the corresponding V_C excursion for the majority of each cycle, reaching nearly 20-V peak.

In both examples, resonance has clearly been achieved, as V_{SWN} and V_{SWP} can both be seen to terminate at the corresponding supply potentials. The peaks and troughs of V_C are also aligned closely with the edges of the excitation drive signal V_{DR}. The relationship between the effective resonant frequency ω_{Res} and the OFF-time phase angle θ_{off} for each switch is easily analyzed; re-casting (4) from [11] in terms of the P and N switching configuration gives

$$\omega_{Res} \approx \frac{\pi\,\omega_{Min}}{(\pi - \theta_{OFF}) + \sqrt{2}\tan^{-1}[\sqrt{2}\cot((\pi - \theta_{OFF})/2)]}. \quad (1)$$

Fig. 16 shows the self-tuning system operating at 2.6 MHz. While still maintaining reasonable tuning accuracy at this frequency, the limitations due to the available technology and the optimization for 125-kHz operation become more apparent. The drain–source capacitances of the LDMOS tuning switches and other parasitics start to become comparable with the values of $C_{P/N}$ (33 pF in this experiment), leading to some capacitive

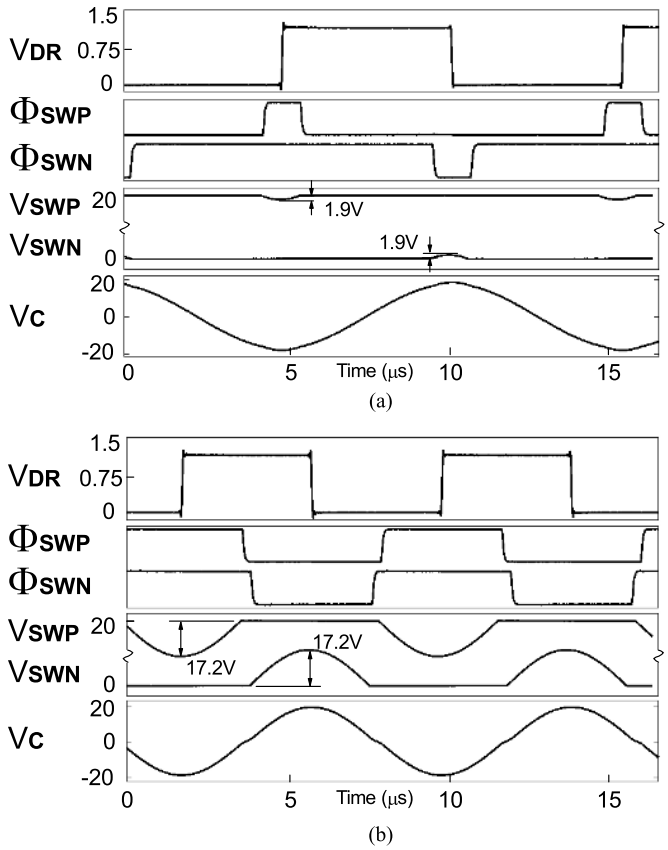

Fig. 15. Measured in-tune operation at (a) 99.36 kHz, $Q = 30$, and $L = 1.3$ mH and (b) 125.9 kHz, $Q = 30$, $L = 1.3$ mH.

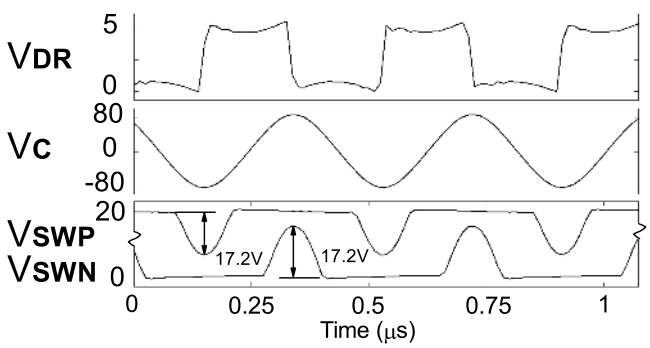

Fig. 16. Measured in-tune operation at 2.61 MHz, $Q = 30$, and $L = 31.5\ \mu$H.

voltage division at the switching pins of the IC. There is some benefit in this insofar, as it allows a larger drive voltage to be used with correspondingly higher antenna current. The effect of this larger current on the output resistance of the simple antenna drivers can be seen with some distortion of the ideally square drive voltage, while the voltage at the inductor/capacitor node is now seen to be much larger. This voltage division also has some impact on the system's tuning range [11].

There is also some visible impact on the propagation delays in the tuning switches, making apparent the limitations of the process technology and emphasizing the need for a phase-trimming capability. Post-fabrication simulations indicate that a combination of internal delays, and incomplete settling of the sign-detection comparator references after some kickback, leads to non-optimal switch timing such that the $V_{\mathrm{SWP/N}}$ excursions do not terminate precisely at the respective supply potentials.

B. Tuning Accuracy Comparison

In order to fairly assess the benefits of the fractional capacitance tuning system, we can compare the static tuning accuracy of the fabricated IC with a conventional implementation having equivalent current, Q factor, and tuning specifications, by considering the phase difference between V_{DR}–V_C compared with the ideal 90° condition. A comparison between physical implementations is not, in reality, very informative, due to differences in system applications (different operating frequencies, power levels, IC processes, and so on). In a conventional quasi-static discrete weighted-capacitor tuning system, the number of selectable capacitors required can be calculated from the specifications for the required tuning accuracy.

The smallest unit capacitance relative to the fixed capacitance must first be calculated. If the nominal resonant frequency is given as $\omega = 1/\sqrt{LC}$ and the maximum offset frequency within the tuning resolution is given by $\omega + \Delta\omega = 1/(L(C + \Delta C))^{1/2}$, then (2) gives the ratio between the smallest selectable capacitor and the fixed capacitor

$$\frac{\Delta C}{C} = \left(\frac{\omega + \Delta\omega}{\omega}\right)^2 - 1. \tag{2}$$

The number of capacitors required to achieve the tuning resolution required is, therefore, given as follows:

$$N_{\mathrm{cap}} = \log_2\left[\frac{1}{\left(\frac{\omega+\Delta\omega}{\omega}\right)^2 - 1}\right]. \tag{3}$$

Note that with a linear capacitor selection range, the tuning frequency spacing will be non-linear due to the inverse relationship between ω and C. Where an absolute minimum frequency offset is specified, the resonant frequency for calculation must be set to the highest resonant frequency to ensure that a sufficiently high resolution is available across the entire tuning range. Alternatively, given the definition of $Q = \omega/\Delta\omega$, (3) may be expressed as per (4) where tuning to within the -3 dB points is sufficient

$$N_{\mathrm{cap}} = \log_2\left[\frac{1}{\left(\frac{Q+1}{Q}\right)^2 - 1}\right]. \tag{4}$$

Table II shows a comparison of results from a batch of 10 samples, in the 110-kHz, 1.3-MHz, and 2.6-MHz operating regions, all with operating Q factors of approximately 30 without additional phase trimming applied. To achieve the same tuning accuracy, an equivalent weighted-capacitor tuning system in the same technology and the same operating Q would require significantly more capacitors and switches (11 transmission gates for 110-kHz operation, 10 for 1.3-MHz operation, and 7 for 2.6-MHz operation). The required IC

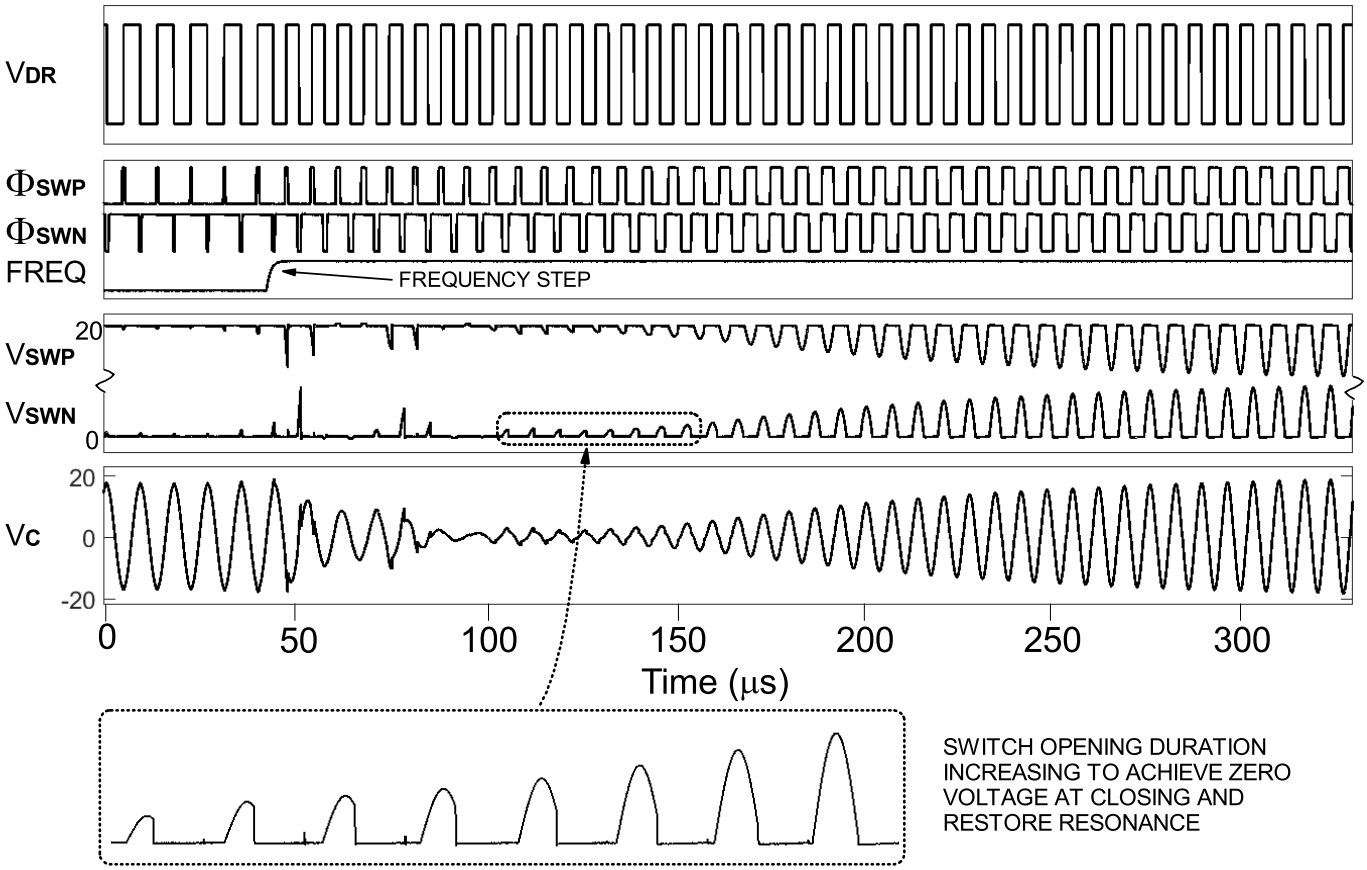

Fig. 17. Measured self-tuning response to a 100–130 kHz frequency step (X8 integrator gain).

TABLE II
COMPARISON OF TUNING ACCURACY AND HV AREA REQUIREMENTS

	This work			Binary-weighted tuning			
	Average 10 samples			Equivalent results			3dB bandwidth
Frequency	110kHz	1.3MHz	2.6MHz	110kHz	1.3MHz	2.6MHz	Any
Tuned phase error (trimming disabled)	0.97°	2.26°	11.3°	> 1°	> 2.5°	> 11°	> 45°
Switches / Package Pins	2	2	2	11	10	7	5
R (PMOS) Ω	4.89			10.6			
R (NMOS) Ω	5.80			10.6			
HV switch area (μm^2)	1360			3740	3400	2380	1700
Other area (mm^2)	0.246			1.35	1.10	0.859	0.615
Typical Transient Settling*	Approximately 125 cycles			N/A			
Power Consumption (mW)	79			Negligible, but no continuous tuning capability			

* With x1 integrator gain, defined by time for tuning to reach steady-state value at Q = 30

die area can be compared fairly by allowing for the same HV switch resistance as measured on the fabricated system. Comparing with a more realistic implementation using five weighted tuning capacitors (i.e., tuning to within the 3-dB bandwidth when $Q = 30$), the zero-voltage switched fractional capacitor method of tuning requires less IC die area and fewer package pins in all cases, significantly reducing the cost of tuning the *LC* circuit. "Other area" listed in Table II includes bond-pad area for the required number of switches and package pins.

In terms of comparative power consumption, the capacitor selection technique has an apparent advantage insofar, as the consumption in each static tuned state is negligible. However, this benefit could only be achieved in a completely static environment, as there is no capability for continuous sensing of disturbances in the resonance condition.

The resistive loss in the HV tuning switches at the maximum rated drive current is approximately 530 mW. This maximum occurs at the upper end of the available tuning range, i.e., when only one switch is closed for the majority of the cycle. This loss can be reduced by increasing the width/length ratio of the FETs, at the expense of larger die area and increased power in the associated gate drive circuits. Note that comparable resistive losses would be incurred by alternative discrete-step tuning configurations. The cyclical switching gate drive power component is clearly frequency-dependent, with simulations indicating that the present design consumes 31 mW at 2.6 MHz.

C. Transient Tuning Behavior

Unlike the conventional tuning systems, the fractional capacitance tuning system can maintain accurate tuning to resonance continuously, while the host system is operating normally. The response to abrupt changes in operating conditions is also rapid and well behaved. This is demonstrated in Fig. 17, which shows the system response to a step change in operating frequency from 100 to 130 kHz, using a moderate integrator gain of x8.

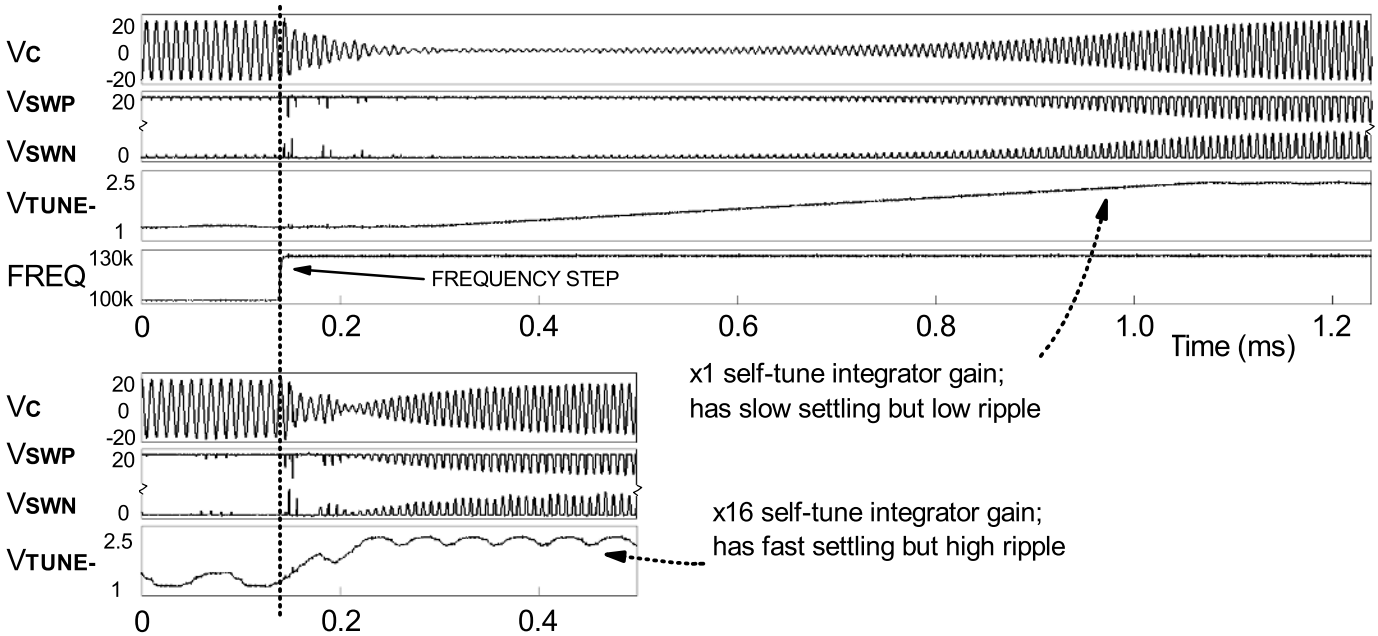

Fig. 18. Measured self-tuning response to a 100–130 kHz frequency step (X1 and X16 integrator gain).

The system is initially stable and resonant at 100 kHz; after the frequency is abruptly increased, there is an immediate, significant drop in the amplitude of the capacitor voltage V_C. Within about 100 μs, the self-tuning loop correctly identifies that the system is no longer resonating and widens the opening durations of Φ_{SWP} and Φ_{SWN} until resonance is restored.

Fig. 18 shows two more extreme cases of integrator gain: x1 (top) and x16 (bottom). As the self-tuning integrator gain is increased, there are more ripples in the tuning setting at steady state, which leads to some uncertainty in the tuning of the *LC* circuit and lowers the average amplitude of oscillation. Some ripples in the tuning are visible regardless of the gain setting, due to the 8-bit quantized tuning range. The response time with an x1 self-tuning gain is given in Table II, taking approximately 125 cycles of oscillation to sweep the tuning range and converge on the optimal tuning setting. With an x32 gain, the settling time reduces to approximately 17 cycles to converge on the optimal tuning; however, the larger gain causes a more significant ripple in the tuning setting and consequently a larger tuning error. This can be seen in Fig. 18, where the average amplitude of V_C is lower due to the large variation of the V_{TUNE} voltages. Experimental results using x32 gain indicate that the average amplitude of V_C is reduced by approximately 4.4 dB compared with the case using x1 gain. A more advanced control loop using a variable integrator time constant could obviously be employed, such that a fast settling time is achieved while maintaining low ripple during the steady state.

Fig. 19 shows a slower frequency sweep from 130–100 kHz in 1.4 ms, with self-tuning disabled (top) and enabled (bottom). Where tuning is disabled, the V_{TUNE} voltages are set such that resonance is approximately mid-way in the sweep. When the system is driven non-resonantly, the amplitude of V_C is reduced. When self-tuning is enabled, the error-detection system adjusts V_{TUNE} so that the resonant frequency is tracked by the tuning loop in real time as it changes. The amplitude of V_C, and therefore I_L, is maintained roughly constant over the entire frequency range.

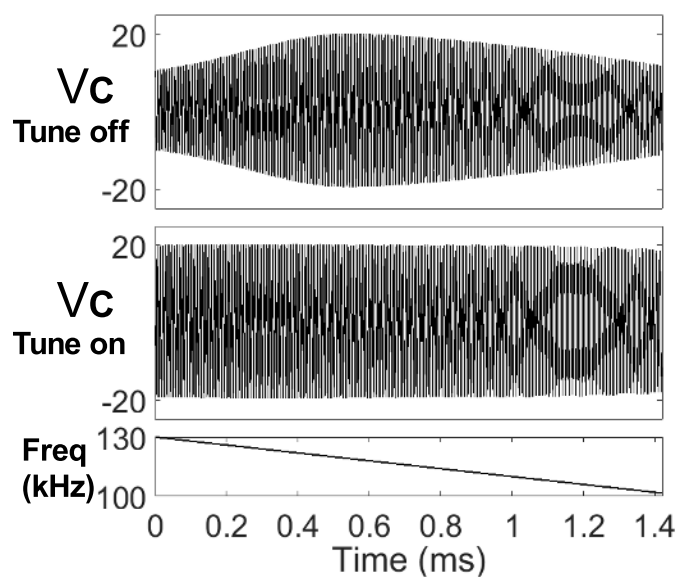

Fig. 19. Measured *LC* circuit internal voltage with excitation swept 130–100 kHz with self-tuning disabled (top) and enabled (bottom).

D. Switch and Driver Delay Compensation With Phase Trimming Circuitry

As shown in Table II, the system's tuning phase error is less than 1° in the 110-kHz region without any phase trimming, which is quite adequate for most practical applications. However, at higher operating frequencies or where larger (possibly external) devices are used, some delay adjustments may be necessary. In order to show the effect of the phase trimming circuitry, the demonstration system was run in its

TABLE III

TUNING ACCURACY WITHOUT PHASE TRIM APPLIED (LEFT) AND WITH PHASE TRIM APPLIED (RIGHT) FOR OPERATION IN THE 2.6-MHz REGION

Condition	Untrimmed	Trimmed
Phase error	11.3°	0.4°
Resonant freq. error (kHz)	8	0.3
V_C loss (dB)	0.6	-

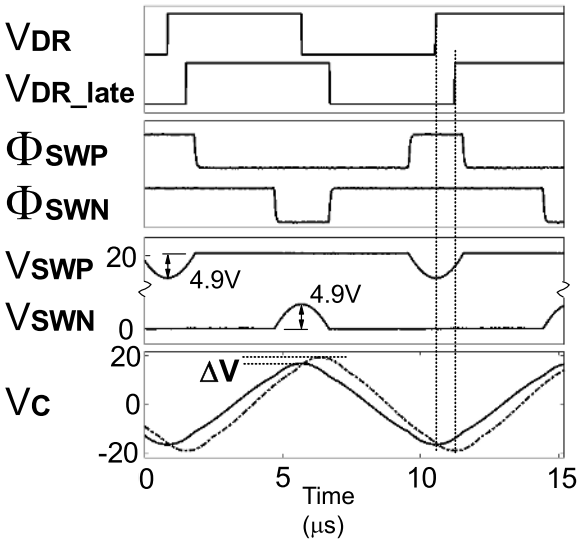

Fig. 20. Measured *LC* circuit voltages at 102.9-kHz operating frequency with a delay of 700 ns added to driver excitation. Phase-trimmed V_C shown in dotted line.

maximum frequency band (2.6-MHz region). Note that the driver is implemented using 5-V transistors, while the capacitor switches are much larger LDMOS devices, and therefore, the latter contributes significantly more delay due to the greater capacitances in their driver chains (the effect of the incomplete comparator reference settling, discussed in Section IV-A, can be treated as a contribution to this delay). Table III shows the results from operation with and without phase trimming applied. Note that the V_C loss is normalized with respect to the phase-trimmed amplitudes.

In this system, the V_{DR}–V_C phase error in this band was measured to be 11.3°. A phase lead was therefore added to the switch control signal ΔSWP to trim the V_{DR}–V_C phase error as closely as possible to zero, both reducing the equivalent frequency offset from approximately 8 kHz–330 Hz and increasing the amplitude of V_C by ensuring that the *LC* circuit was closer to the resonant condition. It is clear that phase trimming becomes essential to maintaining resonance as the operating frequency is increased, or where larger (and thus slower) switching devices are to be used for higher power applications. In such applications, a fully adaptive phase trimming system, possibly using replica delay lines, would be clearly desirable for a commercial implementation.

A second experiment into the effects of phase trimming was used to investigate the opposite scenario, where the drive lags behind the capacitor switching action. The operating frequency was reduced to the 110-kHz region, and a large delay of approximately 700 ns was added to the driver, such that it now dominated over the delay of the capacitor switches.

TABLE IV

MEASURED TUNING ACCURACY WITHOUT PHASE TRIM APPLIED (LEFT) AND WITH PHASE TRIM APPLIED (RIGHT) FOR OPERATION AT 102.9 kHz

Condition	Untrimmed	Trimmed
Phase error	25.1°	0.2°
Resonant freq. error (Hz)	800	7
V_C loss (dB)	1.2	-

Fig. 20 shows mid-band oscillations with both the original and delayed driver waveforms at 102.9 kHz. It can be seen that the oscillation of V_C is aligned closely with the excursions of V_{SWP} and V_{SWN} and hence with the original driver signal when no phase trimming is applied. The V_C traces show the cases both with phase trimming enabled and with no phase trimming, where the correct value of phase trimming aligns V_C with the rising and falling edges of V_{DR}_late. A maximum amplitude drop of ΔV is indicated. Table IV shows the improvement provided by phase trimming in this example.

V. CONCLUSION

A self-tuning transmit driver for *LC* circuits in wireless power transfer applications has been presented. The implementation is fabricated in a standard 0.18-μm CMOS/LDMOS process, with timing generation and high-voltage switches integrated into the same die. The system uses zero-voltage switched fractional capacitors in order to reduce the number of bond pads and package pins required compared with the conventional tuning methods using quasi-static switched arrays of weighted capacitors. The proposed tuning method also permits the continuous tracking of the resonance condition by observing the sign of voltage excursions just before the closing of the switches and is insensitive to the amplitudes in the resonant circuit. The fabricated system exhibits a tuning accuracy, which is significantly better than a practical conventional tuning system, simultaneously requiring fewer capacitors and allowing for high-resolution tuning at high-Q. The measured tuning error from a batch of 10 samples is less than 1° in the 110-kHz region without requiring additional phase trimming. A similar accuracy can be obtained in the maximum chip frequency range of 2.6 MHz using the presented phase trimming architecture to compensate the propagation delay of the capacitor switch drivers. Future improvements to the system architecture are possible to minimize the effect of propagation delays to allow for operation in higher frequency bands for RFID, such as 6.78 MHz.

In applications where rapidly changing detuning effects are present, a more sophisticated control loop for automatic tuning

setting adjustment could be implemented to allow for a faster response time with less steady-state tuning ripple.

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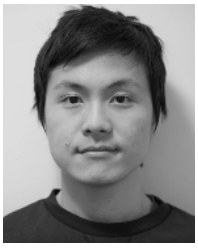

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William Redman-White (M'83–SM'08–F'14) was with NXP Semiconductors (and its predecessor, Philips Semiconductors) as an Engineering Fellow from 1990 to 2011, where he was involved in analog and RF design. Based mainly in Southampton, U.K., he was also with Philips, San Jose, CA, USA, from 2001 to 2003 and in Caen, France, in 1999. Within NXP/Philips Semiconductors, U.K., he was involved in a wide range of projects and products, covering optical storage, cellular and WLAN radio, analog and digital TV, and automotive applications. He was previously with Motorola, Switzerland, GEC-Marconi Research London, and Post Office Telecommunications, U.K. Concurrent with his industrial activities, he has also held a part-time academic position at the University of Southampton, Southampton, where he became a Full Professor in 1998. Previous programs included significant work on design in SOI CMOS. His research and teaching interests include analog and RF IC design, primarily in CMOS technology.

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