A Sensitive Method to Measure the Integral Non-Linearity of a Digital-to-Time Converter based on Phase Modulation

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***Abstract*—A Digital-to-Time Converter (DTC) produces a time delay based on a digital code. Like for data converters, linearity is a key metric for a DTC and it can be characterized by its Integral Non-Linearity (INL). However, measuring the INL of a sub-ps resolution DTC is problematic even when using the best available high-speed oscilloscopes.**

In this paper, we propose a new method to measure the INL of a DTC, by applying digital phase modulation and measuring the output spectrum with a spectrum analyzer. The frequency selectivity of this method allows for improved measurement resolution down to a few fs and allows to measure a INL below 100 fs. The proposed method is verified by behavioral simulations and employed to measure the INL of a high-resolution DTC realized in 65 nm CMOS, with time-resolution of 25 fs and standard deviation of 27 fs.

I. Introduction

Time or clock generation with high fidelity is at the heart of numerous electronic systems. The rapid development in Time-to-Digital Converters (TDCs) and Digital-to-Time Converters (DTCs) [1], that are increasingly used in Phase-Locked Loops (PLLs) [2]–[4], pushes the required time resolution to well below 1 ps. This paper targets the measurement of such small timing steps. The principal instruments traditionally employed for such measurements are the network analyzer or the oscilloscope.

Network-analyzer-based measurement methods quantify the phase difference between two sinusoidal signals, generated by the same source and passing through two different paths [5]. This phase difference is translated into a time difference, assuming accurate knowledge of the carrier frequency. Processing algorithms applied to the detected phase difference allow to achieve more than 10 ps time accuracy with these methods [6]. However, they are not suitable to measure time differences between non-sinusoidal digital signals.

Oscilloscope-based time measurements are applicable to digital signals. The achievable time measurement resolution depends amongst others on the bandwidth and the accuracy of the oscilloscope's sampling clock. The latest commercially available oscilloscopes can provide a sample clock jitter of 75 fs, with a delta-time measurement accuracy in the order of 500 fs for rail-to-rail digital signals [7]. This is just enough to measure 1.25 ps resolution of the state-of-the-art TDC [8], [9], or 550 fs resolution of the latest DTC [10], but it is insufficient to measure time delays in the order of 100 fs or below.

Aiming to overcome the oscilloscope's resolution and accuracy limits, in this paper we propose a new method for time measurements that uses a *spectrum analyzer* as principal instrument. The proposed method is specially devised for a DTC and is based on digital phase modulation, while observing the output spectrum. A DTC produces a delayed version of its clock, controlled by a digital input code. It has gained renewed interest especially in the PLL research field [2]–[4], because it can be used inside a PLL to relax the requirements of the TDC. Similarly to data converters, Integral Non-Linearity (INL) is an essential metric also for time converters (DTCs and TDCs).

The traditional way to measure the INL of a DTC is oscilloscope-based: the oscilloscope detects the time difference between the threshold-crossing points of the delayed output edges. Throughout this paper, we will refer to this procedure as the *direct* method. Alternatively, our proposed approach is an *indirect* method: instead of an oscilloscope measuring directly a delay, we use a spectrum analyzer to measure a deliberately generated spur, whose height is in a one-to-one correspondence with the delay to be measured; then, the delay is deduced and employed to calculate the INL. The frequency selectivity of this approach permits to achieve a time resolution up to a few fs.

This paper is organized as follows. Section II explains the main idea behind the proposed method. Then, the method is verified by behavioral simulations, as described in section III. In Section IV, experimental results on a high resolution DTC are presented, while conclusions are drawn in Section V.

II. Proposed Method

A. The concept

The main goal of the proposed method is to measure a DTC-INL which is too small to be measured reliably by an oscilloscope. An oscilloscope used for direct delay measurements needs wide bandwidth to avoid affecting the observed rise/fall times of the test signal, leading to high vulnerability to noise and interferences in a broad band of frequencies. In contrast, the method to be proposed relies on phase modulation of the DTC-output by means of a digitally controlled periodic delay-step, that generates a narrowband spur related to the size of that delay-step. This spur can be measured by a spectrum analyzer

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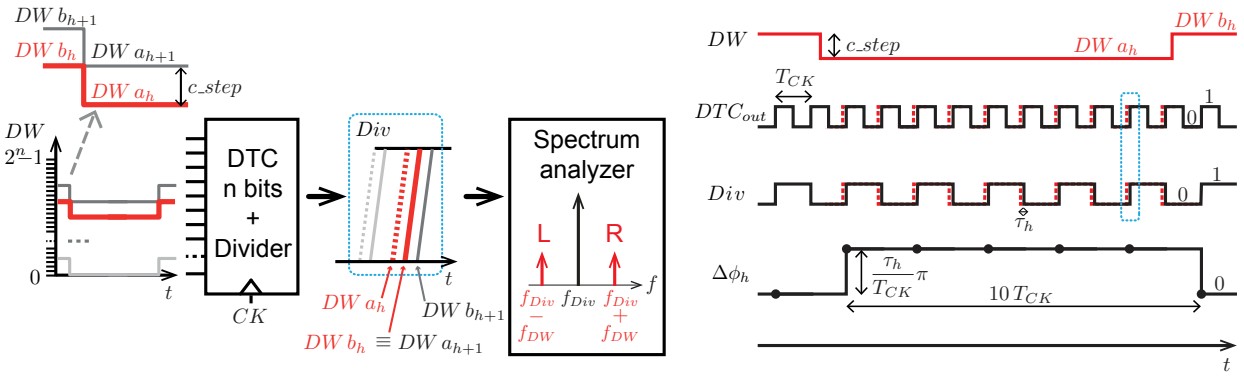

Fig. 1. Block diagram of the phase modulation setup for DTC-INL measurements, expected spectrum with left (L) and right (R) sidebands, and waveforms in time-domain.

with small resolution bandwidth, thus avoiding disturbances at all other frequencies.

The concept can be explained using the block diagram and the waveforms shown in Fig. 1. The Delay Word (DW) is the code at the digital input of the DTC and is periodically switched between two values: $DW\,a_h$ and $DW\,b_h$ (red waveform). Subscript h will be used to identify a particular starting code used for experiment h.

At the DTC output, the rising edges are delayed by a time that depends on the input code. The periodic switching between $DW\,a_h$ and $DW\,b_h$ produces a jump of the rising edge of the DTC output between two determined positions, as shown in Fig. 1. As only the edge controlled by the DTC should be detected, and not the other, a $\div 2$ frequency divider is inserted between the DTC output and the spectrum analyzer. In this way, a phase modulation of the signal Div is achieved. Note that the modulating signal DW (with frequency f_{DW}) is a *code* waveform (in DTC LSBs), because of the digital nature of the DTC input. The phase modulation appears, in the frequency domain, as a couple of sidebands, shifted by an offset frequency f_{DW} (and its harmonics) from the carrier frequency f_{Div}. These sidebands can be measured using a spectrum analyzer.

B. Analysis

The solid waveforms DTC_{out} and Div on the right-hand side of Fig. 1 are the unmodulated signals that will occur if the code applied at the DTC input is constantly equal to $DW\,b_h$. The dotted waveforms are the modulated signals: they coincide with the solid waveforms when $DW\,b_h$ is applied, but they are shifted to the dashed edges as long as $DW\,a_h$ is applied.

The frequency f_{DW} of the code waveform is chosen so that the resulting sidebands are located in an interference-free portion of the spectrum, and far enough from the carrier frequency f_{CK} to not be affected by its phase noise, including 1/f noise. After interference measurements, we chose $f_{CK} = 20 f_{DW}$, as shown in Fig. 1. However, the following analysis is independent of the choice of f_{DW}.

The waveform $\Delta\phi_h$ on the bottom right in Fig. 1 represents the phase difference between the unmodulated Div signal (constant DW) and its modulated form (DW square wave with height c_{step}), sampled at every rising edge of the Div signal. The waveform $\Delta\phi_h$ is a square wave with the same frequency as DW signal; it has 50% duty cycle and its height is $\tau_h/(2T_{CK}) * 2\pi = \tau_h/T_{CK} * \pi$, where T_{CK} is the clock period and τ_h is the delay-step produced by the code-step $c\_step = DW\,b_h - DW\,a_h$, as shown in Fig. 1. The first harmonic $\Delta\Phi_{1\,h}$ of the phase difference is given by:

$$\Delta\Phi_{1\,h} = 2\frac{\tau_h}{T_{CK}} \tag{1}$$

and can be treated as in standard phase modulation theory [11], [12], leading to a spur level relative to the carrier [dBc] given by $20log_{10}(\Delta\Phi_{1\,h}/2)$ and, therefore:

$$spur_h\left(f_{div} \pm f_{DW}\right) = 20log_{10}\left(\frac{\tau_h}{T_{CK}}\right) \qquad [dBc] \tag{2}$$

Equation (2) allows the application of a spectrum-analyzer-based time measurement, because it provides the link between the frequency-domain, in which the measurements are actually done, and the time-domain. From the spur measurement, through equation (2), we can deduce the measured delay-step τ_h associated with c_step. Next, the associated Differential Nonlinearity (DNL), expressed in seconds, can be calculated with the following:

$$DNL\,(h) = \tau_h - \tau_{id} \tag{3}$$

where τ_{id} is the ideal delay-step produced by the code difference c_step, evaluated as the average of all the values τ_h obtained. Finally, the INL can be computed from the cumulative sum of the DNL:

$$INL\,(h) = \sum_{k=0}^{h} DNL\,(k) \tag{4}$$

C. Sensitivity and Resolution

To incorporate all DTC-codes in the INL test, the best value to assign to c_step is 1 LSB. However, this choice can result in very slow measurements to get a complete INL plot, because the number of required points is $2^n - 1$ for an $n-$bit DTC, while a measurement with narrow resolution bandwidth with a spectrum analyzer takes considerable time.

If the INL-behavior of a DTC is rather smooth, its linearity can also be described with a subset of INL points, using a

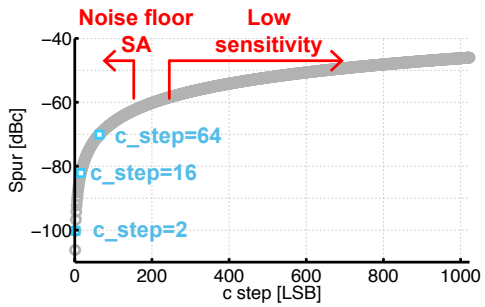

Fig. 2. Plot of $spur$ as a function of c_step, described in equation (6), for the case $n = 10$, $\tau_{FS} = 100$ps, and $T_{CK} = 20$ ns.

coarser delay-step. However, the logarithmic relation between spur and delay in equation (2) suggests that a very coarse delay-step may lead to reduced sensitivity. This is because a spectrum analyzer has a limited resolution and accuracy and at some point the variation of spur strength may be too small to be detected. In this section, we will focus on this trade-off between noise-limitations and the limited sensitivity.

The relation between input codes and delays produced by the DTC is linear:

$$\tau_h = \frac{\tau_{FS}}{2^n - 1} c\_step \tag{5}$$

where τ_h is the delay-step resulting from the application of the code difference c_step at the DTC's input, n is the DTC's number of bits, and τ_{FS} is the DTC's full-scale delay (i.e. the delay corresponding to the input code going from 0 to $2^n - 1$). Equation (2) can be rewritten in the following form:

$$spur_h\left(f_{div} \pm f_{DW}\right) = 20log_{10}\left(\frac{\frac{\tau_{FS}}{2^n-1} c\_step}{T_{CK}}\right) \quad [dBc] \tag{6}$$

where the logarithmic dependence of $spur_h$ as a function of c_step is evident, as shown in Fig. 2, for the case $n = 10$, $\tau_{FS} = 100$ ps, and $T_{CK} = 20$ ns.

The sensitivity of the method can be quantified as the variation in spur strength due to the change of the delay-step, evaluated at a certain nominal delay-step value. We can calculate it by taking the derivative of equation (2), or as a function of c_step (in LSBs), using equation (5), obtaining:

$$\Delta\, spur_h = \left[20log_{10}\left(e\right)\right] \frac{\Delta\tau_h}{\tau_h} \simeq 8.69 \frac{\Delta c\_step}{c\_step} \tag{7}$$

Equation (7) can be used to understand the limits associated with the c_step choice, highlighted in the spur curve in Fig. 2.

For a coarse c_step (around 200 LSB), the limitation is the flatness of the spur curve, i.e. a low sensitivity. As an example, with the values used for the plot in Fig. 2, for $c\_step = 200$ a deviation of 3 LSB (non-linearity) in the DTC's delay would result in only 0.13 dB spur change, which is hardly distinguishable from other environmental sources of variation (the experimentally observed uncertainty was 0.2 dB in the PXA-SA [13]).

For a c_step equal to one or a few LSBs, more INL points are available, but the main limit is the noise floor of the spectrum analyzer that can prevent it from distinguishing the low spur. However, the spectrum analyzer's noise floor can be reduced with a narrow resolution bandwidth RBW (up to −155 dBm noise floor with RBW= 1 Hz in the PXA-SA [13]).

A good value for c_step is, therefore, the minimum value needed to distinguish the spur from the noise floor. For example, with RBW= 200 kHz, the spectrum analyzer's noise floor is −102 dBm for [13]; with a 3 dBm carrier and equation (6), the value $c\_step = 2$ LSB would produce a distinguishable spur of −100 dBc= −97 dBm, with a resulting time resolution of 196 fs. An average between multiple measurements is needed to reduce the variability due to noise. By pushing the noise floor to the minimum, it becomes possible to detect a −140 dBc spur, corresponding (from equation (2)) to only 2 fs time delay. This value is far beyond the hundreds of fs values achievable with top-class oscilloscopes commercially available [7].

D. Algorithm

Aiming to detect sub-ps INL, the essence of the proposed measurement method is to always generate the same delay τ_h by changing the input waveform. In this way, the method's sensitivity in equation (7) is the same during the measurements, and other variations are minimized. Depending on the spur strength, the measured delay can be higher or lower than its nominal value and this determines the polarity of the INL curve.

The algorithm of the proposed method is based on these considerations together with equations (2)-(4). It consists of the following steps, partly shown in Fig. 1:

1) divide the overall code range into equal intervals of height c_step, covering codes from 0 up to $2^n - 1$;
2) start with index $h = 0$
3) apply the DW waveform h and measure $spur_h$;
4) calculate τ_h by applying equation (2);
5) increase h and repeat steps 3 to 4, until all values of h have been considered;
6) evaluate τ_{id} as the average of all the values τ_h;
7) calculate DNL using equation (3) and INL using equation (4).

Notice that in step 1 the DW waveforms differ only by their lower ($DW\, a_h$) and upper ($DW\, b_h$) values. Therefore, each waveform is identified by the index h. The upper value of one DW waveform must coincide with the lower value of the next one, that is $DW\, b_h = DW\, a_{h+1}$; this allows us to obtain INL as cumulative sum of DNL.

Ideally, for all the values h, the measured spur, and therefore the delay-step τ_h, will be always the same. However, due to the circuit nonlinearity, the values τ_h are dependent on the index h.

III. Simulations

We tested the proposed method by running behavioral simulations. The goal is to verify the equations presented in section II and to check whether the conventional direct and our indirect method lead to the same INL results.

To compare results both in time and in frequency domain, the behavioral simulations need to have enough time resolution, to distinguish the delay of the DTC in the time

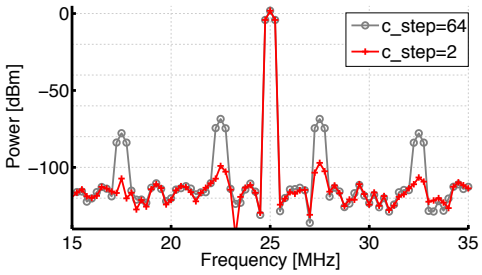

Fig. 3. Simulated spectrum of Div signal, with $c\_step = 2$ LSB and $c\_step = 64$ LSB applied at the DTC input.

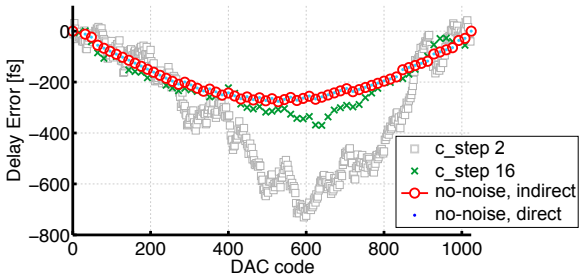

Fig. 4. Simulated INL, for different values of c_step and for direct and indirect methods. The values of c_step used are highlighted on Fig. 2.

domain, but also long simulation time, to produce a spectrum with enough frequency resolution. For these simulations, we chose a time resolution of 20 fs and a simulation time of 4μs, corresponding to a frequency resolution of 250 kHz.

The simulated DTC has $n = 10$ bits, a full-scale delay $\tau_{FS} = 100$ ps, and a clock with period $T_{CK} = 20$ ns. A quadratic nonlinearity is inserted on purpose in the model with maximum INL of 250 fs. The frequency of the DW waveform is set to $f_{DW} = 2.5$ MHz, the Div signal has $f_{Div} = 25$ MHz. White noise has been added to model a -120 dBm spectrum analyzer's noise floor.

Fig. 3 shows the simulated spectrum of the divider output waveform, as it would appear on the screen of a spectrum analyzer, for two quite different values of c_step within the limits discussed in section II-C, to clearly show the spur differences. As expected, the spectrum exhibits the carrier tone at $f_{Div} = 25$ MHz and two sidebands at $f_{Div} \pm f_{DW}$ (first harmonics), namely 22.5 MHz and 27.5 MHz. For $c\_step = 64$ LSB, the figure also shows the third harmonics at $f_{Div} \pm 3f_{DW}$, due to the square wave shape of the modulating signal; these higher harmonics do not add more information and they are not considered for the measurements. The simulated first-harmonic sidebands are -100.6 dBc for $c\_step = 2$ LSB and -70.4 dBc for $c\_step = 64$ LSB, matching the values obtained from equation (6).

Fig. 4 aims to compare the INL using both the direct and the indirect methods. The figure also shows the effect on the INL curve by two c_step values in the trade-off range discussed in section II-C. For simplicity, the two methods are compared in the noiseless case, with $c\_step = 16$ LSB. The shape of the noiseless INL curve (circles) exhibits the quadratic nonlinearity inserted on-purpose in the behavioral model. The algorithm of section II-D was used to calculate it, where one spectrum for each point of the INL curve has been obtained. The small-dotted curve in Fig. 4 refers to the direct method. It has been derived by plotting the DTC output as a function of time, then evaluating the time instants t_k where the rising edges cross a 700 mV voltage threshold and finally using the standard formulas from [14]. The INL from the two methods differ by at most 1.1 fs, due presumably to numerical noise, i.e. only 1% of 1 DTC LSB.

By adding -120 dBm white noise in the simulations, we can investigate the effect of different code-step choices on the INL. For $c\_step = 2$ LSB, the first spur is close to the simulated noise floor, as shown in Fig. 3, resulting in a detailed (511 points) but noisy INL plot in Fig. 4. The drift due to high-frequency noise can be reduced by obtaining multiple INL plots and averaging them at each code. However, as simulations already take multiple days, no averages for any value of c_step have been done here. Instead a higher value of $c\_step = 16$ LSB was used, resulting in a less noisy result closer to the true INL. A larger c_step produces less INL points but is more robust to noise.

IV. Measurements

We actually developed this INL-measurement method to allow for measuring the INL of a record high-resolution DTC, implemented in CMOS 65 nm technology that exploits a constant slope principle [15]. Measuring the DTC with on-chip DAC using the direct method failed, because of the DTC resolution in the order of tens of fs. Fig. 5 shows the block scheme of the measurement setup. The DTC realizes a delay using a ramp waveform with a fixed slope, starting from an initial voltage defined by a Digital-to-Analog Converter (DAC). The delay is controllable by the DAC voltage, which can either be on-chip or external. The digital interface of this chip is not fast enough to support MHz modulation of the DAC code. Instead, an external DAC (Agilent M8190A Arbitrary Waveform Generator) was used in these experiments to produce a square wave (V_{ext}) that periodically switches between two voltage levels, effectively implementing the delay-step, and the chip acts as a Voltage-to-Time Converter (VTC). The procedure is the same as described in section II; compared to the scheme in Fig. 1, the only difference here is that the DW waveforms with height c_step are now converted into V_{ext} square waves with height v_step, through the external DAC. The V_{ext} jitter did not affect the sideband position during the measurement. We used the 10 MSB-bits of the Agilent M8190A 14-bit DAC. We checked its INL was below +/−0.5 LSB (0.05% referring to 10-bit full-scale) so it is not the bottleneck in our DTC-INL measurement. Data averaging can reduce the DAC thermal noise, however some 1/f noise remains.

The measurements are done with $f_{CK} = 50$ MHz, $f_{Div} = 25$ MHz, and using 40 values for the square waves V_{ext} with $f_{V_{ext}} = f_{DW} = 2.5$ MHz and height $v\_step = 0.98$ mV each. The choice of v_step is equivalent to c_step of about 25 LSB in a 10-bit full scale, on the same order as the c_step choices in section III. A smaller v_step or c_step would result in more

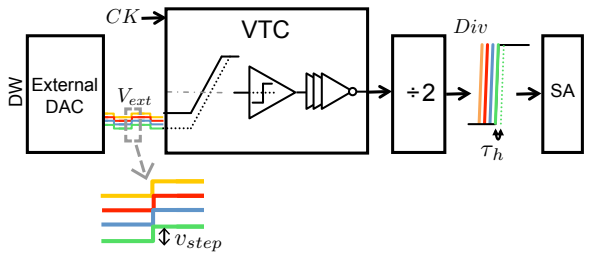

Fig. 5. Setup used to measure the INL of the DTC [15] (acting as a VTC), with the proposed method.

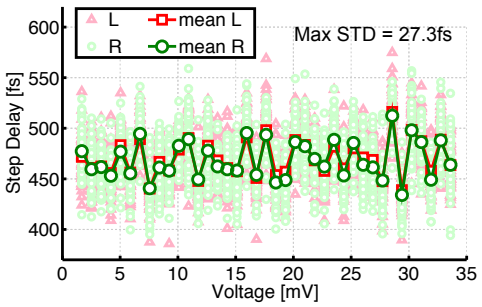

Fig. 6. Measured delay-step produced by the DTC [15], as a function of the upper voltage of the modulating square waves; 50 repetitions for each delay.

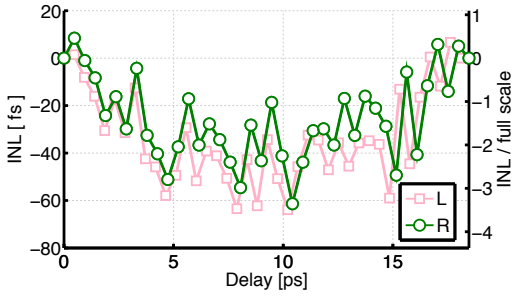

Fig. 7. Measured INL, produced by the DTC [15], set with full-scale 19 ps, using the proposed method ($V_{ext} = 0$ to 33.6mV with steps of 0.98mV).

measured INL points but is less robust to noise and requires longer measurement time. The algorithm in section II-D is repeated 50 times, leading to 50 sweeps through the set of 40 square wave voltages. The DTC in measurement has a tunable full-scale delay $19-189$ ps, and we use it here at its minimum delay to apply the method in the most challenging case. The spectrum analyzer's resolution bandwidth is set to 10 kHz, leading to -115 dBm noise floor and -118 dBc minimum detectable spur (assuming SNR$=$ 0 dB and 3 dBm carrier), and resulting in 25 fs time resolution from equation (2).

Fig. 6 shows the 40 measured delays and indeed shows an average of about 475 fs (19 ps/40). The delays have been calculated separately for the left (L) and the right (R) sideband. The maximum standard deviation is 27.3 fs. The resulting averaged INL curve is shown in Fig. 7. The two y-axes refer to the absolute INL in fs, and its normalized value with respect to the DTC full-scale delay, respectively. The maximum INL value is 64 fs and corresponds to 0.34% in the normalized scale. The difference between left and right sidebands produces a maximum INL difference of 20 fs, that is less than the standard deviation 27.3 fs of the time step measurement. Therefore, in this case, either the left or the right spurs produce a sufficiently precise INL plot. However, depending on the implementation of the DTC, if there is also a coexisting amplitude modulation, the delay measured using the left spur would be higher than the one for the right spur. In such a case, averaging between left and right spurs produces the proper result.

V. Conclusion

In this paper, we have presented a very sensitive method to measure the INL of DTCs, based on phase modulation, and capable to achieve a time resolution of a few fs, which is 1-2 orders of magnitude better than what is achievable with high-speed sampling oscilloscope. The new method has been verified with behavioral simulations, and used to measure the INL of a high-resolution DTC with 19 ps full-scale. An INL in the order of 50 fs was measured, with a standard deviation of 27.3 fs.

References

[1] G. Roberts and M. Ali-Bakhshian, "A brief introduction to time-to-digital and digital-to-time converters," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 57, no. 3, pp. 153–157, March 2010.

[2] V. Chillara, Y.-H. Liu, B. Wang, A. Ba, M. Vidojkovic, K. Philips, H. de Groot, and R. Staszewski, "9.8 an 860 uw 2.1-to-2.7ghz all-digital pll-based frequency modulator with a dtc-assisted snapshot tdc for wpan (bluetooth smart and zigbee) applications," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, Feb 2014, pp. 172–173.

[3] N. Pavlovic and J. Bergervoet, "A 5.3ghz digital-to-time-converter-based fractional-n all-digital pll," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, Feb 2011, pp. 54–56.

[4] K. Raczkowski, N. Markulic, B. Hershberg, J. Van Driessche, and J. Craninckx, "A 9.2-12.7 ghz wideband fractional-n subsampling pll in 28nm cmos with 280fs rms jitter," in *Radio Frequency Integrated Circuits Symposium, 2014 IEEE*, June 2014, pp. 89–92.

[5] B. B. O'Brien, "Simple technique for high-resolution time-delay and group-velocity measurements at radio frequencies," *Instrumentation and Measurement, IEEE Transactions on*, vol. 18, no. 3, pp. 160–162, Sept 1969.

[6] X. Zhu, Y. Li, S. Yong, and Z. Zhuang, "A novel definition and measurement method of group delay and its application," *Instrumentation and Measurement, IEEE Transactions on*, vol. 58, no. 1, pp. 229–233, Jan 2009.

[7] "Ininiium z-series oscilloscopes," Keysight. [Online]. Available: http://literature.cdn.keysight.com/litweb/pdf/5991-3868EN.pdf

[8] N. Andersson and M. Vesterbacka, "A vernier time-to-digital converter with delay latch chain architecture," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 2014, Accepted for publication.

[9] K. Kim, W. Yu, and S. Cho, "A 9 bit, 1.12 ps resolution 2.5 b/stage pipelined time-to-digital converter in 65 nm cmos using time-register," *Solid-State Circuits, IEEE Journal of*, vol. 49, no. 4, pp. 1007–1016, April 2014.

[10] N. Markulic, K. Raczkowski, P. Wambacq, and J. Craninckx, "A 10-bit, 550-fs step digital-to-time converter in 28nm cmos," in *ESSCIRC (ESSCIRC), 2014 Proceedings of the*, Sept 2014.

[11] S. Haykin, *Communication Systems*, 4th ed. Wiley, 2000.

[12] S. L. J. Gierkink, "Low-spur, low-phase-noise clock multiplier based on a combination of pll and recirculating dll with dual-pulse ring oscillator and self-correcting charge pump," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 12, pp. 2967–2976, Dec 2008.

[13] "N9030a pxa specifications guide," Keysight. [Online]. Available: http://literature.cdn.keysight.com/litweb/pdf/N9030-90017.pdf

[14] F. Maloberti, *Data Converters*, 1st ed. Springer, 2007.

[15] J. Z. Ru, C. Palattella, E. Klumperink, and B. Nauta, "A high-linearity digital-to-time converter technique: Constant-slope charging," *Solid-State Circuits, IEEE Journal of*, Accepted for publication.