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A sensitivity analysis of SPICE parameters using an eleven-stage ring oscillator

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A Sensitivity Analysis of SPICE Parameters Using an Eleven-Stage Ring Oscillator

JANET M. CASSARD

Abstract—**SPICE is a circuit simulator which predicts node voltages and currents as a function of time from device model parameters. Model parameters are determined by the manufacturing process. Process-induced variations in these parameters occur within a chip or from chip to chip and cause corresponding variations in circuit performance. Values for the model parameters used in simulators are usually obtained from measurements on test structures which are found along the periphery of the circuit or in test chips located at several sites on the product wafer. Because of the spatial separation between test structures and the circuits of interest, differences between measured and simulated performance can occur. This paper presents examples of how well model parameters extracted from a test chip can predict the ac response of a dynamic circuit element (ring oscillator) on the same wafer. Simulation results show which model parameters are critical to performance. A comparison between measurement and simulation results is given and the importance of intra-chip and intra-wafer parameter variations is discussed. For the samples tested, the polysilicon gate linewidth variation was determined to be the primary cause of the ring oscillator frequency variation.**

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NOMENCLATURE

Symbol	Units	Identification
$CGD0$	F/m	Gate-to-drain overlap capacitance per meter of channel length.
KP_n	A/V^2	$\left(\frac{\text{n-channel transconductance}}{V_D}\right)\left(\frac{L_n}{W_n}\right)$.
KP_p	A/V^2	$\left(\frac{\text{p-channel transconductance}}{V_D}\right)\left(\frac{L_p}{W_p}\right)$.

L_n	μm	Channel length for n-channel devices.
L_p	μm	Channel length for p-channel devices.
LD	μm	Lateral diffusion.
t_{ox}	nm	Oxide thickness.
V_D	V	Drain voltage.
V_{DD}	V	Power supply voltage.
V_{SS}	V	Ground voltage.
$VT0_n$	V	Threshold voltage for n-channel devices.
$VT0_p$	V	Threshold voltage for p-channel devices.
W_n	μm	Channel width for n-channel devices.
W_p	μm	Channel width for p-channel devices.

I. Introduction

BEFORE fabricating complex VLSI circuits it is important to identify errors in the circuit design. The effectiveness of SPICE in simulating actual circuit performance from a set of device model parameters is influenced by process-induced variations that affect these input parameters. In this paper, the critical input parameters are identified, and the effect of their variation on the simulation is estimated. A test chip containing ring oscillators and test structures for extracting the model parameters for SPICE was designed and fabricated in a p-well CMOS bulk local oxide-isolated process at two silicon foundries using 5-μm design rules [1]. An automated parametric test system was used to measure the electrical model input parameters, and the nonelectrical parameters were determined from physical measurements. The mean and standard deviation of each parameter was determined. A manual test system was used to measure the frequency of an eleven-stage ring oscillator.

The ring oscillator was simulated, using SPICE 2G.4, to determine the sensitivity of the ac oscillation frequency to fixed model-parameter variations. The model parameters critical to the frequency of oscillation were identified, and measured variations in these critical model parameters were used to examine the variations in simulated frequency.

This paper compares the measured ring oscillator performance to the simulated performance. Differences between the measured and simulated oscillation frequency means are due to the inaccuracy of the SPICE model (e.g., in scaling), deficiencies in the design of the test structures used for extracting the SPICE parameters, and deficiencies in measurement methods. Differences between the measured and simulated ranges are due to intrachip and intrawafer parameter variations. The results of this study show that measured variations in approximately one-fourth of the SPICE model parameters, those critical to ac response, provide an adequate model for the measured ring oscillator frequency range.

II. Experimental Procedure and Results

The wafers studied contain 32 or 21 test chips for foundries A or B, respectively. Each chip includes identical MOSFET's systematically placed across the test chip, cross-bridge resistors [2], [3], capacitors, and ring oscillators. The chip was designed in a 2 by N probe pad configuration [4], [5] to maximize testing efficiency. The wafers were measured with an automated parametric test system, and test results were analyzed using statistical evaluation techniques [6]. The test methods for obtaining the model parameters for SPICE can be found elsewhere [7]–[9]. The test results for selected parameters are shown in Table I. A manual station was used to measure the ring oscillator frequency. A low-capacitance probe (0.1 pF) was used to probe the output in order to minimize the capacitive loading.

TABLE I
A Comparison of Critical Input Parameter Values for Samples from Two Silicon Foundries

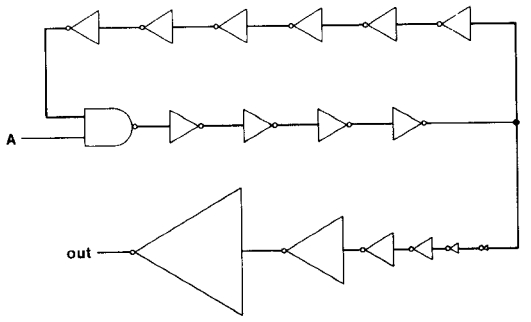
Parameter	Value for sample from Foundry A		Value for sample from Foundry B	
V_{DD}	5 00	V	5.00	V
L_p	5 00 ± 19	μm	5 00 ± .15	μm
L_n	5.00 ± .27	μm	5 00 ± .25	μm
t_{ox}	75 0 ± 5.0	nm	87.5 ± 2 5	nm
KP_n	33.9 ± 0 5	$\mu A/V^2$	33.5 ± 0 7	$\mu A/V^2$
LD	0 58 ± 06	μm	0 90 ± .09	μm
KP_p	14.0 ± 0.3	$\mu A/V^2$	11.3 ± 0 5	$\mu A/V^2$
W_n	78.2 ± 0 3	μm	78.2 ± 0 3	μm
$VT0_n$	0 96 ± 02	V	0 82 ± 06	V
$CGD0$	267 ± 45	pF/m	355 ± 46	pF/m
$VT0_p$	−0.88 ± .01	V	−0.66 ± .09	V

A ring oscillator was chosen for this analysis because it is a simple circuit, it is used widely on test chips for monitoring process variations, and its oscillation frequency is sensitive to SPICE model parameters. An eleven-stage ring oscillator was designed since initial simulations, for the process and design employed, indicated that the output waveform would achieve maximum oscillation amplitude for that odd number of stages. Also, a prime number of stages was chosen to help suppress the occurrence of harmonics that might otherwise occur for the relatively small number of stages employed [10].

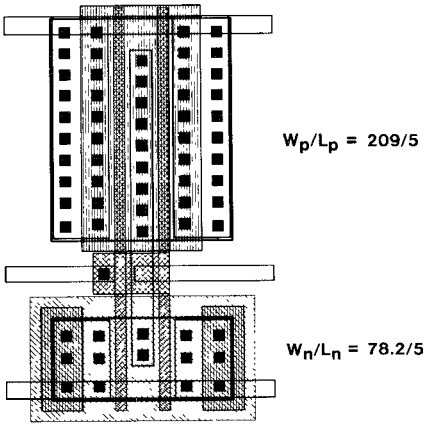
The ring oscillator consists of three basic elements: an inverter, a NAND gate, and an output buffer. Ten inverters and one NAND gate are tied together forming the circuit. The NAND gate is used in place of one inverter to prevent multiple oscillations in the ring [10]. The six-stage output buffer is tied to one node of this ring. In each successive stage of the output buffer, the channel widths are twice as large as the previous stage to minimize the capacitive loading introduced by the measurement probe [11] and to make efficient use of silicon area. A block diagram of the ring oscillator is shown in Fig. 1 along with the circuit diagram of one inverter.

III. Simulations

To determine the sensitivity of SPICE simulations to device model parameter variations, two groups of simulations were performed. The first simulations determined the sensitivity of the frequency of the ring oscillator to a fixed variation in each model parameter. From this, a set of



(a)



(b)

Fig. 1. (a) A block diagram of the ring oscillator is shown along with (b) the circuit diagram of one inverter.

critical parameters, or parameters which had the greatest effect on the output was selected. Based on these results a second group of simulations was performed using the variations in model parameters measured for the wafers from the two foundries. This was done to predict the range over which the measured frequency would be expected to vary. All simulations were performed using MOS2 in SPICE 2G.4 [7], [8], [12]–[14]. Simulated and measured waveforms are plotted in Fig. 2.

For the first group of simulations, all model parameters, including the channel lengths, the channel widths, the temperature, and the power supply voltages, were individually varied ± 10 percent about the measured mean and the frequencies recorded. This resulted in an ordered list of parameters ranked according to the sensitivity of SPICE to their variation. For this work, the critical parameters were defined as those which caused a frequency variation of more than 3.5 percent when the model parameter was varied. These critical parameters and the corresponding simulated frequency ranges obtained for the wafers from the two silicon foundries are listed in Table II. To obtain a realistic estimate of the effect that each critical parameter has on the frequency, for the processes used in this work, each parameter was also individually varied ± 1 measured standard deviation. The frequency results are also included in Table II.

To determine the range over which the measured frequency would be expected to vary, a second group of simulations was performed in which all of the critical

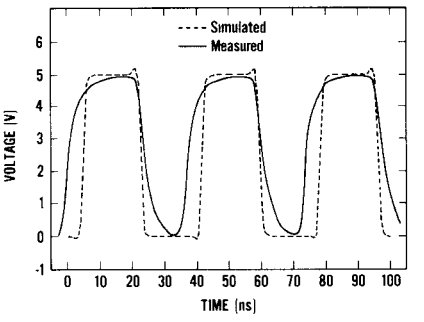


Fig. 2. The measured and simulated ring oscillator waveforms are plotted on the same axes.

TABLE II
A COMPARISON OF SIMULATED FREQUENCY RANGES (IN MEGAHERTZ) FOR SAMPLES FROM TWO SILICON FOUNDRIES WHEN THE INPUT PARAMETER IS VARIED ± 10 PERCENT OR $\pm \sigma$

(The parameters listed are the critical parameters because they cause a frequency variation of more than 3.5 percent when the parameter is varied ± 10 percent about its measured mean.)

	Foundry A		*Foundry B*	
Parameter	$\pm 10\%$ *Range*	$\pm\sigma$ *Range*	$\pm 10\%$ *Range*	$\pm\sigma$ *Range*
V_{DD}	7.9	–	8.2	–
L_p	6.7	2.4	8.6	2.6
L_n	5.2	2.9	6.9	3.5
t_{ox}	3.2	2.2	3.0	0.8
KP_n	3.2	0.4	3.6	0.7
LD	2.8	2.8	5.4	5.4
KP_p	2.6	0.4	3.4	1.4
W_n	2.0	0.2	2.1	.04
$VT0_n$	1.5	0.4	1.5	0.9
$CGD0$	1.3	1.8	1.9	2.6
$VT0_p$	1.1	0.2	0.7	1.1
Simulated Mean	29.7 *MHz*		35.6 *MHz*	

TABLE III
A COMPARISON OF MEASURED VERSUS SIMULATED MEAN VALUES AND RANGES FOR SAMPLES FROM TWO SILICON FOUNDRIES

(Due to the low percent difference between the measured and simulated mean values, the intrawafer mean of each parameter is a reasonable estimate of the actual model parameter. For the measured ring oscillator frequency range, the intrawafer variations in the critical parameters provide an adequate model.)

	Foundry A	*Foundry B*
Measured Mean Value	30.7 *MHz*	34.3 *MHz*
Simulated Mean Value	29.7 *MHz*	35.6 *MHz*
Percent Difference in the Means	3.4 %	3.7 %
Measured Range	± 6.3 *MHz*	± 7.0 *MHz*
Simulated Range	± 7.0 *MHz*	± 9.9 *MHz*
Percent Difference in the Ranges	10.0 %	29.3 %

parameters were varied ± 1 standard deviation, representing the intra-wafer variations, and the highest and lowest frequencies determined. This approach assumes the parameters are statistically independent. These results are given and compared in Table III with actual measurements from ring oscillators on the wafer.

IV. DISCUSSION

Two types of deviations exist between the measured and simulated results. They are: 1) the differences between the measured frequency mean and the simulated frequency

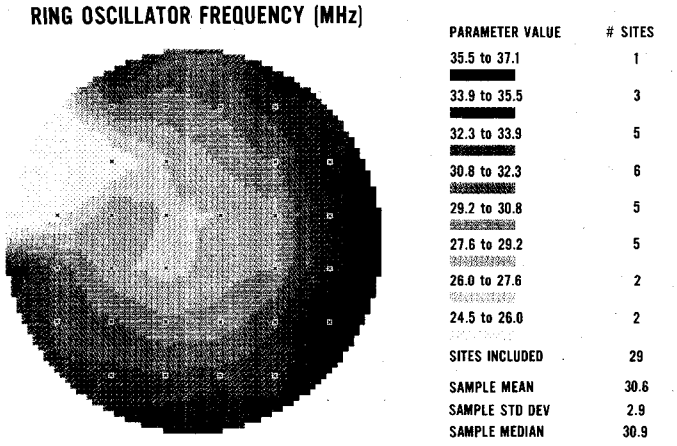


Fig. 3. A ring oscillator frequency wafer map shows the test site locations and the intrawafer parameter variations. An approximate inverse correlation exists between the ring oscillator frequency and the polysilicon gate linewidth, Fig. 4, suggesting that the channel length variation is the primary cause of the frequency variation.

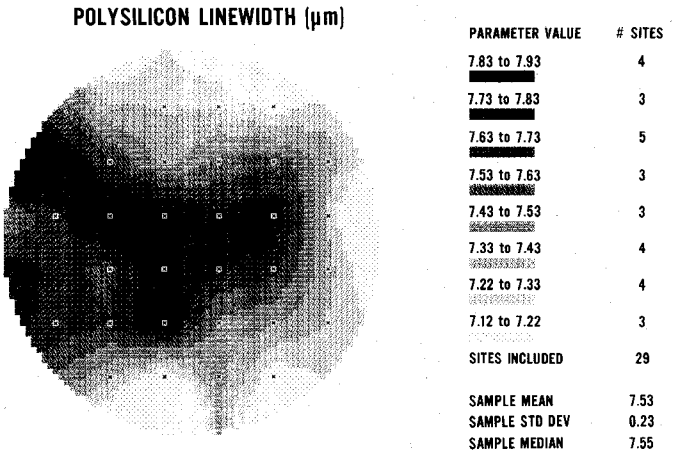


Fig. 4. A polysilicon gate linewidth wafer map shows the test site locations and the intrawafer parameter variations.

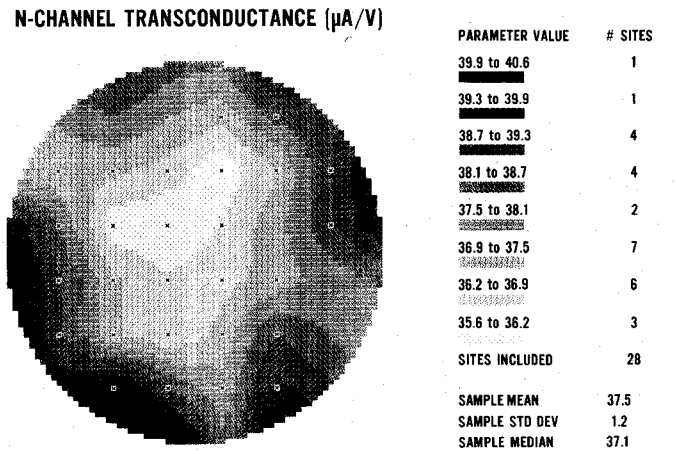


Fig. 5. A transconductance wafer map for an n-channel MOSFET shows the test site locations and the intrawafer parameter variations. An approximate inverse correlation exists between the transconductances (n- and p-channel) and the channel length supporting the conclusion that the principle cause of the intrawafer frequency variation is the intrawafer polysilicon gate linewidth variation which in turn causes a corresponding variation in the n- and p-channel transconductances.

utilizing the mean values of all the model parameters, and 2) the simulated range in which the measured results are expected to be found and the actual measured range.

Several factors can cause differences between the simulated and measured results. The first type of deviations can be due to the inaccuracy of the SPICE model, deficiencies in the design of test structures used for extracting the SPICE parameters, and deficiencies in measurement methods. The results given in Table III for the two silicon foundries show close agreement between the measured and simulated means.

The second type of deviations can be due to intrachip and intrawafer parameter variations which result from processing variations over the wafer. In Table III, the measured range of values is compared to the simulated range. For this work, the simulated range is obtained by using the critical model parameters with their corresponding measured standard deviation, or intrawafer variations, which produce the highest and lowest frequencies. Hence, the assumption that the parameters are statistically independent yields a worst case range. Therefore, the simulated range is larger than the measured range.

A wafer map illustrating the intrawafer ring oscillator frequency variations for the sample from foundry *A* is shown in Fig. 3. The map was produced using STAT2 [6]. To identify the cause of these frequency variations, wafer maps were made for several critical input parameters. A polysilicon gate linewidth wafer map is shown in Fig. 4 for structures designed to have a linewidth of 8.0 μm. It is assumed that the same variation would exist for 5-μm structures. An approximate inverse correlation exists between the polysilicon gate linewidth, also called the channel length, and the ring oscillator frequency suggesting that the channel length variation is the primary cause of the frequency variation. To support this conclusion, transconductance wafer maps for n- and p-channel MOSFET's, shown in Figs. 5 and 6, respectively, show an approximate inverse correlation with the channel length. It is, therefore, concluded that the principle cause of the intrawafer frequency variation is the intrawafer polysilicon gate linewidth variation which in turn causes a corresponding variation in the n- and p-channel transconductances. To obtain tighter control on the circuits performance and hence increase the reliability of the process, it is important to minimize polysilicon linewidth variations across a wafer.

Variations of a given parameter within a chip (intrachip variations) can lead to differences between the model parameters measured and their corresponding value in the actual circuit. To estimate the magnitude of these differences, identical MOSFET's placed across a test chip were tested and the intrachip variations in selected critical parameters measured. The devices probed in these MOSFET arrays had a channel length of 8.0 μm and a channel width of 77.0 μm. Ten n-channel and ten p-channel arrays were placed across each test chip. The wafer was arranged such that six test chips were evenly spaced across the diameter of the wafer. Data values from the 8.0-μm devices are taken from all of the MOSFET's across the diameter of the wafer. The n- and p-channel transconductances are plotted as a function of wafer position in Figs. 7

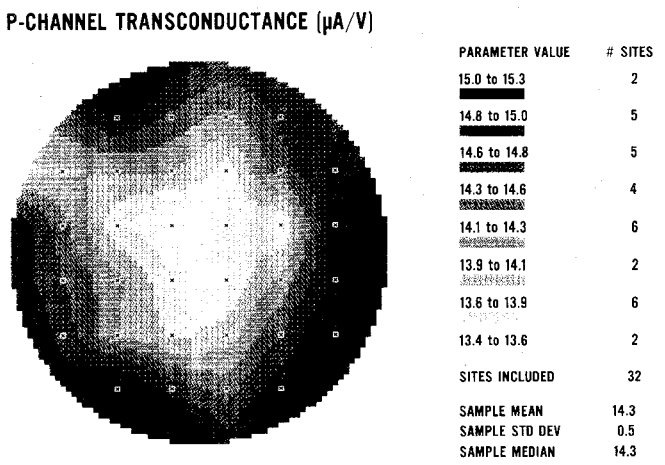


Fig. 6. A transconductance wafer map for a p-channel MOSFET shows the test site locations and the intrawafer parameter variations.

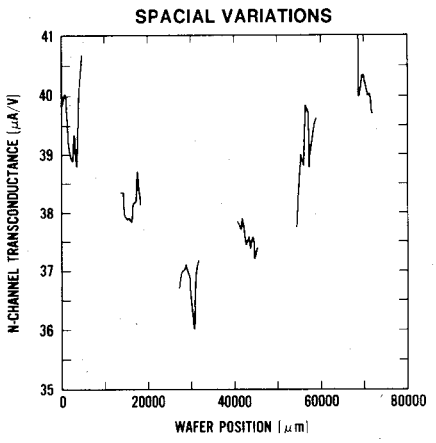


Fig. 7. The n-channel transconductance is plotted against the position across the diameter of a wafer. While the overall intrawafer variation is similar to that seen in Fig. 5, an intrachip variation in the parameter is also observed. The measured intrachip variations suggest that SPICE simulations can be influenced by the intrachip variation in the critical input parameters.

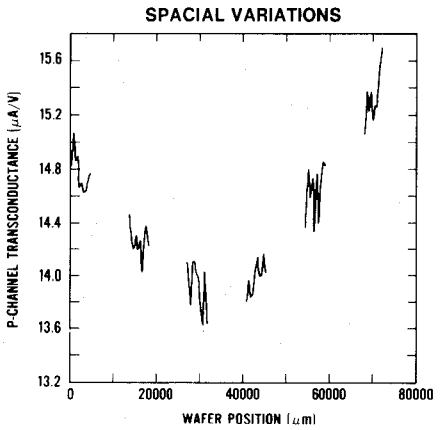


Fig. 8. The p-channel transconductance is plotted against the position across the diameter of a wafer.

and 8, respectively. While the overall intrawafer variations seen in Figs. 7 and 8 are similar to those seen in their corresponding wafer maps, Figs. 5 and 6, an intrachip variation in the parameter is also observed. To identify the cause of these variations, further analysis involving additional test structures is needed. The measured intrachip variations suggest that SPICE simulations can be influenced by the intrachip variation in the critical input parameters.

V. Conclusions

A sensitivity analysis was performed and the critical parameters, which are shown in Table I, were identified and then measured. The intrawafer variations of these parameters are sufficient for determining the range within which to expect the measured frequency of a ring oscillator. The magnitude of the simulated range is approximately the magnitude of the spread of the frequency data. Intrawafer process variations account for this range in the measured frequency results.

Due to the lack of proximity between the test structures from which the SPICE parameters are obtained and the ring oscillators, intrachip variations can cause a difference between the measured and simulated ring oscillator frequency.

The conclusions that can be drawn from this work based on the samples tested are: 1) there is a subset of the total SPICE parameters which have the greatest effect on the simulation; 2) the intrawafer mean of each parameter is a reasonable estimate of the actual model parameter; and 3) the intrawafer variations in the critical parameters can account for a frequency range that is approximately equal to the measured frequency range. For the samples tested, it was determined that: 1) the polysilicon gate linewidth is indirectly proportional to the frequency and was the primary cause of the frequency variation; and 2) intrachip parameter variations can influence SPICE sensitivity.

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(*End of Special Papers Section.*)

Regular Papers

Techniques for a 5-V-Only 64K EPROM Based Upon Substrate Hot-Electron Injection

JAMES L. McCREARY, MEMBER, IEEE, BOAZ EITAN, MEMBER, IEEE, AND DANIEL AMRANY

Abstract—**A 64K EPROM based upon substrate hot-electron injection was designed and fabricated. 5-V-only programming was demonstrated by on-chip charge pumps. The typical programming rate was approximately 1 V/ms. Sense amplifier improvements provided 4-mV offset, 52-dB PSRR, and 60-dB CMRR.**

I. Introduction

CONVENTIONAL EPROM products have demonstrated the manufacturability and reliability of the channel-hot-electron programming technique. Programming cycle time less than 20 ms and better than 10-year retention are now industry standards. This paper describes the evaluation of a 5-V-only 64K EPROM based upon substrate hot-electron programming.

Conventional EPROM's use the method of channel hot-electron (CHE) programming. This involves the generation of hot-electrons in the high-field region between the pinched-off channel and the drain. Electrons with sufficient energy have a small probability of being injected across the thin oxide to the floating gate, thereby programming the device (increasing the threshold voltage). The efficiency of this injection process is low. This may be improved by applying large drain and gate voltages, but this results in high drain current. Consequently, one disadvantage of the CHE approach is that it does not allow 5-V-only operation but requires external high-voltage sup-

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