A Seven-Junction Electron Pump: Design, Fabrication, and Operation

Mark W. Keller, John M. Martinis, Andrew H. Steinbach, and Neil M. Zimmerman

***Abstract*—We have developed a seven-junction electron pump for use in a new standard of capacitance based on measuring the voltage produced when a known charge is placed on a capacitor. This new pump, with an error per pumped electron of 15×10^{-9}, is about 30 times more accurate than a five-junction pump made previously at NIST. By careful design of the pump geometry, we have reduced the effect of cross capacitance and simplified device operation. Our fabrication recipe produces small, stable tunnel junctions relatively quickly and reliably. We have developed a method of tuning the pump for highly accurate electron counting. This tuning can be quickly repeated whenever fluctuations in background charges degrade accuracy.**

I. Introduction

THE ELECTRON pump consists of a chain of metal islands separated by tunnel junctions, with a gate electrode coupled capacitively to each island [1]. Each island's total capacitance is small enough that the Coulomb charging energy required to add one electron is much larger than the thermal energy at a temperature of about 0.1 K [2]. A sequence of voltage pulses applied to the gate electrodes manipulates the Coulomb blockade and causes a single electron to tunnel through each junction in the chain, thus "pumping" one electron through the device. Using the pump as an electron counter, we can realize a primary capacitance standard by pumping a known number of electrons onto a capacitor and measuring the voltage that develops across the capacitor [3]. NIST is currently working to develop such a standard [4], [5]. A long-term metrology goal is to combine the new capacitance standard with the calculable capacitor and the Josephson voltage standard to achieve a new measurement of the fine structure constant [3].

The proposed capacitance standard requires pumping $\sim10^8$ electrons onto a 1 pF capacitor with an uncertainty in the number of electrons of ±1. Thus the pump must have an error per pumped electron of about 10^{-8}. The pump must also have a small leakage rate when the gate pulses are turned off (the hold mode) so that the charge on the capacitor remains fixed while the voltage is measured. In previous work [6], a five-junction pump was operated with an error per electron of about 500×10^{-9} and a hold time of about 10 s. The seven-junction pump described in this paper has an error per electron of 15×10^{-9} and a hold time of about 600 s. Accuracy measurements over a range of pumping speed and temperature have been described elsewhere [7]. Here we discuss several design considerations, give details of the fabrication process, and describe our procedures for operating the electron pump with high accuracy.

Manuscript received June 20, 1996; revised October 1, 1996.

M. W. Keller, J. M. Martinis, and A. H. Steinbach are with the National Institute of Standards and Technology, Boulder, CO 80303 USA (e-mail: mark.keller@boulder.nist.gov).

N. M. Zimmerman is with the National Institute of Standards and Technology, Gaithersburg, MD 20899 USA.

Publisher Item Identifier S 0018-9456(97)02153-0.

II. Pump Design

We have made several refinements in order to make the pump easier to fabricate and operate. Most of the design considerations for the pump are also important for other SET devices.

A. Capacitance Modeling

In designing the pump, it is necessary to calculate the capacitances for various arrangements of metal film electrodes on a substrate. We use a computer program to calculate the capacitance between all pairs of conductors in an arbitrary two-dimensional pattern, assuming a dielectric constant that is the average of that of the substrate and vacuum. Each conductor consists of multiple panels, and we calculate the charge induced on each panel when one conductor is held at unity potential and the others are held at zero. The program gives approximate results that are adequate for quickly exploring many possible designs. All capacitance values given in this section were calculated using this program.

B. Stray Capacitance

In order to maximize the Coulomb blockade and thus minimize unwanted tunneling events, the total capacitance of each island in the pump must be small [2]. The island capacitance is determined by the junction capacitance $C_{\rm j}$, the gate capacitance $C_{\rm g}$, the stray capacitance to all nearby conductors $C_{\rm stray}$, and the self capacitance of the island $C_{\rm self}$. Fabrication considerations restrict $C_{\rm j}$ to values larger than about 0.2 fF ($\approx$ 50 nm $\times$ 50 nm junctions), and all other capacitances should be made much smaller than $C_{\rm j}$ to simplify theoretical analysis of the pump. $C_{\rm g}$ can easily be made less than 0.1 $C_{\rm j}$. $C_{\rm self}$ can be made small be reducing the island size to about 1 μm. $C_{\rm stray}$ can be reduced by using a substrate with a small dielectric constant.

The arrangements of islands and gates for the five-junction and seven-junction pumps are shown in Fig. 1. The five-junction pump was made on a sapphire substrate with a dielectric constant of $\epsilon\approx10$. With the geometry of Fig. 1(a), we calculate $C_{\rm g}\approx0.03$ fF, $C_{\rm stray}\approx0.16$ fF, and $C_{\rm self}\approx0.02$ fF. For the seven-junction pump we have used a fused quartz

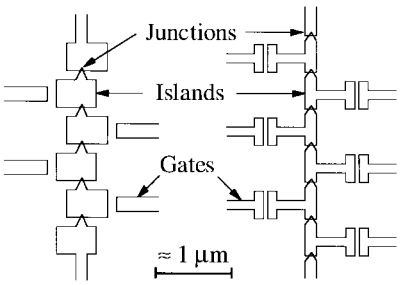

Fig. 1. Geometry of islands and gates for the (a) five-junction pump and the (b) seven-junction pump. The dual image from the two-angle evaporation is not shown for clarity.

substrate with $\epsilon = 3.75$. With the geometry in Fig. 1(b), we calculate $C_{\rm g} \approx 0.02$ fF, $C_{\rm stray} \approx 0.06$ fF, and $C_{\rm self} \approx 0.01$ fF. The reductions in $C_{\rm stray}$ and $C_{\rm self}$ allow us to achieve the same total island capacitance with larger junctions which can be fabricated more reliably and with better uniformity.

C. Cross Capacitance

The small distances between all the islands and gates in Fig. 1 lead to significant cross capacitance which interferes with the operation of the pump. When a voltage is applied to one gate electrode, the island nearest that gate is polarized with a charge, but significant polarization also occurs on neighboring islands. This cross-capacitance effect can be eliminated by electronically adding a fraction of the applied voltage, with opposite polarity, to the neighboring gates. When the fractions are adjusted properly, though gain potentiometers in a special circuit described below, each island can be polarized separately [6]. However, adjusting the gains for exact cancellation is difficult if the cross capacitance is too large. For the five-junction pump [Fig. 1(a)], the capacitance $C_{\rm nn}$ between each gate and the nearest neighbor island was 40% of the direct gate-to-island capacitance $C_{\rm g}$. The cancellation gains had to be carefully optimized for each pump device *in situ*, which was a tedious process requiring about a half hour when done by a practiced operator. For the seven-junction pump [Fig. 1(b)], the geometry has been changed to reduce $C_{\rm nn}$ to 20% of C_g. With this design, finding the optimal cancellation gains is much easier. Furthermore, the gains can be accurately predicted from a two-dimensional calculation of the cross capacitance and very little *in situ* optimization is needed.

III. Pump Fabrication

We fabricate the pump using the standard technique of two-angle evaporation of Al though a mask patterned by electron beam lithography, with an oxidation step after the first layer to form tunnel junctions where the two layers overlap [8]. The angle between the evaporations determines the amount of overlap and thus the area and capacitance of the junctions. For fixed oxide thickness, junction capacitance is inversely proportional to junction resistance, which is easily measured at room temperature. Our approach to making small junctions with a certain value of capacitance is to pattern identical masks on four chips and then evaporate junctions on one chip at a time, using the junction resistance to determine a new angle for the next evaporation until the target value is obtained. We typically achieve the target resistance in one out of each set of four devices and we can complete two sets in one day. Below we describe the fabrication process in more detail.

Large scale leads and bonding pads in 6 mm $\times$ 6 mm patterns are fabricated on a fused quartz wafer using conventional optical lithography and Au metallization. A bilayer electron beam resist, consisting of $\approx$500 nm of the copolymer poly(methylmethacrylate-methacrylic acid) and $\approx$100 nm of poly(methylmethacrylate), is spun onto the wafer. The wafer is then coated with $\approx$10 nm of Au or Al, evaporated from a resistively heated source, to provide a conductive layer. A transparent protective tape is placed on the front side of the wafer before sawing it into individual chips. Four chips at a time are mounted on the stage of a scanning electron microscope with metal screws to provide electrical contact to the front surface of each chip. All four chips are exposed with the same electron dose, stripped of the thin conductive layer, and developed identically. One chip at a time is then placed in an electron beam evaporation chamber on a room temperature stage whose angle to the source can be varied continuously. Before Al is deposited on the chip, $\approx$20 nm of Al is evaporated with the shutter closed and with 1.3 mPa (10 μtorr) of O_2 in the chamber. If this is not done, the junction resistance often increases rapidly upon exposure to air at room temperature, becoming larger than a few megaohms in 1 to 3 days. This phenomenon is not understood, but the use of O_2 during deposition of Al for small tunnel junctions has been reported elsewhere [9]. The bottom and top Al layers are $\approx$30 nm and $\approx$40 nm thick, respectively, and are evaporated at a pressure of 0.1 to 0.3 mPa and a rate of $\approx$0.3 nm/s. Before depositing the top layer, the bottom layer is oxidized in 13 Pa (100 mtorr) of O_2 for 5 min at room temperature. With these oxidation parameters, we find that a resistance per junction of about 500 kΩ corresponds to a junction capacitance of about 0.25 fF. After liftoff in a beaker of acetone, only the edges of the chip are touched with tweezers to avoid damage to the junctions from electrostatic discharge. Since the device is on an insulating substrate, touching a bonding pad often destroys the junctions even if the tweezers are connected to a grounded metal plate below the chip. The resistance of the seven junctions in series is measured using a handheld multimeter with 1 MΩ in series with each lead. Completed devices are stored in a sealed box which is purged with dry N_2.

We use a scanning force microscope to obtain images of completed devices without any apparent damage to the tunnel junctions. This allows us to avoid the time and expense of cooling down devices with fatal submicrometer flaws that cannot be detected with an optical microscope.

IV. Pump Operation

Each device to be measured is mounted on a header consisting of Au-plated pins epoxied into holes in a Cu base. The chip is attached to the header with grease and Al wire bonds connect the pins to pads on the chip. The header plugs

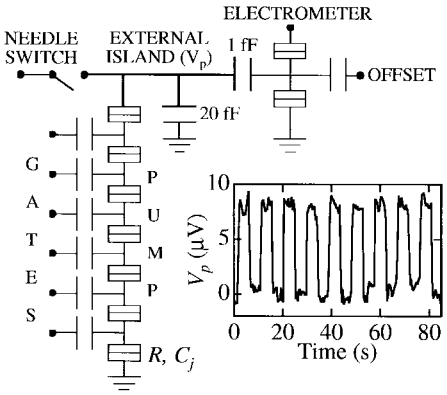

Fig. 2. Schematic of the circuit used to study the pump. All components except the needle switch are fabricated on a single chip. The plot shows V_p versus time when pumping $\pm e$ with a wait time of 4.5 s between electrons.

into Au-plated sockets soldered into a printed circuit board. This system allows us to measure pump devices many times over long periods and to easily transfer devices between NIST laboratories in Boulder, CO, and in Gaithersburg, MD. The printed circuit board is mounted in a Cu box attached to the mixing chamber of a dilution refrigerator. The base of the header is clamped to the Cu box to provide thermal contact. All electrical leads entering the box are coaxial. The gate leads are strongly attenuated and the other leads have filters for radio and microwave frequencies [10]. A permanent magnet beneath the header forces the Al of the pump out of the superconducting state.

The circuit used to study the electron pump is shown in Fig. 2. We give a brief description here; further details can be found in [7]. The pump is connected to an external island, shown with heavier lines, whose voltage V_p is monitored by an electrometer [2] (also based on small tunnel junctions). A cryogenic switch, consisting of a needle on a magnetically controlled lever, contacts a metallic pad that is part of the external island. We close the switch to measure the current-voltage curve of the pump and the gain of the electrometer. We open the switch to detect intentionally pumped electrons or errors. The plot in Fig. 2 shows V_p versus time for the $\pm e$ pumping mode in which one electron is repeatedly pumped on and off the external island. Each step of 7.6 μV corresponds to a change in the island charge of e.

To operate the electron pump, we use custom electronics to perform four functions, as illustrated in Fig. 3. The pulse generator has a digital logic section which allows us to set various parameters such as the number of electrons pumped, the direction of pumping, and the wait time between pumped electrons. The digital section controls a high speed analog section which generates triangular voltage pulses on six output channels by charging and discharging capacitors. A dc bias for each line can be adjusted to compensate for background charges on the islands of the pump, as described below. The pulses and dc biases are summed channel-by-channel to produce a set of voltages $\{V_{\rm g}\}$ on the gate lines. The cross capacitance cancellation circuit performs a 6×6 matrix transformation to create a set of voltages $\{V'_{\rm g}\}$. When the cross capacitance gains are properly adjusted (see below), a voltage

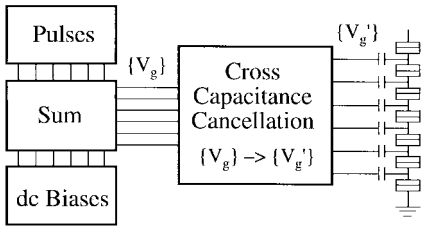

Fig. 3. Schematic operational circuit for the pump. Both the sum and cross capacitance cancellation circuits have bandwidth $\geq$50 MHz.

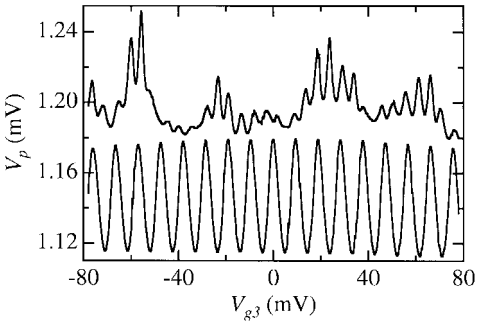

Fig. 4. V_p versus V_{g3} at constant current bias showing cancelling of the cross capacitance. Top trace is with no cancellation, i.e., $\{V_{\rm g}\} = \{V'_{\rm g}\}$. Bottom trace (offset vertically) is after tuning the cancellation gains to the optimal values.

V_{gi} applied to channel i is transformed into the appropriate set of voltages $\{V'_{\rm g}\}$ that polarizes only island i.

A. Cross Capacitance Cancellation

The voltage V_p across the pump at constant bias current is fundamentally periodic in the charge on any island with period e. If each V_{gi} polarizes only island i, then V_p is a periodic function of any V_{gi}. The top trace of Fig. 4 shows that when V_{g3} is swept without the cross capacitance cancellation ($\{V_{\rm g}\} = \{V'_{\rm g}\}$), V_p is not periodic, implying that V_{g3} polarizes more than one island. After the 36 gain potentiometers of the cross capacitance cancellation circuit are systematically adjusted [11], V_p versus any V_{gi} is periodic, as seen in the bottom trace of Fig. 4 for V_{g3}. This result clearly shows that we have cancelled the polarization on neighboring islands, as is necessary for accurate electron pumping. Starting from random values of the 36 potentiometers, the adjustment requires two or three iterations to converge. However, our capacitance calculation program predicts gain values that are very close to optimal, thus only a brief fine-tuning is needed after setting the gains to the predicted values. Since the cross capacitance depends only on the geometry of islands and gates, the adjustment of the gains is needed only the first time each device is operated.

B. Background Charge Compensation

Background charges in the junction oxide or the substrate produce random island polarization charges of order e which fluctuate slowly over time at low temperature. To compensate these charges, dc biases on the gates are tuned so that the charge on each island in the absence of a gate pulse is much

smaller than e. We adjust the dc biases for minimum pumping errors as follows. We operate the pump in the $\pm e$ mode (as in the plot in Fig. 2) at a rate much faster than the electrometer can respond (typically 5 MHz) so that the electrometer signal is constant as long as there are no errors. An error causes a sudden jump in the signal, corresponding to a change of e in the average external island charge, which can easily be seen when the electrometer signal is displayed on an oscilloscope. We then increase the bias on a given gate until the error rate increases noticeably, decrease the bias until the error rate increases again, and use the average bias as the optimal setting for that gate. The difference between the two settings where errors increase is typically $0.5e$ and the repeatability of the optimal settings is about $\pm 0.05e$. The adjustment of all six gate lines takes about 10 min, so it can be quickly repeated whenever changes in the background charges affect the pump accuracy. We find that the time between required adjustments varies from less than one hour to tens of hours. The background charges appear to be more stable after a few weeks at a refrigerator temperature of 35 mK to 200 mK than shortly after cooldown.

V. Conclusion

The seven-junction pump is a relatively easy-to-operate cryoelectronic device that transforms electron counting from a novel laboratory phenomenon into a reliable process suitable for metrology. As our recent study of pump accuracy has shown [7], the pump is close to the level of performance which would make a capacitance standard based on charging a capacitor competitive with existing standards. We believe a better fundamental understanding of the error processes will allow us to improve accuracy even further. Our future research will involve a prototype capacitance standard and working to make all components of the standard operate with an imprecision near 10^{-8}. Progress on individual components and analysis of some of the remaining challenges are reported elsewhere [4], [5], [12].

Acknowledgment

The authors thank R. L. Kautz for helpful comments on the manuscript.

References

[1] H. Pothier, P. Lafarge, C. Urbina, D. Esteve, and M. H. Devoret, "Single-electron pump based on charging effects," *Europhys. Lett.*, vol. 17, pp. 249–254, 1992.

[2] For a review of Coulomb blockade effects and devices, see *Single Charge Tunneling*, H. Grabert and M. H. Devoret, Eds. New York: Plenum, 1992.

[3] E. R. Williams, R. N. Ghosh, and J. M. Martinis, "Measuring the electron's charge and the fine-structure constant by counting electrons on a capacitor," *J. Res. Natl. Inst. Stand. Tech.*, vol. 97, pp. 299–304, Mar.–Apr. 1992.

[4] A. F. Clark, N. M. Zimmerman, E. R. Williams, A. Amar, D. Song, F. C. Wellstood, C. J. Lobb, and R. J. Soulen, "Application of single electron tunneling: Precision capacitance ratio measurements," *Appl. Phys. Lett.*, vol. 66, pp. 2588–2590, 1995.

[5] N. M. Zimmerman, "Capacitors with very low loss: Cryogenic vacuum-gap capacitors," *IEEE Trans. Instrum. Meas.*, vol. 45, pp. 841–846, 1996.

[6] J. M. Martinis, M. Nahum, and H. D. Jensen, "Metrological accuracy of the electron pump," *Phys. Rev. Lett.*, vol. 72, pp. 904–907, 1994.

[7] M. W. Keller, J. M. Martinis, N. M. Zimmerman, and A. H. Steinbach, "Accuracy of electron counting using a 7-junction electron pump," *Appl. Phys. Lett.*, vol. 69, pp. 1804–1806, 1996.

[8] G. J. Dolan, "Offset masks for lift-off photoprocessing," *Appl. Phys. Lett.*, vol. 31, pp. 337–339, 1977.

[9] L. Ji, P. D. Dresselhaus, S. Han, K. Lin, W. Zheng, and J. E. Lukens, "Fabrication and characterization of single-electron transistors and traps," *J. Vac. Sci. Technol. B*, vol. 12, pp. 3619–3622, Nov.–Dec. 1994.

[10] J. M. Martinis, M. H. Devoret, and J. Clarke, "Experimental tests for the quantum behavior of a macroscopic degree of freedom: The phase difference across a Josephson junction," *Phys. Rev. B*, vol. 35, pp. 4682–4698, 1987.

[11] We have developed an algorithm for adjustment of the gains that is straightforward to execute but difficult to explain briefly. The algorithm and the circuit used to implement it can be obtained by contacting the authors.

[12] N. M. Zimmerman, J. L. Cobb, and A. F. Clark, "Recent results and future challenges for the NIST charged-capacitor experiment," *IEEE Trans. Instrum. Meas.*, vol. 46, Apr. 1996.

Mark W. Keller reveived the B.S. degree in physics from Pacific Lutheran University, Tacoma, WA, in 1988, and the Ph.D. degree in applied physics from Yale University, New Haven, CT, in 1995.

He was a National Research Council Postdoctoral Associate, Cryoelectronic Metrology Group, National Institute of Standards and Technology (NIST), Boulder, CO, from 1995 to 1996 and is currently a Research Physicist with that group. His research involves fundamental processes in single-electron tunneling devices and metrological applications of these devices such as a new capacitance standard.

John M. Martinis received the B.S. degree in physics and the Ph.D. degree in physics from the University of California, Berkeley, in 1980 and 1987, respectively.

Upon completing a postdoctoral position at the Commisiariat Energie Atomic, Saclay, France, he joined the Cryoelectronic Metrology Group, National Institute of Standards and Technology (NIST), Boulder, CO. He has been involved in understanding the basic physics of the Coulomb blockade, and is working to use this phenomena to make a new fundamental electrical standard based on counting electrons.

Andrew H. Steinbach was born on January 21, 1965. He received the B.A. degree in physics from Bates College, Lewiston, ME, in 1987. He is currently pursuing the Ph.D. degree in physics at the University of Colorado, Boulder, where he conducts dissertation research at the National Institute of Standard and Technology (NIST), Boulder, CO.

His thesis work involves mesoscopic physics, single-electron tunneling devices, and applications of dc SQUID's.

Neil M. Zimmerman, for a photograph and biography, see this issue, p. 298.