EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN-EP/87-81
April 16th, 1987

A Si STRIP DETECTOR WITH INTEGRATED COUPLING CAPACITORS

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ABSTRACT

A silicon microstrip detector with capacitive coupling of the diode strips to the metallization and with individual polysilicon resistors to each diode has been developed. The detector was tested in a minimum ionizing particle beam showing a performance similar to conventional strip detectors and a spatial resolution of 3.5 μm. Capacitive coupling allows the decoupling of the leakage current from the input to the charge sensitive preamplifier especially in the case of LSI electronics.

To be submitted to Nuclear Instruments and Methods

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1. INTRODUCTION

Si microstrip detectors are by now in regular use in high energy physics experiments at CERN and Fermilab [e.g. 1,2], where very good spatial resolution in the order of σ = 5 μm is required. So far systems using hybridised or component readout electronics have been built with up to roughly 10,000 channels. To go beyond this limit one has to apply LSI readout electronics with multiplexing in order to match the high density and very large number of strips. This is especially the case for the geometry of collider experiments, where one can only afford a very small amount of non-sensitive detector material forbidding bulky assemblies of cables and electronic components near the interaction region.

Using conventional detectors together with LSI readout chips [3] brings with it the inconvenience that the leakage current of each strip is fed into the preamplifier. It is not possible to couple capacitively to the preamplifier as in the case of conventional electronics because one needs several tens of picofarad for the coupling capacitance in order to avoid capacitive signal losses to the back plane. Leakage currents of individual strips often vary by a factor of up to 1000 across one detector. This does not in general affect the spatial resolution as long as leakage currents for single strips stay below about 200 nA/strip. With chip readout this phenomenon introduces however considerable base line differences between channels of one chip and requires an otherwise unnecessarily large dynamic range of the ADCs.

We have therefore designed and built a microstrip detector with capacitive coupling between diodes and metallization for later use in a microvertex detector in a LEP experiment [4]. The design, fabrication, electrical performance of such a detector and first results from a beam test performed with a prototype detector are described.

2. DETECTOR DESIGN

The microstrip detector consists of 512 diode strips with 25 μm pitch (15 μm spacing and 10 μm linewidth). Each diode is connected to a bias line by an individual polysilicon biasing resistor. The coupling of the metal to the diode is capacitive via a very thin oxide layer.

Each strip consists of three regions. An active detector part which is 10 μm wide and 23 mm long. A connecting line, 15 μm wide and with varying length according to the strip position. The connecting line ends in a bonding pad of 80 x 200 μm^2. The pads are made large to facilitate automatic bonding. This also enlarges the area of the coupling capacitor. At each end of the active detector area

is the connection zone with high resistivity polysilicon biasing resistors, connected to a metal strip providing the bias for diodes, the so-called bias strip. The polysilicon resistors are designed such that all strips have equal resistivity. The total detector size is 18 mm by 30 mm. A schematic layout of the strips, connecting lines, bonding pads, polysilicon and bias strips is shown in Fig. 1.

The mask set consists of 4 layers. The first mask defines the diffused pn-junction strip pattern. The pn-junction extends over the active area and also over the connecting line and pad. This design gives lower stray capacitance than using metal running over oxide. The disadvantage is the increased detector area which gives rise to increased leakage current and the possibility of getting signals from particles traversing this area. The second mask opens contact holes in the passivation oxide to give contact between the polysilicon resistors and the diffused pn-junction. The third mask defines the polysilicon resistors which run from the contact hole to a common metal line. Four strips are grouped together and have a common resistor in series which are specially matched. In this way every bias resistor will have an equal number of squares and the same resistance. The resistivity of the polysilicon was chosen so that the resistor value should be approximately 3 MΩ.

The last mask defines the metal pattern. 8 μm wide metal lines run over the active area pn-junction and connecting line. The metal is terminated in large pads. The area of metal defines the coupling capacitor. The capacitor value can be tailored by varying the oxide thickness. The value of the coupling capacitance has to be large compared with the feedback capacitance of the charge sensitive amplifier in order not to deteriorate the signal to noise ratio at the output of the amplifier (see Appendix). The coupling capacitance has also to be sufficiently larger than the interstrip capacitance to avoid the signal spreading over too many strips. We chose 100 nm and 200 nm oxide thickness giving a capacity of 70 pF and 35 pF, respectively. The thin oxide is estimated to withstand a voltage of 60 to 90 V. The contact holes connecting the diodes to the polysilicon strips also have a metallized pad to make direct probing possible. A guard-ring is situated around the entire active area.

In this first design there is no mask for contact holes between metal and polysilicon. This feature does not allow the polysilicon to be passivated with oxide. In the long run this can affect the stability of the polysilicon resistors. Temperature measurements on similarily processed polysilicon resistors indicate good temperature stability and long term stability.

3. PROCESS CONSIDERATIONS

Microstrip particle detectors usually have a high circumference to area ratio. This will make the surface contribution to the leakage current high. In earlier designs of the same detector [5], but without the capacitive diode strip coupling and polysilicon resistors, values of leakage current of 120 pF/strip at 120 volts reverse bias voltage have been achieved. These numbers were obtained by careful control of oxide charges and special gettering techniques. Deposition of polysilicon includes new processing steps and will affect the leakage current and breakdown voltage.

The process aims at controlling the oxide charge and electrical parameters. HCl oxidation is reported to give good electrical quality of the oxide and reduce the number of oxidation induced stacking faults. It also reduces the number of mobile charges in the oxide and the number of interface traps and increases surface lifetime (velocity). It influences the stability of the device, the leakage current and the breakdown voltage.

Detector grade silicon wafers from Wacker were used as substrates. The 2 inch, ⟨111⟩ oriented wafers were n-type phosphorous doped with a resistivity between 1500 and 3000 Ωcm and a thickness of 280 microns.

Before processing all 24 wafers were marked (MII-1 to 24) on the back for identification purposes and rinsed using standard RCANH_3 and HCl processes. A 1 µm thick oxide was grown using a combination of dry oxidations and wet oxidations at a temperature of 1100°C. All of the dry oxidations were performed using a 0.5% addition of HCl. The HCl was supplied by passing N_2 through 1.1.1 trichloroethane. Wet oxidation was performed by burning H_2 and O_2 in a quartz chamber outside the furnace. After the oxidation the front was covered with positive photoresist and the thick oxide on the back was etched using buffered hydrofluoric acid.

Before phosphorous deposition on the back photoresist was stripped in aceton and plasma and both NH_3 and HCl rinsing was performed. The phosphorous deposition gave a sheet resistivity of approximately 5 Ω/□. The high dose on the back was used to ensure good ohmic contact and to prevent the depletion zone to reach the back surface.

After deposition the phosphorous glass was stripped in 5% hydrofluoric acid. The wafers were cleaned in a HCl rinse and diffusion was performed at 1000°C. The active detector area was defined in a photolithographic step while the back was masked during etching in buffered hydrofluoric acid.

After stripping of resist and a standard RCA-rinse, the pn-junctions were made by deposition of boron from the gas phase. Deposition was performed at 930°C and 1050°C to give 45 Ω/□ and 10 Ω/□ sheet resistance respectively. The deposited boron was subsequently diffused at 930°C resulting in a high sheet resistance of 75 Ω/□ and a low value of 15 Ω/□.

To tailor the passivation oxide to specified thicknesses two different diffusion and oxidation steps were used. Both oxidations were performed at 930°C but with different times of wet oxidation. Finally 6 wafers were each processed with the four combinations of oxide thickness and sheet resistance (Table 1).

After diffusion and oxidation contact holes for the biasing resistors were opened in the passivation oxide using photolithography. Resist stripping and HCl rinsing were performed before deposition of polycrystalline silicon. The polysilicon was deposited at 790°C using a standard LPCVD process. The 500 nm polysilicon was implanted with boron at an energy of 60 keV and to a dose of $1 \cdot 10^{14}$ At/cm^2. The implantation was annealed in N_2 at 900°C for 30 minutes. The sheet resistance of the polysilicon is approximately 48.5 kΩ/□, giving a resistor value of about 3.2 MΩ. A photolithographic step defined the polysilicon pattern which was etched in a barrel reactor using CF_4 with 17% O_2. The resist was stripped in the same reactor and the wafers were thoroughly cleaned before metallization. Approximately 1 µm of pure aluminium was deposited using E-gun evaporation. The metal was patterned in a photolithographic step. Resist was stripped in aceton and plasma and finally the wafers were sintered in forming gas at 450°C for 15 minutes.

A high degree of cleanliness was kept throughout all the processing and at the same time HCl oxidations were used to give a good oxide quality. Nitrogen annealing was used after oxidation to reduce the oxide charge. The process includes various gettering steps in order to achieve low leakage current.

4. RESULTS FROM MEASUREMENTS

Four detectors, one of each type (Table 1) with capacitive coupling between diode and metallization (from now on called detectors A) and one of conventional design (from now on called detector B), 256 strips, 128 on each side, have been connected by wire bonding to an aluminium fanout. These assemblies were then mounted onto aluminium precision frames for use in a test beam. The thicknesses of detectors A and B were measured to be 260±10 µm and 268±10 µm respectively.

4.1 Electrical Properties

4.1.1 Leakage current

The leakage current behaviour as a function of bias voltage and at a given bias voltage as a function of time has been studied for 15 different detectors cut from wafers indicated in Table 1. The dependence of leakage current on bias voltage for detector 17F is shown in Fig. 2. The leakage currents i_1 and i_2 are measured on both bias strips simultaneously, thus giving the sum of the current on 256 strips each. The approximate square root behaviour indicates that its origin is a bulk generation current. The average leakage current per strip derived from this curve is very low, I = 90 pA at V_B = 100 V. All other detectors which have been measured exhibit considerable variations (up to factor of 10) of the leakage current with time at a fixed bias voltage (V_B = 120 V), but most of them finally settle to stable current levels well below values required for min. I. particle detection. Two of the detectors have a leakage current of more than 10 µA for all 512 strips together. Further investigations on leakage current variations with time at fixed bias voltage on these detectors are continuing at present.

4.1.2 Capacitance

The capacitance of 48 metal strips versus the backplane has been measured as a function of bias voltage for all 4 types of detector A and for detector B. For this measurement we use a bridge with measuring frequency 10.6 kHz and an rms amplitude of 200 mV. Figure 3 shows a globally linear dependence from about V_B = 1 V to V_B = 100 V on log-log scale as expected when the depletion develops through the detector. From V_B = 100 V to V_B= 160 V the capacitance is constant showing that depletion is reached at 100 volts. At very low bias voltage the capacitance of all measured detectors flattens to values of ~ 9-16 pF/strip. Except for detector A MII-16R there is no significant difference between detectors A and detector B, indicating that the diode-metallization capacitance is bigger than 15 pF. The capacitance of a single strip w.r.t. all its neighbours and the backplane measured as a function of bias voltage is shown in Fig. 4 for both types of detectors. It varies only slowly above V_B = 1 V and reaches a plateau above ~ 20 V, since full sideways depletion is already reached at low V_B. The single strip capacitance with respect to its neighbours and with respect to the backplane, measured at V_B = 40 V for the 5 detectors is listed in Table 2. The 2 detectors with the higher diode sheet resistance have smaller interstrip capacitance.

4.2 First Results from Beam Tests

Detectors A (MII-16R) and B (MI-28F) have been installed in a test beam of high energy electrons and pions (E = 20-200 GeV/c) in the North Hall of the SPS at CERN. A Si telescope providing a measurement of space tracks with very high spatial resolution (part of the NA32 experiment [1]) was already set up in this beam allowing precision impact determination of each particle at the position of the detector under study (Fig. 5). We present first results from this beam test on the response of these two detectors to minimum ionizing particles.

The readout electronics used in this test are the standard NA32 electronics; a hybrid charge sensitive preamplifier, a shaper amplifier and a line receiver - and are described in some detail in ref. [6]. The pulseheights from 96 adjacent strips of each test detector were digitized by 12 bit ADCs (LeCroy 2281). The average electronics noise of one channel for this set-up is ENC $\simeq$ 900 e^-. Several hundred thousand beam tracks have been recorded.

4.2.1 dE/dx distribution

In the offline analysis events are selected with a good track reconstructed in the Si vertex telescope. Then a search for a signal in a region around the predicted impact of the particle is performed, demanding that one strip has a pulseheight larger than $4 \times \sigma_{noise}$. A signal cluster is defined as the number of adjacent strips which exceed $4 \times \sigma_{noise}$ with one strip added on each side. The average cluster size defined in this way is $\langle n \rangle = 3.5$. The resulting cluster pulseheight distribution (in ADC counts) for detectors A and B is shown in Fig. 6, a and b respectively. The most probable energy loss corresponds to $21.5 \times \sigma_{noise}$ (noise of 1 channel) for detector A and $22.5 \times \sigma_{noise}$ for detector B. The widths of these distributions are 45% and 42% of the most probable pulseheight for detectors A and B respectively. Landau's theory gives for these ratios 26 percent. It is well known that this is in disagreement with experiment and the theory has been corrected [7,8] by smearing the Landau distribution with a Gaussian corresponding to a correction for the binding energies of electrons in Si atoms. In addition the noise of the electronics has to be added. These corrections increase the ratio to about 39 percent for the electronics used in the beam test. Moreover in order to reproduce our wider distributions we had to increase in Landau's formula the measured thickness of the detectors, but without changing the positions of the maxima. This correction was 12% for detector B and 25% for detector A. The resulting phenomenological curves are shown in Fig. 6. Work on the interpretation of this additional correction which we found necessary is in progress. In Fig. 7 the mean pulseheights of the strip with maximum pulseheight and its left

and right neighbours are shown. Detector A collects somewhat less charge than detector B as expected due to the limited coupling capacitance. The observed charge distribution extends over more strips on the detector A compared with detector B. This is also reflected in the measured cluster multiplicity distribution, obtained for clusters defined as above but side strips were accepted only if they had pulseheight bigger than 1 σ. These distributions are presented in Figs. 8a and b.

4.1.2 Spatial resolution

The spatial resolution was determined from residue distribution of the coordinates measured in the test detectors with respect to the precisely measured tracks. Figures 9a and b show these residue distributions for detectors A and B respectively. Subtracting out the error in the track projection we find σ = 3.5 μm and σ = 3.2 μm for detectors A and B. We have also determined the resolution for the case when particles traverse the detector with an angle of 5° off the vertical incidence. In this case we find σ = 3.2 μm for detector A. The coordinate determination uses linear interpolation between pulseheights on the individual strips in a cluster. We expect to reach a better precision using a non-linear method for coordinate assignment [9,10].

For part of the detector A only every second strip was connected to the readout electronics. This can be done without disturbing the field distribution for this type of detector since the bias voltage is fed independently through the polysilicon resistors to each diode. In this region the spatial resolution was measured to be 5.5 μm.

5. CONCLUSION

A new type of silicon microstrip detector has been developed with capacitive coupling of the diode strips to the metallization. The bias voltage to the diodes is provided through polysilicon resistors connecting separately each diode to a common bias bus-line. This concept has a number of advantages in the application of these detectors in large systems. In particular it allows to decouple the leakage current from the input to the charge sensitive preamplifier also in the case of LSI electronics, which do not allow big enough coupling capacitances on the chip itself due to space limitations. It also enables to run these detectors in capacitive charge division readout mode at any given ratio between readout and floating strips. A test of one such detector in a beam of minimum ionizing particles has demonstrated that these detectors have similar performance as conventionally implanted strip detectors [10] and have very good spatial resolution σ = 3.5 μm.

Acknowledgements

We would like to thank Mrs. F. Buschman from the Center for Industrial Research for processing of the detectors. We thank M. Bosman, F. Wickens and D. Kelsey from the NA32 collaboration for their help in the data taking during the test run and for discussions concerning NA32 analysis programs. We also thank G. Anzivino for her work in the early stage of the development.

REFERENCES

[1] R. Bailey et al., Z. Phys. C. Particles and Fields 28 (1985) 357.

[2] J.C. Anjos et al., Phys. Rev. Lett. 58 (1987) 311.

[3] G. Anzivino et al., "First Results from a Silicon Microstrip Detector with VLSI Readout", NIM A243 (1986) 153.

[4] DELPHI Microvertex Detector, Addendum to Technical Proposal, DELPHI 86-86 GEN-52, CERN, 6 October 1986.

[5] L. Evensen et al., "A New Silicon Microstrip Particle-Detector with Low Leakage Current", paper presented at the 12th Nordic Semiconductor Meeting, June 8-11, 1986, Jevnaker, Norway.

[6] B. Hyams et al., NIM 205 (1983) 99.

[7] P. Shulek et al., Soviet J. Nucl. Phys. 4 (1967) 400.

[8] (a) S. Hancock et al., NIM B1 (1984) 16;
(b) S. Hancock et al., Phys. Rev. A28 Nr. 2 (1983) 615.

[9] E. Belau et al., NIM 214 (1983) 253.

[10] P. Weilhammer, "Experience with Si Detectors in NA32", Invited talk at the Workshop "New Solid-State Devices for High Energy Physics", Berkeley, October 1985.

Table 1

Sheet resistance and oxide thickness for four groups of wafers used for the described detectors.

Wafers	Sheet Resistance	Oxide Thickness
1 - 6	75 Ω/□	100 nm
7 - 12	75 Ω/□	200 nm
13 - 18	15 Ω/□	200 nm
19 - 24	15 Ω/□	100 nm

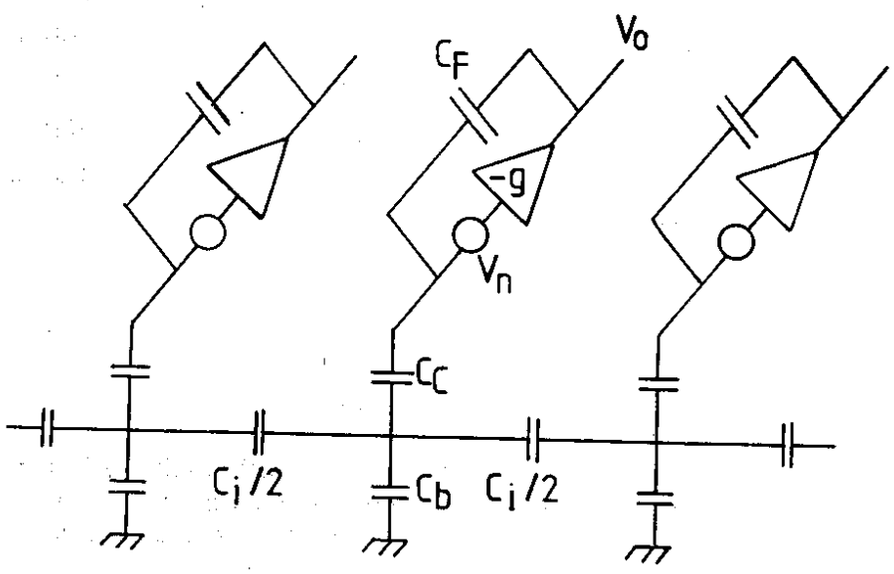
Table 2

Capacitance of 1 strip with respect to all neighbouring strips and with respect to the backplane. Values are given at 40 V for comparison, since detector MII-10R could not be measured at a higher voltage.

Detector Type	Detector #	Interstrip Capacitance	Backplane Capacitance
A	MII- 4R	4.0 pF	0.8 pF
	MII-10R	2.5 pF	1.05 pF
	MII-16R	4.7 pF	0.8 pF
	MII-23R	4.7 pF	0.6 pF
B	MI -28F	3.3 pF	0.7 pF

APPENDIX

For the calculation of the signal and noise output voltages V_{os} and V_{on} the following simplified circuit diagram is used :



C_i is the interstrip capacitance, C_b is the backplane capacitance, C_C is the coupling capacitance, ΔQ is the charge generated in the diode strips, C_F is the feedback capacitance, V_n is the noise voltage referred to the amplifier input, -g is the gain of the inverting amplifier and V_o is the output voltage. C_i and C_b are lumped together as C_P which in our case is smaller than C_C. Assuming infinite impedance of the amplifier, it can be shown that

$$V_{os}/V_{on} = \frac{\Delta Q}{V_n} \cdot \frac{1}{C_P[(C_F/C_C)+1] + C_F}$$

From this the following conclusions can be drawn :

1) It is important to minimize the capacitance C_P since the signal to noise ratio depends almost linearly on $1/C_P$.

2) For large ratios of C_C to C_F the signal to noise ratio becomes virtually independent of the absolute value of C_C.

Figure captions

Fig. 1 Layout of detector.

Fig. 2 Leakage currents measured on 2 bias strips as a function of bias voltage for detector MII-17F.

Fig. 3 Capacitance of 48 strips w.r.t. backplane for 4 detectors of type A (▽, o, □, △) and detector B (•).

Fig. 4 Capacitance of 1 strip versus neighbours and backplane as a function of bias voltage.

Fig. 5 Schematic layout of telescope built up with Si strips detectors used in test experiments.
B1-V8 = silicon microstrip detectors for reconstruction of beam tracks (strip orientations with respect to horizontal plane.
TD = Detector to be tested.

Fig. 6 Cluster pulseheight distribution a) for detector A (MII-16R) and b) detector B (MI-28F) (b). The histogram represents the measurement and the smooth curve is the phenomenological prediction.

Fig. 7 Mean pulseheights of strips in a cluster and its neighbourhood (as in Fig. 6).

Fig. 8 Cluster multiplicity (as in Fig. 6).

Fig. 9 Residue distributions (as in Fig. 6).

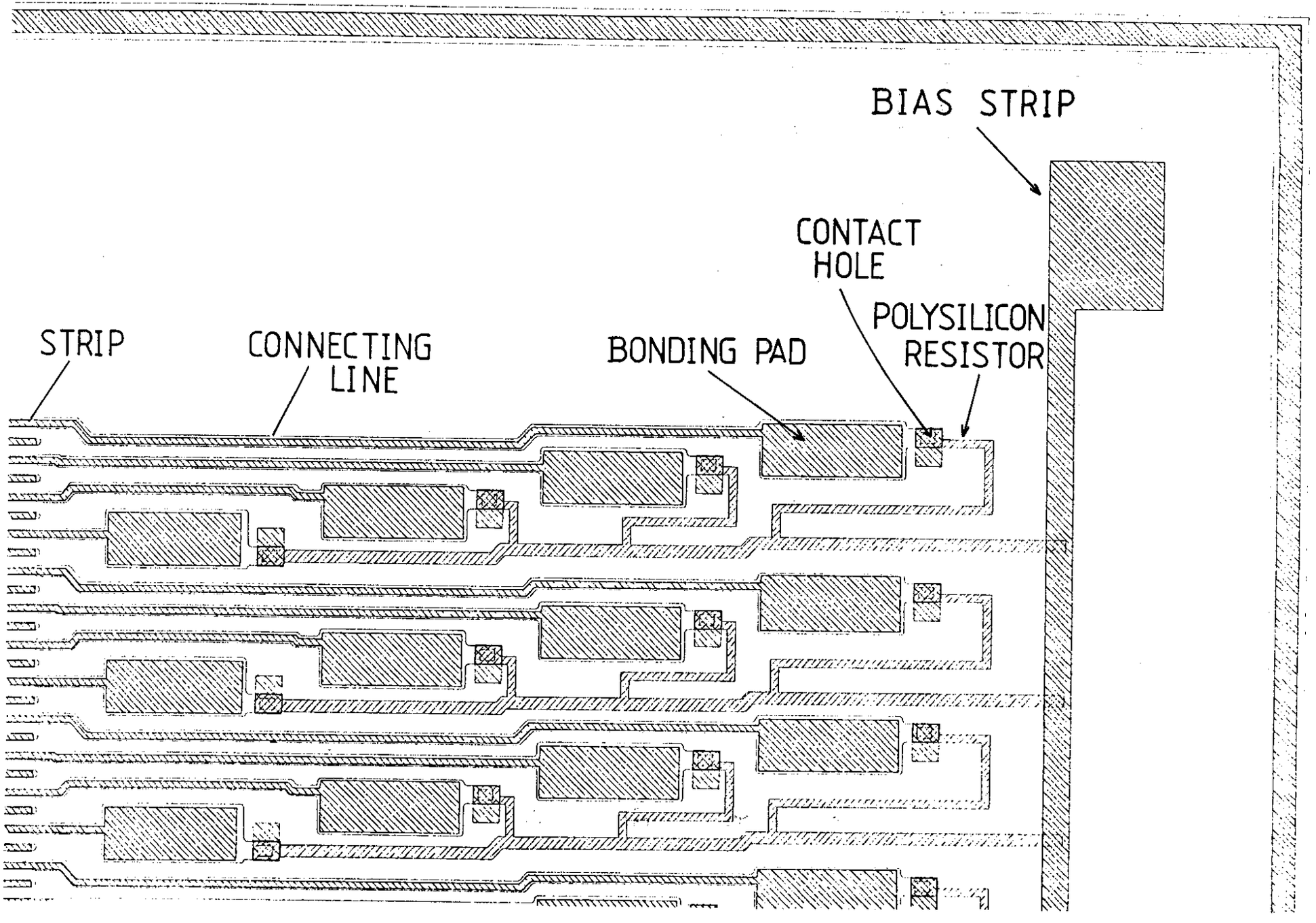

BIAS STRIP
CONTACT HOLE
POLYSILICON RESISTOR
STRIP
CONNECTING LINE
BONDING PAD

Fig. 1

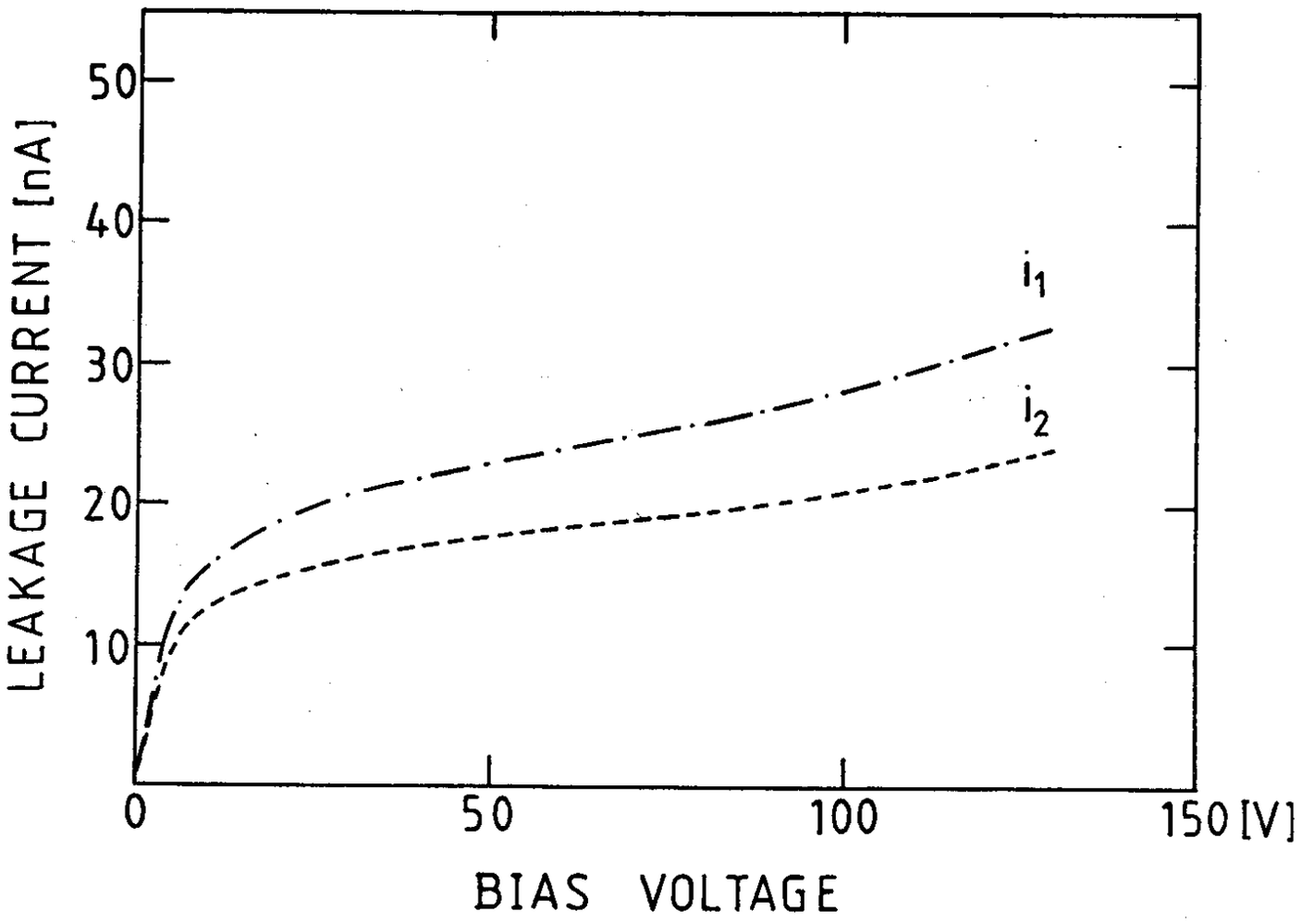

LEAKAGE CURRENT [nA]
50
40
30
20
10
0
50
100
150 [V]
BIAS VOLTAGE
i_1
i_2

Fig. 2

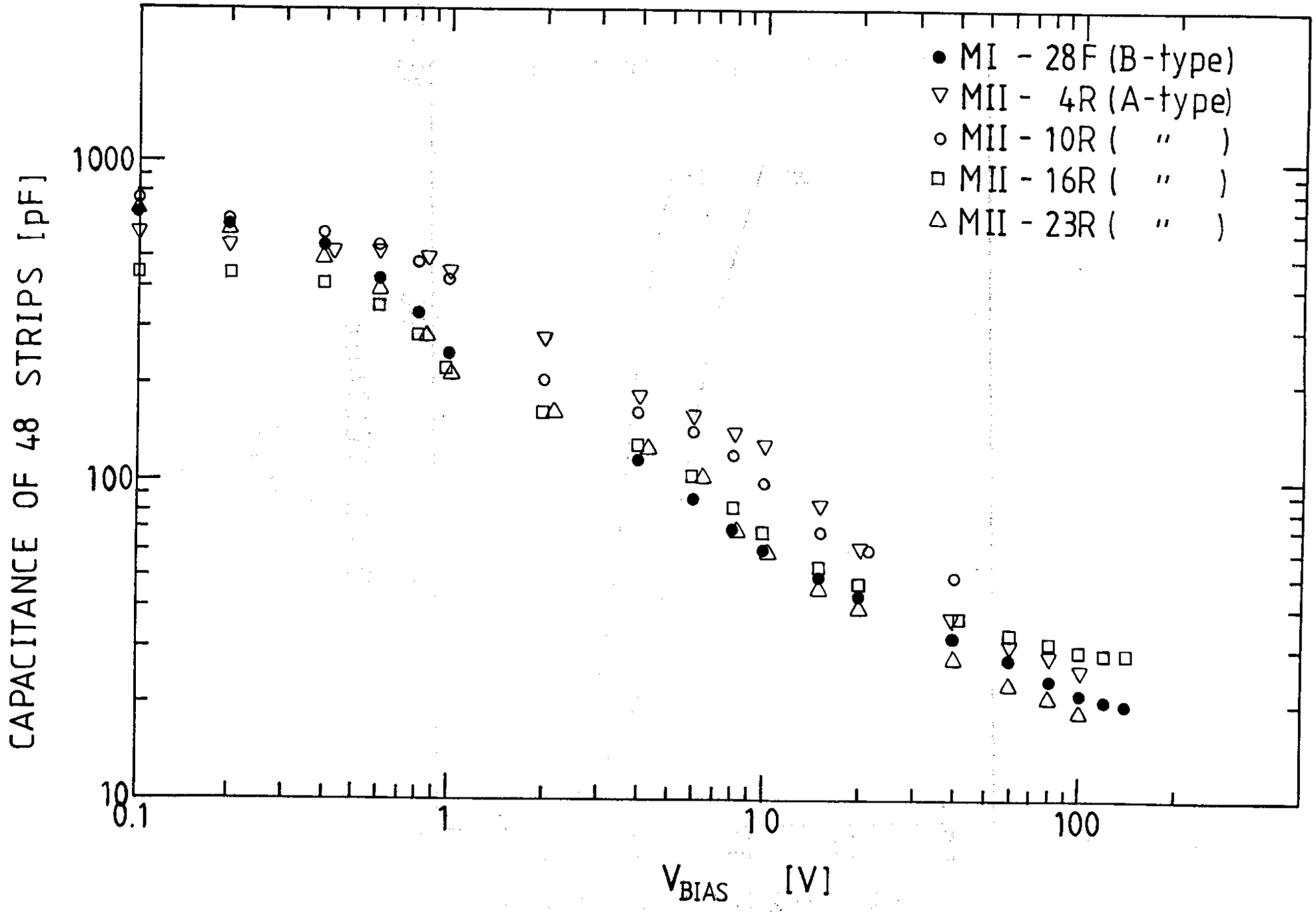

● MI - 28F (B-type)
▽ MII - 4R (A-type)
○ MII - 10R (〃)
□ MII - 16R (〃)
△ MII - 23R (〃)
CAPACITANCE OF 48 STRIPS [pF]
1000
100
10
0.1
1
10
100
V_{BIAS} [V]

Fig. 3

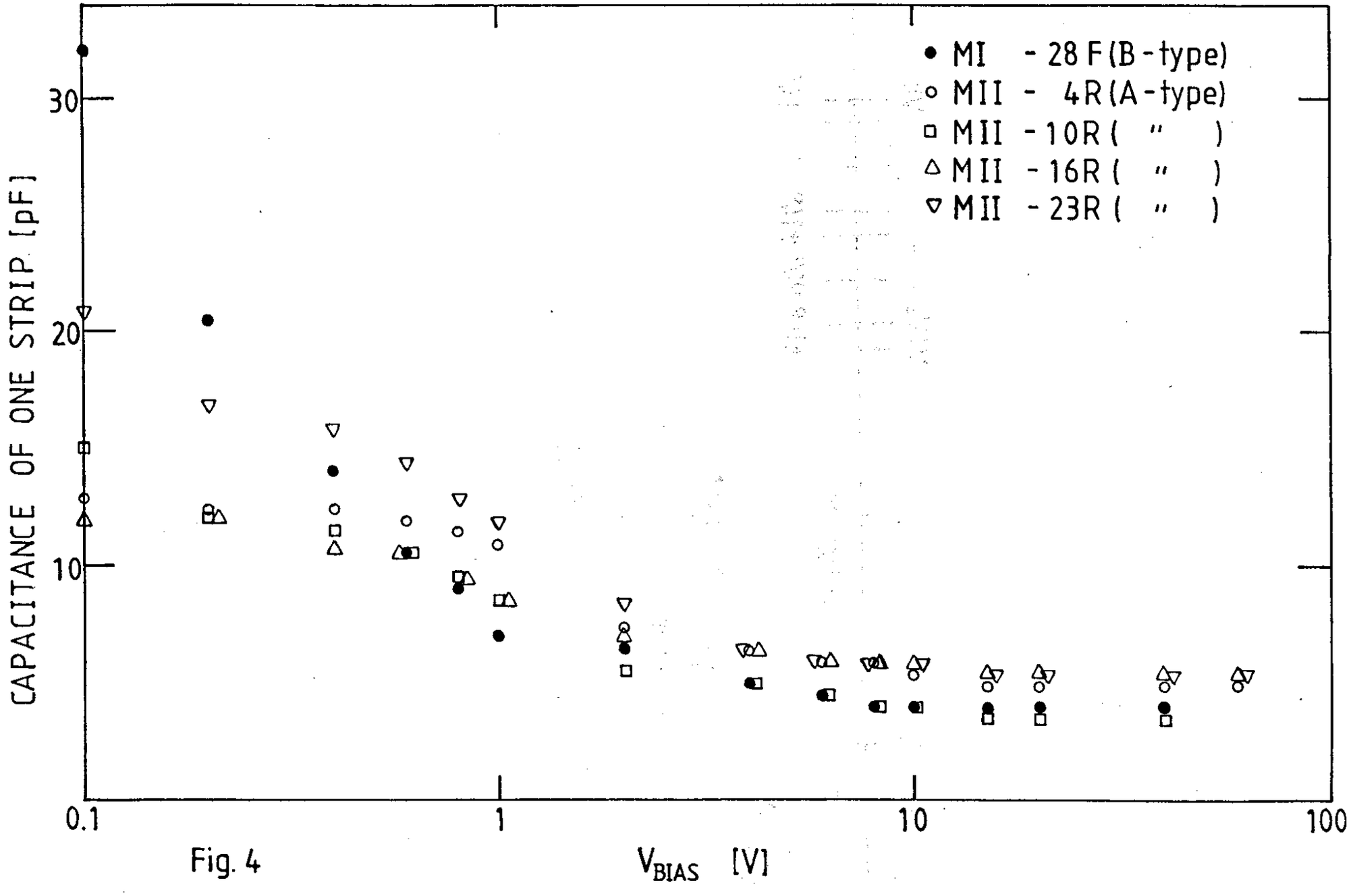

MI - 28 F (B-type)
MII - 4R (A-type)
MII - 10R (")
MII - 16R (")
MII - 23R (")
CAPACITANCE OF ONE STRIP [pF]
30
20
10
0.1
1
10
100
V_{BIAS} [V]

Fig. 4

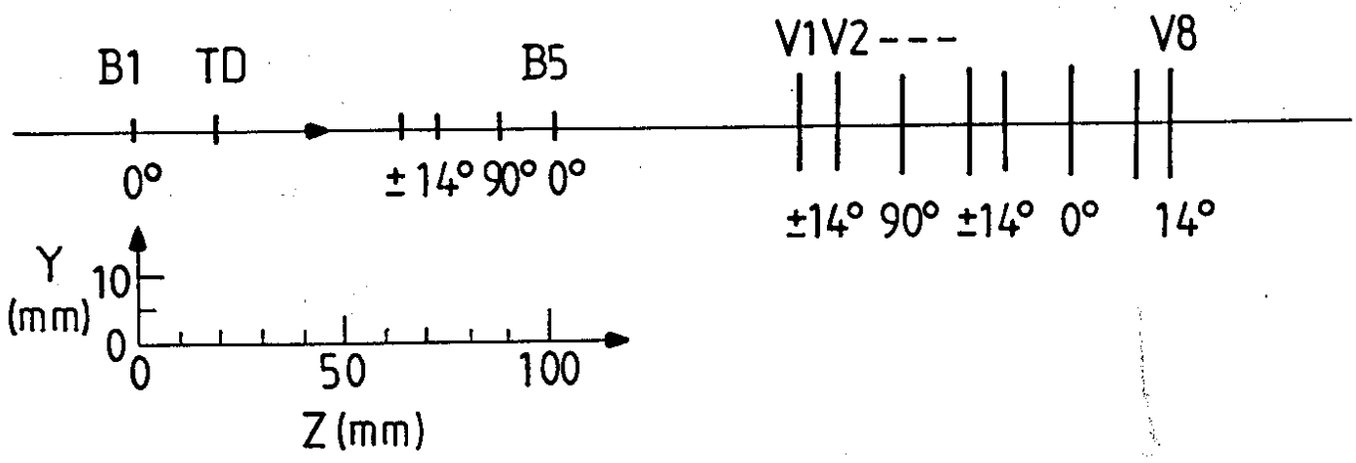


Fig. 5

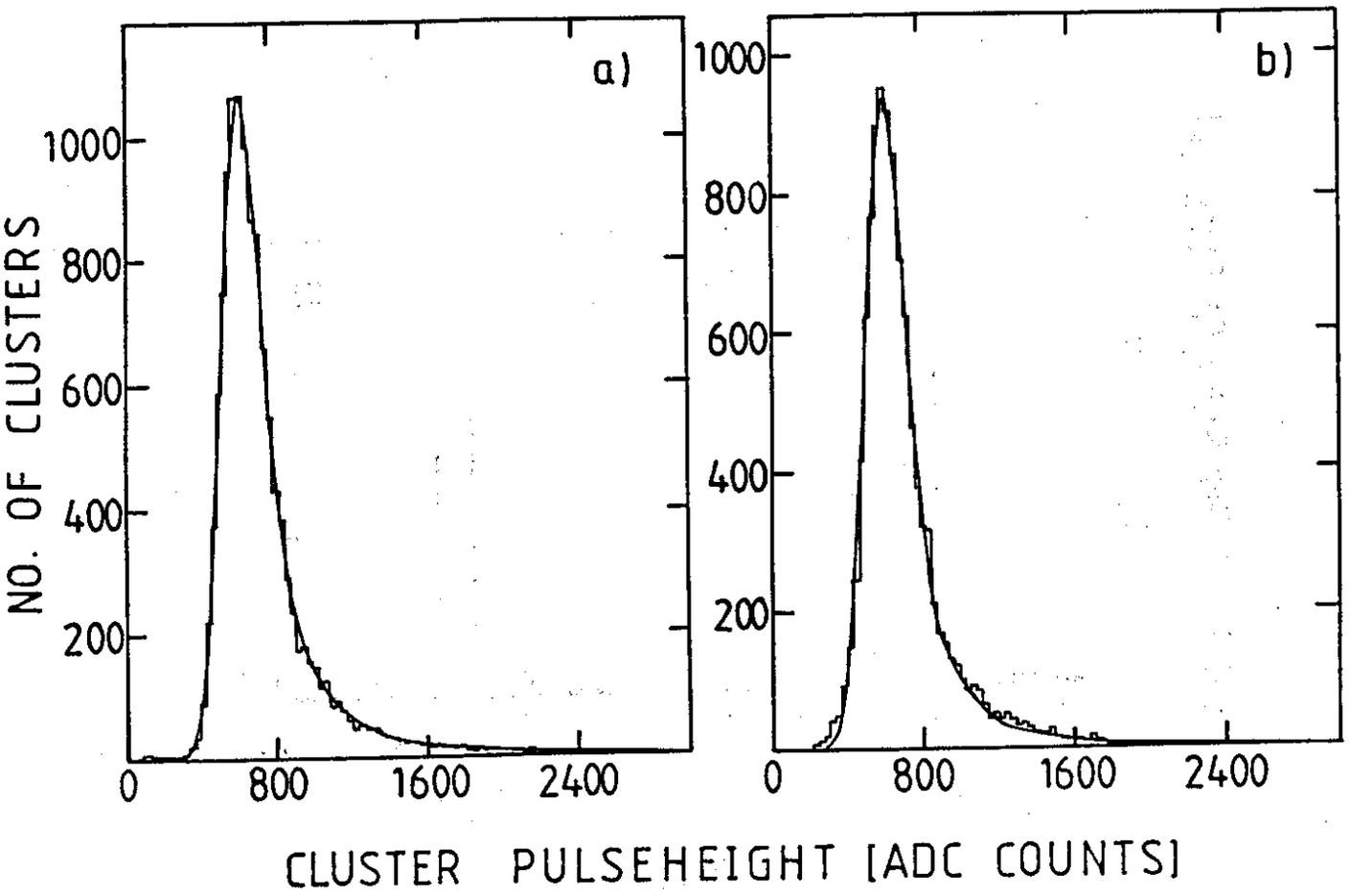

a)
b)
NO. OF CLUSTERS
1000
800
600
400
200
0
800
1600
2400
CLUSTER PULSEHEIGHT [ADC COUNTS]

Fig. 6

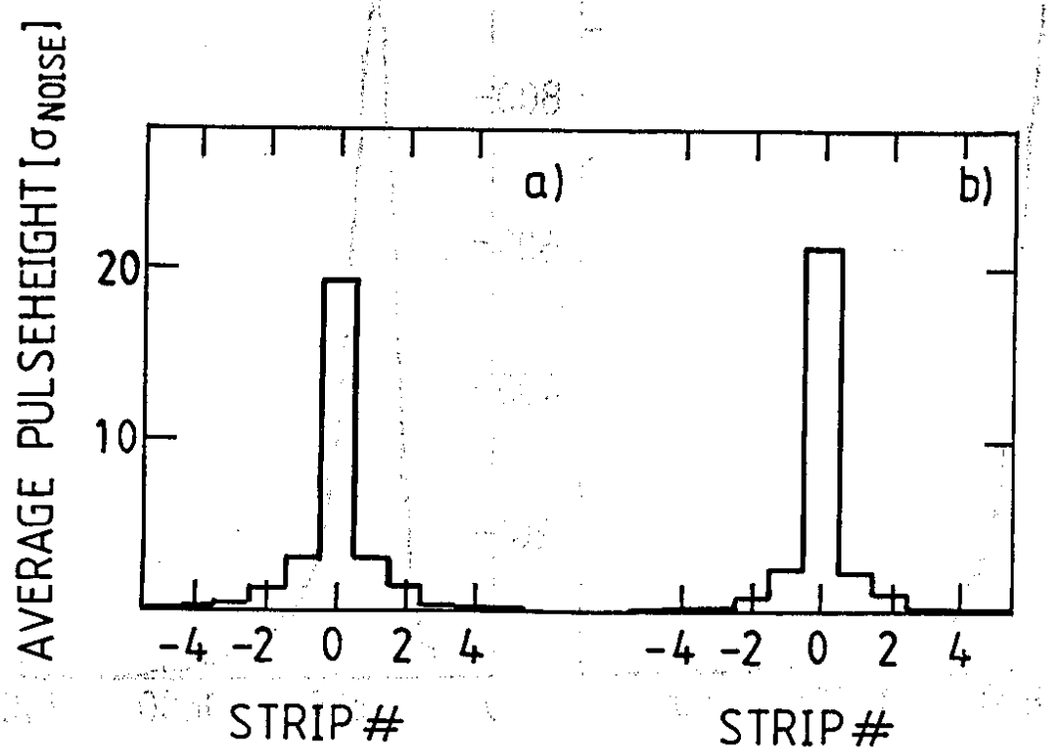

AVERAGE PULSEHEIGHT [σNOISE]
20
10
a)
b)
-4 -2 0 2 4
-4 -2 0 2 4
STRIP#
STRIP#

Fig.7

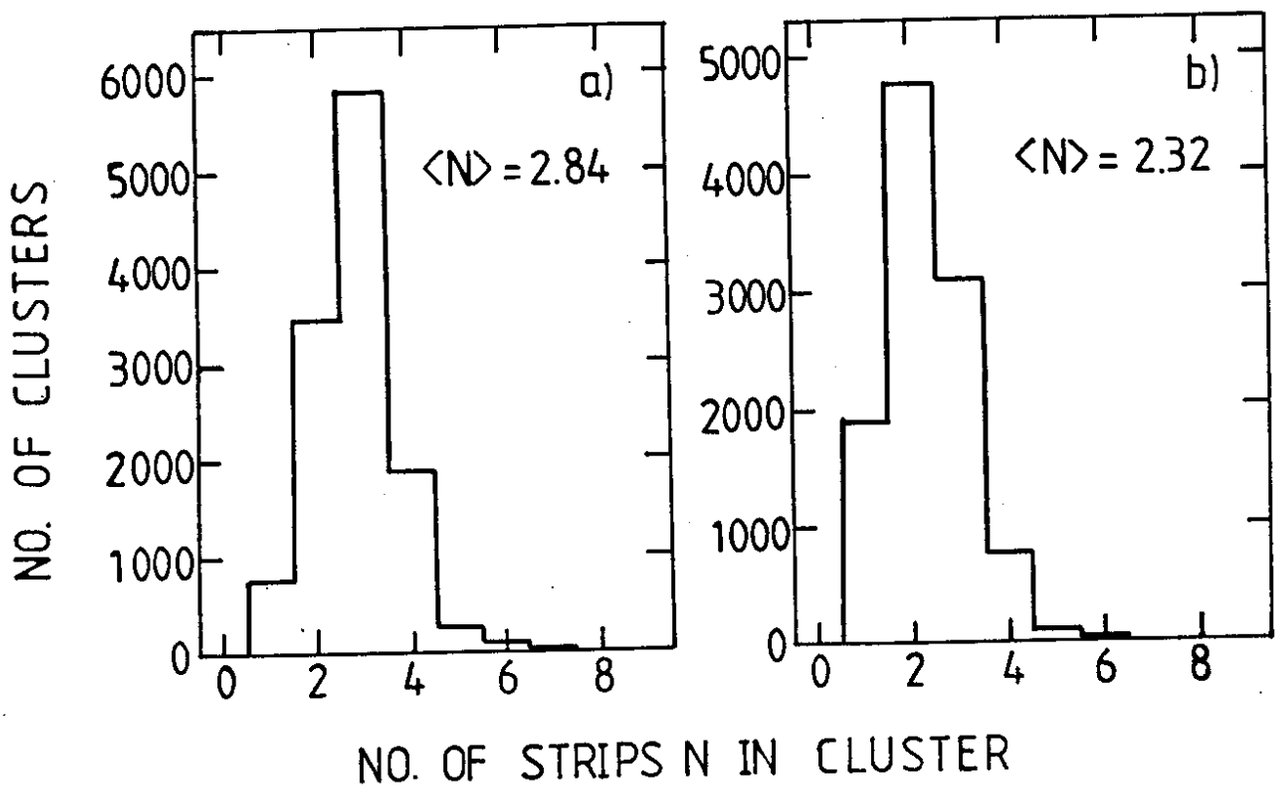

NO. OF CLUSTERS
6000
5000
4000
3000
2000
1000
0
a)
<N> = 2.84
0 2 4 6 8
5000
4000
3000
2000
1000
0
b)
<N> = 2.32
0 2 4 6 8
NO. OF STRIPS N IN CLUSTER

Fig. 8

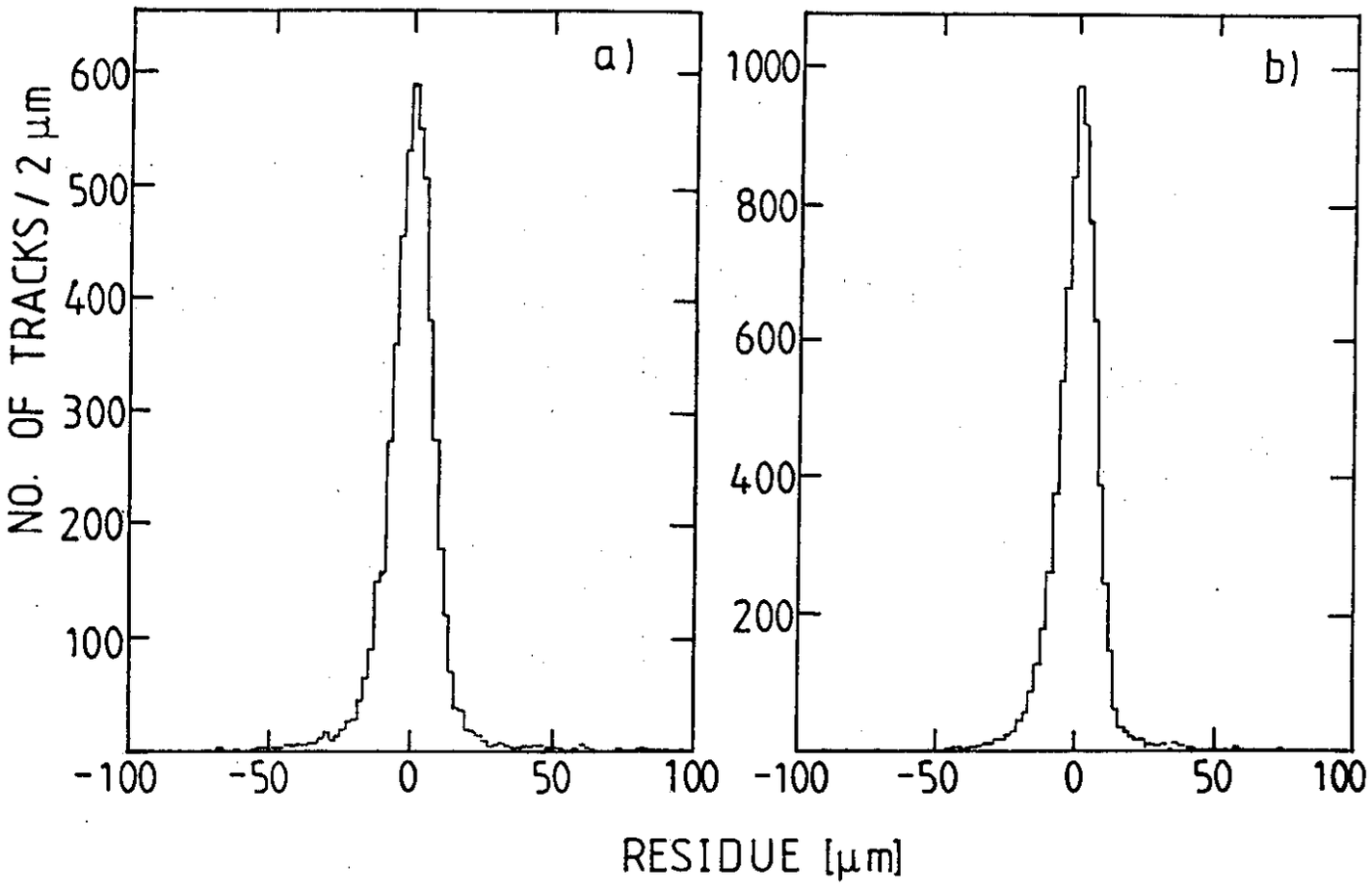

a)
b)
NO. OF TRACKS / 2 µm
600
500
400
300
200
100
1000
800
600
400
200
-100
-50
0
50
100
RESIDUE [µm]

Fig. 9