P. Sivonen, S. Kangasmaa, and A. Pärssinen, A SiGe RF front-end with on-chip VCO for a GPS receiver, in Proceedings of the European Solid-State Circuits Conference, pp. 435-438, Florence, Italy, Sep. 2002.

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A SiGe RF Front-End with On-Chip VCO for a GPS Receiver

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Abstract

A GPS direct conversion RF front-end with on-chip VCO fabricated in 0.35μm SiGe BiCMOS technology is presented. The properties of inductively degenerated common-emitter LNA and resistively degenerated Gilbert downconversion mixer are examined. The approximative equations for the front-end DSB-NF and IIP3 are given. By applying the derived formulas, the front-end performance can be readily estimated and optimized. The implemented RF front-end has a voltage conversion gain of 25.8 dB, DSB-NF of 2.7 dB, IIP3 of -14.5 dBm and IIP2 of +26 dBm. The 3.15 GHz VCO has a phase noise of -99 dBc/Hz at 100 kHz offset. The front-end draws 15.3 mA from a 2.7 V supply.

1. Introduction

As GPS receivers become common in portable mass products, the power consumption, cost, size, and yield of the receiver parts become critical. Here, a low-power, robust, and high-performance 0.35μm SiGe RF front-end for a GPS receiver is presented. The on-chip RF section of the receiver (Fig. 1) consist of an LNA, I and Q mixers, LO buffers, divide-by-two quadrature generator, and double-frequency VCO. In order to reject the interference from substrate or supply, balanced circuits are employed. The receiver is mounted in a QFN package.

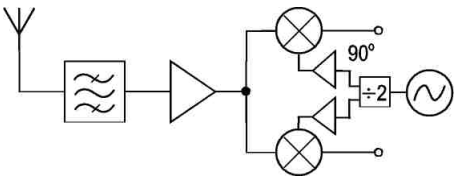

Figure 1. RF front-end of GPS homodyne receiver.

2. LNA

The LNA is based on the most commonly used topology i.e. inductively degenerated common-emitter amplifier as shown in Fig. 2. The preselection filter with single-ended input and balanced output transforms the single-ended signal differential for LNA, thus, omitting the need for additional balun. The LNA input impedance at the frequency of operation was selected to be 50 Ω differential instead of 100 Ω. The parasitic package capacitance C_p at the transistor base, within same order of magnitude as C_π, makes it difficult to realize an input impedance larger than 50 Ω without wasting power or using large emitter inductance. The impedance level could be increased also by a passive impedance transformation network, but this would require extra components complicating the design and increasing the cost.

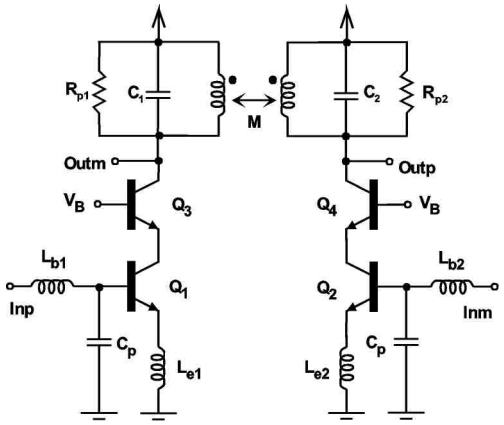

Figure 2. Schematic of LNA.

The amplifier is biased with PTAT base current driven through 20 kΩ resistors used to isolate the bias circuit from the signal path. The sizes of the input devices Q_1 and Q_2 are selected to be 4 x minimum size in order to ensure that the contribution of the base resistance r_b to the amplifier noise figure is negligible. The devices Q_1 and Q_2 are biased at the collector current of 1.1 mA each and then the required emitter inductance to realize an input impedance of 50 Ω is about 1.1 nH. Finally, in order to series resonate the input impedance at 1.575 GHz, the (external) base inductors of about 8.2 nH are needed.

If the noise contributions of the cascode transistors are neglected and perfect input matching ($R_{in} = R_s$) is assumed, the LNA noise figure at the resonance frequency ω_0 can be approximated as

$$NF_{LNA} = 1 + \frac{R_{lb}}{R_s} + \frac{r_b k^2}{R_s} + \frac{g_m R_s}{2\beta_0 k^2} + \frac{k^2}{2 g_m R_s \beta_0}\left(\frac{\omega_T}{\omega_0}\right)^2 + \frac{g_m R_s}{2k^2}\left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{4R_s}{R_L k^2}\left(\frac{\omega_0}{\omega_T}\right)^2 \quad (1)$$

where $\omega_T \approx \frac{g_m}{C_\pi}$ and $k = \frac{C_\pi}{(C_p + C_\pi)}$. For the designed LNA, $R_{lb} = 2.2\ \Omega$, $r_b = 5.0\ \Omega$, $R_s = 25\ \Omega$, $k = 0.5$, $g_m = 43$ mS, $\beta_0 = 88$, $C_\pi = 575$ fF and $R_L = 80\ \Omega$.

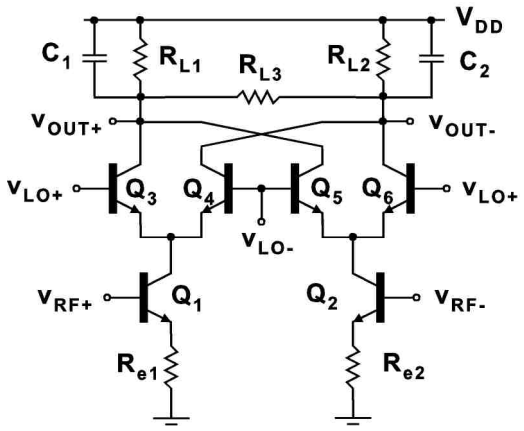

Figure 3. Schematic of downconversion mixer.

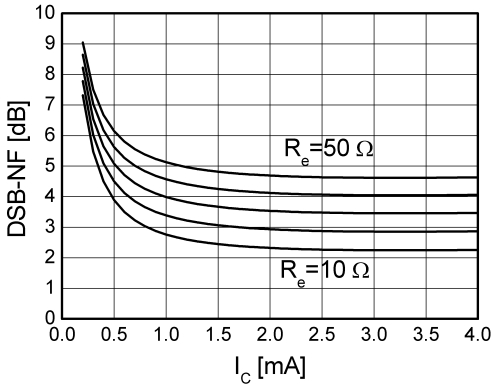

Figure 4. DSB-NF given by Eq. (3).

Substituting data into Eq. (1) gives

$$NF_{LNA}=1+\frac{2.20}{25}+\frac{1.20}{25}+\frac{2.46}{25}+\frac{0.98}{25}+\frac{2.26}{25}\approx 1.35\ dB. \quad (2)$$

Simulations predict 1.54 dB with cascode transistors making some contribution. The largest contributions in this case are seen to be the base shot noise $\overline{i_b^2}$ of the device, the equivalent parallel load resistance R_L and the series resistor R_{lb} of the base inductor L_b, respectively. The noise contributions of the cascode devices are minimized by using the minimum area devices because then the capacitances at their emitters are minimized [1].

A tuned load peeks the gain of the amplifier at 1.575 GHz. The load comprises a 7 nH differential inductor resonating with the parallel capacitance of 0.95 pF, realized with $C_1 = C_2 = 1.9$ pF, and parasitics. The parallel resistors R_{pi} set the LNA voltage gain to 20.5 dB. The LNA and mixers are ac-coupled with the 4 pF capacitors.

3. Downconversion Mixer

The downconversion mixers are implemented as modified Gilbert cells with resistively degenerated common-emitter RF input stages as shown in Fig. 3. To relax the linearity requirements of the following baseband block, the output of the mixer consist of a first-order RC low-pass filter. The resistors $R_{L1} - R_{L2}$ are used to set the output common-mode level. The mixer voltage gain can be tuned to the desired value by tuning the resistance R_{L3}.

If the noise contribution of the switching quad is neglected and the mixer commutation is assumed square-wave like [2], the mixer DSB-NF can be approximated as

$$NF_{DSB} = \frac{\pi^2}{8}(1 + \frac{r_b}{R_{out1}} + \frac{g_m(R_{out1}+R_e)^2}{2R_{out1}\beta_0} + \frac{1}{2g_mR_{out1}} + \frac{R_e}{R_{out1}} + \frac{2(1+g_mR_e)^2}{g_m^2R_LR_{out1}}) \quad (3)$$

where R_{out1} is the single-ended LNA output impedance. Figure 4 shows the DSB-NF given by Eq. (3) as a function of collector bias current I_c with emitter degeneration resistance values $R_e = 10, 20, 30, 40, 50\ \Omega$. The component values used are $r_b = 5.0\ \Omega$, $R_{out1} = 80\ \Omega$, $\beta_0 = 88$ and $R_L = 190\ \Omega$.

The linearity of the front-end is dominated by the mixer and the main source of mixer nonlinearity is the input RF stage. Thus, the odd-order nonlinearity of the mixer can be examined by using the results derived in [3], in which the high-frequency nonlinearity equations in Volterra series for the degenerated common-emitter amplifier stage are derived. Using two input signals of the same amplitude V_s at frequencies ω_a and ω_b, the magnitude of the input-referred IM_3 products at frequencies $(2\omega_a - \omega_b)$ and $(2\omega_b - \omega_a)$ of the mixer RF input stage is given by [3]

$$|IM_3| \approx |\frac{A_1(s)}{I_c}|^3 |\frac{V_T}{4}[1+sC_{je}Z(s)]\{-1+\frac{A_1(\triangle s)}{g_m} + \frac{A_1(2s)}{2g_m}[1+2sC_{je}Z(2s)]\}||V_s|^2 = |K(s)||V_s|^2 \quad (4)$$

where $Z(s) = Z_b(s) + R_e$, Z_b is the impedance at the base, and $A_1(s)$ is the Volterra series coefficient. If it is assumed that the IIP3 of the whole front-end is mainly determined by the mixer linearity, the IIP3 in dBm of the front-end is given by

$$IIP3 = 10\log\left(\frac{2}{A_v^2 \cdot |K(s)| \cdot R_s \cdot 1mW}\right) \quad (5)$$

where A_v is the LNA voltage gain (20.5 dB). Figure 5 shows the IIP3 of the front-end given by Eq. (5) as a function of I_c with $R_e = 10, 20, 30, 40, 50\ \Omega$.

In this design, the mixer was biased with the collector current of 1.3 mA and the emitter degeneration resistance of 30 Ω was used. With these parameters the designed mixer has a low contribution to the front-end noise figure and the linearity of the front-end is sufficient with a low-power consumption. By substituting the data of the mixer designed in this work to Eq. (3) gives

$$NF_{DSB} = \frac{\pi^2}{8}(1 + \frac{5.0}{80} + \frac{3.6}{80} + \frac{9.5}{80} + \frac{30.0}{80} + \frac{25.2}{80}) \approx 3.7\ dB. \quad (6)$$

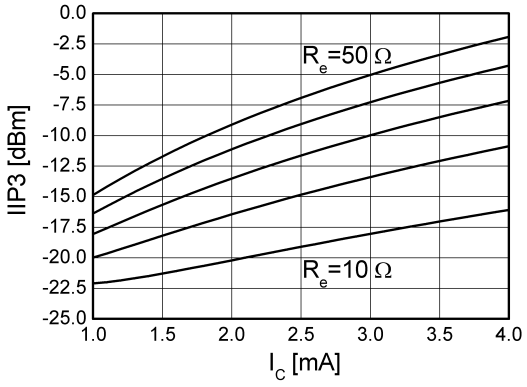

Figure 5. IIP3 of front-end given by Eq. (5).

Simulations predict 4.1 dB with the switching quad making some contribution. In this case, the largest contributions to the mixer noise figure are seen to be the R_e, the equivalent load resistance R_L and the collector shot noise i_c of the RF input device, respectively.

The DSB-NF of the whole front-end is given by [4]

$$NF = NF_{LNA} + 2 \cdot \frac{(NF_{DSB} - 1)}{G_a} \qquad (7)$$

where the G_a is the LNA available power gain given by

$$G_a = \frac{A_v^2}{4} \frac{R_s}{R_{out1}} = \frac{10.6^2}{4} \cdot \frac{25\Omega}{80\Omega} \approx 9.4\, dB. \qquad (8)$$

The factor of two in Eq. (7) is due to the fact that there are two mixers whose noise is uncorrelated. By substituting the data in Eq. (7) the DSB-NF of the front-end is finally given as

$$NF = 1.38 + 2 \cdot \frac{(2.36 - 1)}{8.77} \approx 2.2\, dB. \qquad (9)$$

Simulations predict 2.3 dB. In addition, with the values used in this design, Eq. (5) predicts $IIP3 \approx -16.5$ dBm for the front-end. The simulations with typical process parameters give the same result.

4. LO Circuitry

The block diagram of the LO circuitry is shown in Fig. 6. The double-frequency VCO drives the flip-flops to produce the desired LO frequency with quadrature phases. The buffered LO signals drive the I and Q mixers.

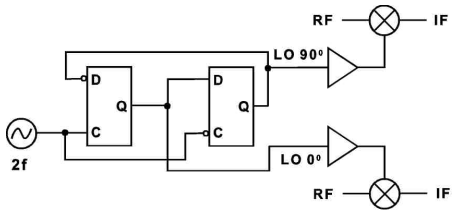

Figure 6. Block diagram of LO circuitry.

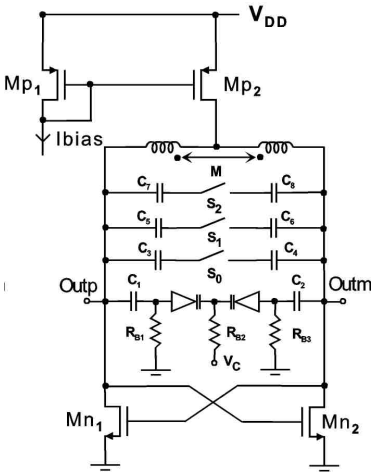

Figure 7. Schematic of VCO.

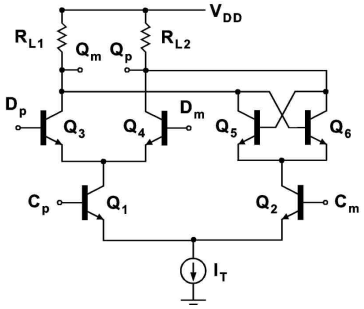

Figure 8. Schematic of flip-flop.

The VCO (Fig. 7) consists of a cross-coupled NMOS pair with a PMOS current source. A 1.5 nH differential inductor, a switchable 3-bit array of binary-weighted capacitors, and a pn-junction varactors tune the VCO to 3.15 GHz. The VCO has a continuous tuning range of 115 MHz whereas the discrete tuning scheme extends the total tuning range to 508 MHz. With the differential inductor Q of 15, the VCO output swing is about 1.8 V_{PP} at 3 mA bias current. The source-follower buffer couples the VCO to the frequency divider.

The flip-flops (Fig. 8) use the minimum size transistors to maximize the speed with a low current consumption. The tail current is 450 μA and the implemented bias current is inversely proportional to the reference resistor realized with the same material as the load resistors of flip-flops. This kind of biasing method minimizes the output voltage swing variations due to the variations of load resistors. The load resistors of 700 Ω set the output voltage swing to 600 mV_{PP}.

The LO buffer consists of an emitter-follower and so-called totem-pole stage [5]. The totem-pole circuit combines the advantages of emitter-follower and common-emitter stages in the sense of charging and discharging a load capacitance. Each LO buffer is biased at the constant bias current of 850 μA. The constant bias was found to best stabilize the LO voltage level of 500 mV_{PP} driving the mixers.

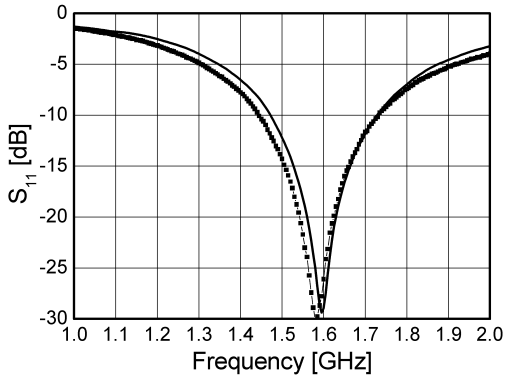

Figure 9. Measured and simulated (solid line) LNA input impedance matching.

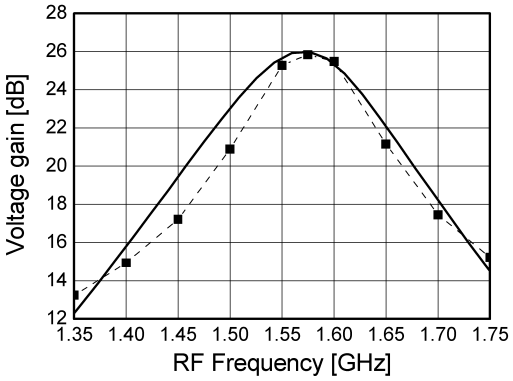

Figure 10. Measured and simulated (solid line) RF front-end voltage gain.

5. Measurement Results

The LNA scattering parameter S_{11} and RF front-end voltage conversion gain are plotted in Figures 9 and 10. As the mixer voltage conversion gain was designed to be 5.5 dB, the total RF front-end voltage gain is about 26 dB. The measured VCO phase noise is shown in Fig. 11. The most relevant results of the front-end are summarized in Table 1. The reported current consumption includes an LNA (2.7 mA), VCO + buffer (3.0 mA + 0.6 mA), phase shifter (1.0 mA), LO buffers (1.7 mA), and mixers (6.3 mA). The current consumption of 15.3 mA is higher than the expected 13.9 mA because the bias current used to bias the front-end was generated on-chip and this reference current varies with process.

6. Conclusions

A GPS direct conversion RF front-end with on-chip VCO fabricated in 0.35μm SiGe BiCMOS technology is presented. The equations representing the properties of the front-end are given. By applying the derived formulas, the front-end performance can be readily evaluated and optimized at the early state of the design. The results of the analysis are found to be consistent with the simulated and measured performance.

The authors wish to thank Ari Vilander, Lassi Hyvönen, and Pauli Seppinen for assistance and expertise.

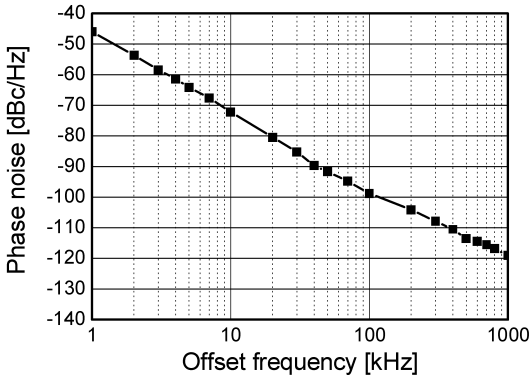

Figure 11. Measured VCO phase noise.

Table 1. RF front-end simulated and measured results.

Parameter	Sim.	Meas.	Unit
S_{11} (balanced 50 Ω)	-29	$\leq$ -25	dB
Voltage gain	26.0	25.8	dB
DSB-NF	2.3	2.7	dB
Phase imbalance	na	≤ 3.0	deg
Gain imbalance	na	0.1	dB
P_{-1dB}(in-band)	-26.9	-27.6	dBm
IIP3 (in-band)	-16.5	-14.5	dBm
IIP2 (in-band)	na	+26.0	dBm
LO level at RF input	na	-105	dBm
VCO total tuning range	18	16	%
Phase noise @ 100 kHz	-94	-99	dBc / Hz
Pushing	na	-1.6	MHz / V
Current consumption	13.9	15.3	mA

7. References

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