A silicon avalanche photodetector fabricated with standard CMOS technology with over 1 THz gain-bandwidth product

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Abstract: We present a silicon avalanche photodetector (APD) fabricated with standard complementary metal-oxide-semiconductor (CMOS) technology without any process modification or special substrates. The CMOS-APD is based on N^+/P-well junction, and its current-voltage characteristics, responsivity, avalanche gain, and photodetection frequency response are measured. Gain-bandwidth product over 1 THz is achieved with the CMOS-APD having avalanche gain of 569 and 3-dB photodetection bandwidth of 3.2 GHz.

OCIS codes: (040.0040) Detectors; (040.1345) Avalanche photodiodes (APDs); (040.5160) Photodetectors; (040.6040) Silicon; (200.0200) Optics in computing; (200.4650) Optical interconnects; (230.0230) Optical devices; (230.0040) Detectors; (230.5160) Photodetectors; (230.5170) Photodiodes; (250.0250) Optoelectronics; (250.0040) Detectors; (250.1345) Avalanche photodiodes (APDs).

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#135192 - $15.00 USD Received 15 Sep 2010; revised 13 Oct 2010; accepted 19 Oct 2010; published 3 Nov 2010

1. Introduction

With the data rate between electronic appliances continuously increasing, the interconnect bottleneck becomes a serious problem [1,2]. As a solution for this problem, optical interconnect technology has been vigorously investigated. In particular, silicon photonics has been actively investigated for optical rack-to-rack, board-to-board, and chip-to-chip interconnects because silicon photonics can provide low-cost solutions for high-speed interconnects with the possibility of photonic components integrated with silicon electronics [2,3]. Such an expectation is especially high for monolithic electronic-photonic integrated circuits (EPICs) based on complementary metal-oxide-semiconductor (CMOS) technology as CMOS is the dominant platform for most integrated circuits [3–5].

In order to realize CMOS EPICs for optical interconnects, implementation of high-speed and high-responsivity photodetectors is required. Germanium-based photodetectors have been investigated due to their large absorption coefficient at 1.3-μm and 1.5-μm wavelengths as well as compatibility with CMOS technology [6–8]. Another interesting approach is using standard CMOS technology without any modifications for 850-nm photodetector realization. Although such CMOS-compatible photodetectors (CMOS-PDs) suffer from limitations of non-optimal device structures, they have advantages of low fabrication cost and high volume manufacturability. A high-performance CMOS-PD monolithically integrated with CMOS circuits can immediately provide very cost-effective solutions for many optical interconnect applications.

Several approaches have been tried to improve the bandwidth-efficiency product of CMOS-PDs, which have the inherent disadvantage of narrow depletion regions provided by high doping concentrations in standard CMOS technology. To suppress slow diffusion components in photocurrents, a spatially modulated light (SML) photodetector was reported [9]. The SML photodetector has 3-dB photodetection bandwidth of about 500 MHz, but, it suffers from low responsivity. A photodetector formed by multiple p^+-p-n structure in standard CMOS technology was reported, which provides high responsivity with the large depletion region and avalanche gain [10]. However, it has disadvantages of relatively high dark currents, low avalanche gain, and limited bandwidth. Based on the same structure, bandwidth enhancement was achieved with elimination of slow diffusion photogenerated carriers by body biasing [11]. Although bandwidth can be enhanced with this approach, responsivity is severely reduced owing to the decreased depletion region of N-well/P-substrate junction and reduced diffusion currents from P-substrate. We have demonstrated CMOS-compatible avalanche photodetectors (CMOS-APDs) based on P^+/N-well junctions fabricated with standard CMOS technology [12], and Iiyama et al. reported hole-injection-type and electron-injection-type CMOS-APDs [13]. These CMOS-APDs provide high-speed operation with reduction of slow photogenerated carriers in the P-substrate region, and high responsivity with internal gain provided by the avalanche multiplication process.

In this paper, we investigate a CMOS-APD based on N^+/P-well junction, which can be realized with standard CMOS technology. Current-voltage relation, responsivity, avalanche gain, and photodetection bandwidth are characterized. The fabricated CMOS-APD has responsivity of 2.94 A/W with avalanche gain of 569 and 3-dB bandwidth of 3.2 GHz at the reverse bias voltage of 10.6 V, achieving the highest gain-bandwidth product among CMOS-PDs reported until now.

#135192 - $15.00 USD Received 15 Sep 2010; revised 13 Oct 2010; accepted 19 Oct 2010; published 3 Nov 2010

2. Device description

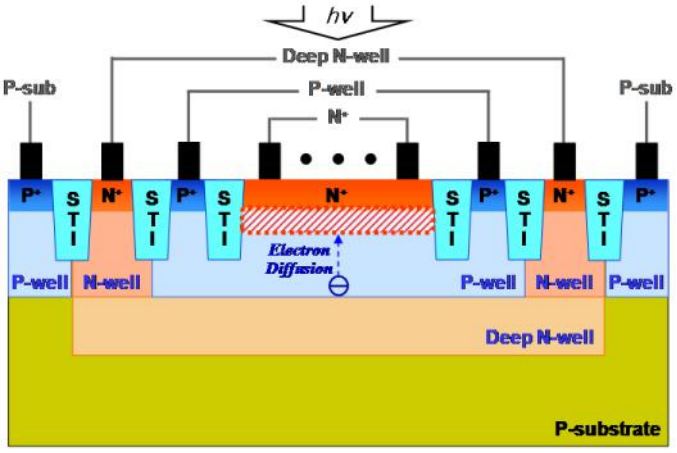

Fig. 1. Cross-sectional structures of the fabricated CMOS-APD.

Figure 1 shows the CMOS-APD based on N^+/P-well junction. The CMOS-APD was designed and fabricated with 65-nm standard CMOS technology without any process modification. It can be realized without violating any design rules for the CMOS process technology. It includes shallow trench isolation (STI) between P^+ and N^+ regions, which prevent premature edge breakdown. The reverse bias voltage is applied to the N^+/P-well junction, and photocurrents are extracted from N^+ contacts located inside P-well. N^+ contacts for Deep N-well and P^+ contacts for P-substrate are both tied to ground in order to exclude any influence of Deep N-well and P-substrate on photodetection. An optical window having the area of 30 by 30 μm^2 is formed by blocking the salicide process.

3. Measurement results and analyses

For CMOS-APD characterization, an 850-nm laser diode was used as an optical source, and a lensed-fiber was used for injecting light into the CMOS-APD on wafer. All measurements were done at room temperature. For DC measurements, 0.1 mW of light measured at the lensed-fiber output was injected into the CMOS-APD.

3.1 Current-voltage characteristic

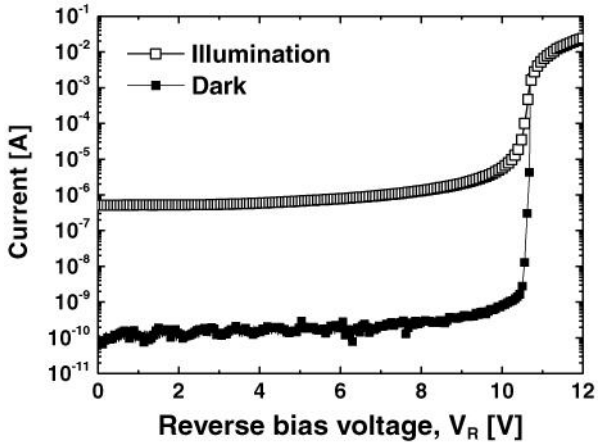

Fig. 2. Current-voltage characteristics of the CMOS-APD under illumination and dark conditions.

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Figure 2 shows measured current-voltage characteristics of the fabricated CMOS-APD with and without optical illumination. The avalanche breakdown voltage can be defined as the voltage at which the dark current reaches 10 μA [6,7], and, with this definition, the avalanche breakdown voltage of the CMOS-APD is about 10.7 V. When the reverse bias voltage is small, the CMOS-APD has low photocurrents of about 0.5 μA. With the reverse bias voltage approaching the avalanche breakdown voltage, photocurrents start to increase dramatically with internal gain provided by the avalanche multiplication process.

3.2 Responsivity and avalanche gain

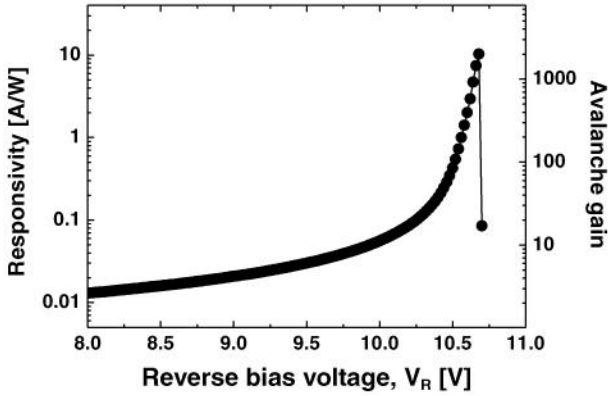

Fig. 3. Responsivity and avalanche gain of the CMOS-APD as a function of the reverse bias voltage.

Figure 3 shows responsivity and avalanche gain of the CMOS-APD as a function of the reverse bias voltage. The photocurrent is determined by subtracting the dark current from the photodetected current, and the avalanche gain is determined by the ratio of photocurrent at a given bias to that at the reverse voltage of 1 V, where avalanche gain is insignificant. Responsivity increases initially with the reverse bias voltage due to the increased depletion width, and dramatically in the avalanche regime due to the high avalanche gain. The maximum responsivity is 10.3 A/W, corresponding to avalanche gain of 1993, at the reverse bias voltage of 10.68 V. With further increase in the reverse bias voltage, however, avalanche gain rapidly go down with rapid increase in dark currents.

3.3 Photodetection frequency response and bandwidth

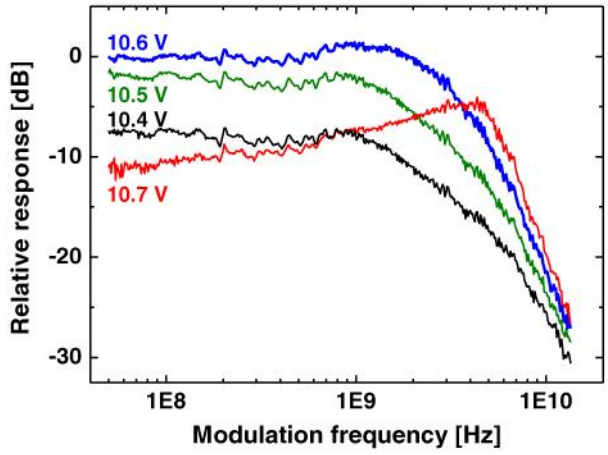

Fig. 4. Photodetection frequency responses of the CMOS-APD at different bias voltages.

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For photodetection frequency response measurement of the CMOS-APD, an electro-optical modulator and a vector network analyzer were used with prior calibration of cables and RF connectors. The average optical power injected into photodetectors was 0.1 mW, and the measured frequency range was from 50 MHz to 13.5 GHz. Figure 4 shows photodetection frequency responses of the CMOS-APD at different bias voltages approaching the avalanche breakdown. As the reverse bias voltage is increased, the photodetection frequency response increases because of increased avalanche gain but goes down when the reverse bias voltage exceeds the maximum avalanche gain condition. In addition, peaking in the response can be observed, especially with a large reverse bias voltage, which is due to the inductive component produced in the avalanche regime [12,14]. The maximum 3-dB bandwidth achieved is about 3.2 GHz at the reverse bias voltage of 10.6 V. Our CMOS-APD has better bandwidth performance than other CMOS-PDs previously reported since using only N^+/P-well junction for photodetection excludes the contribution of slow diffusion photogenerated carriers in the P-substrate region. The charge neutral P-well region is much thinner than the P-substrate region, and consequently, carrier transport by diffusion takes less time, resulting in better bandwidth performances. In addition, the CMOS-APD based on N^+/P-well junction has higher bandwidth than P^+/N-well type CMOS-APD [12], because electrons move faster in P-well than holes in N-well.

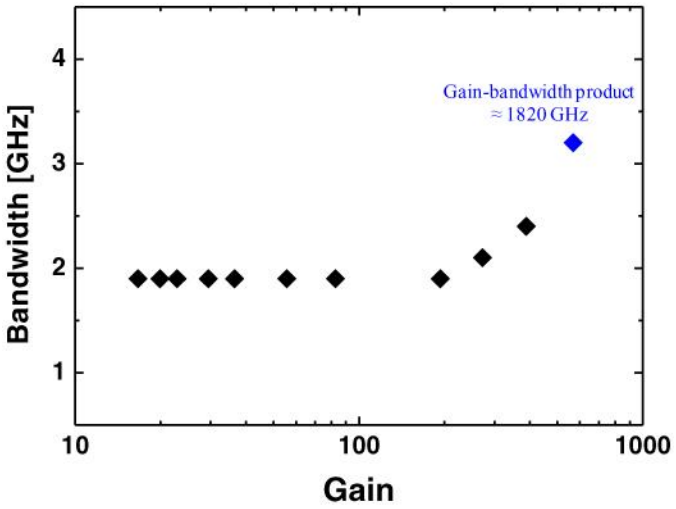

Fig. 5. Gain-bandwidth characteristic of the CMOS-APD.

Figure 5 shows measured 3-dB bandwidth as a function of measured avalanche gain. The increase in 3-dB bandwidth for gain larger than about 200 is due to the enhanced peaking effect in the photodetection response [12,14]. Due to this, our CMOS-APD does not show the decreasing 3-dB bandwidth with the increasing gain as has been observed in other APDs. The maximum gain-bandwidth product achieved is about 1820 GHz with corresponding avalanche gain of 569 and 3-dB bandwidth of 3.2 GHz at the reverse bias voltage of 10.6 V. At this bias, the photodetected current is about 300 μA and the dark current is about 0.3 μA.

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Table 1. Performance comparison of silicon avalanche photodetectors fabricated with standard CMOS technology

	[10]	[11]*	[13]**		This work
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS		65-nm CMOS
Structure	Multiple p^+-p-n APD	Multiple p^+-p-n APD with body contact	Hole-injection-type APD	Electron-injection-type APD	N^+/P-well APD
R	0.74 A/W	0.085 ~0.38 A/W	0.4 ~2.2 A/W	0.6 ~2.3 A/W	2.94 A/W
M	2	3 ~7	45 ~260	72 ~280	569
BW	1.6 GHz	2.8 ~1.4 GHz	2 ~0.35 GHz	2.4 ~0.65 GHz	3.2 GHz
GBP	3.2 GHz	8.4 ~9.8 GHz	90 GHz	180 GHz	1820 GHz

R: responsivity, M: avalanche gain, BW: bandwidth, GBP: gain-bandwidth product * Estimated from data shown in Fig. 1 and Fig. 2 of ref. 11 ** Estimated from data shown in Fig. 3 and Fig. 5 of ref. 13

Table 1 compares various published results of silicon avalanche photodetectors in standard CMOS technology with our work. The electron-injection-type APD reported by Iiyama et al. [13] has the same junction structure as our APD, but our APD has much better performance due to, we believe, the STI which allows much higher field across junction before breakdown. To the best of our knowledge, this work achieves the highest gain-bandwidth product reported for silicon photodetectors fabricated with standard CMOS technology.

4. Conclusion

A CMOS-APD based on N^+/P-well junction is fabricated and characterized with the goal of achieving high-gain and high-speed photodetectors. Its current-voltage characteristics, responsivity, avalanche gain, and photodetection bandwidth are investigated. It achieves the responsivity of 2.94 A/W with avalanche gain of 569 and 3-dB bandwidth of 3.2 GHz, corresponding to gain-bandwidth product of about 1820 GHz. With this, high-performance and cost-effective monolithic CMOS optical receivers can be realized, which can play an important role for optical interconnect applications.

Acknowledgments

This work was supported by the IT R&D program of MKE/KEIT [002145]. The authors are very thankful to IDEC for EDA software support. The authors also would like to thank Dr. H.-S. Kang in Samsung Electronics Corporation for many useful discussions.

#135192 - $15.00 USD Received 15 Sep 2010; revised 13 Oct 2010; accepted 19 Oct 2010; published 3 Nov 2010