

A Silicon-Based Electrical Source for Surface Plasmon Polaritons

Robert J. Walters,^a Rob V. A. van Loon,^a Ihor Brunets,^b Jurriaan Schmitz,^b and Albert Polman^a

^aCenter for Nanophotonics, FOM Institute for Atomic and Molecular Physics,
Science Park 113, 1098XG Amsterdam, The Netherlands

^bMESA+ Institute for Nanotechnology, University of Twente,
P.O. Box 217, 7500AE Enschede, The Netherlands
Contact e-mail: walters@amolf.nl

I. INTRODUCTION

AFTER nearly forty-five years of scaling driven by Moore's Law, the silicon microelectronics world is now defined by length scales that are some ten times smaller than the dimensions of typical micro-optical components. This size mismatch poses an important challenge for those working to integrate photonics with CMOS technology. One promising solution is to move from optical components made with dielectric materials to metal-dielectric interfaces, where optical modes called surface plasmon polaritons (SPPs) offer unique opportunities to confine and control light [1]. Research groups working in the rapidly developing field of plasmonics have now demonstrated many passive components that suggest the potential of SPPs for applications in sensing and integrated optical communication. Recently, the first active plasmonic devices based on III-V materials [2] and organic materials [3] have been reported. Here we demonstrate that a silicon-based electrical source for SPPs can be fabricated using established microtechnology processes that are compatible with back-end CMOS technology.

The metal-insulator-metal (MIM) plasmon waveguide geometry is particularly promising for electrically driven SPP sources, because the metallic cladding layers that support and guide the SPP mode can also serve as contact electrodes. In our devices, optically thick gold cladding layers surround a semi-insulating layer of alumina that contains optically active silicon nanocrystals. When a current is applied through the insulator layer, the embedded nanocrystals are excited by an impact ionization process. Through an appropriate choice of insulator thickness, the only radiative decay pathways available to excited nanocrystals are plasmonic modes. This results in electrical SPP excitation over a spectral range determined by the properties of the silicon nanocrystals, including the distribution of nanocrystal sizes, morphologies, and surface passivation conditions.

II. DEVICE FABRICATION

Typically, silicon nanocrystals are created in a silica host material by annealing silicon-rich silicon oxides (SiO_x ; $x < 2$) at high temperatures ($> 900^\circ\text{C}$). These methods are incompatible with the maximum temperatures that can be tolerated during back-end CMOS processing without damaging the metal interconnect layers ($\sim 450^\circ\text{C}$).

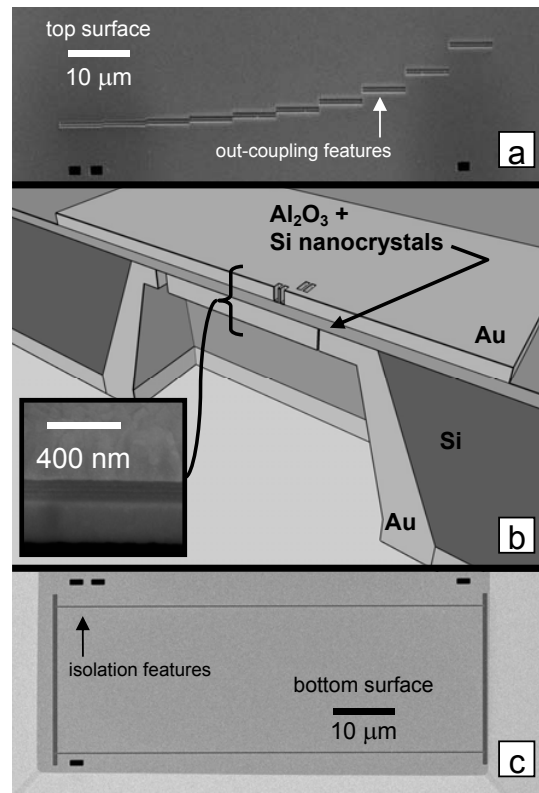


Figure 1. An electrical source for SPPs in a MIM waveguide geometry is shown schematically in (b), with an inset cross sectional SEM image of the device. Plan-view SEM images of the top (a) and bottom (c) surfaces of the suspended membrane respectively depict the out-coupling and isolation structures created by focused ion beam milling. Light is scattered from electrically generated plasmons into the far field from the structures in the top surface.

In our fabrication process, the optically active silicon nanocrystal material is instead obtained by sequential atomic layer deposition (ALD) of 20 nm thick layers of Al_2O_3 (at 300°C) and low pressure chemical vapor deposition (LPCVD) of silicon (at 325°C). This process flow results in smooth and abrupt interfaces and allows precise control of both the insulator layer thickness and the internal locations of nanocrystal layers [4]. Four layers of silicon and five layers of alumina are grown without vacuum break for a total insulator layer thickness of ~ 100 nm.

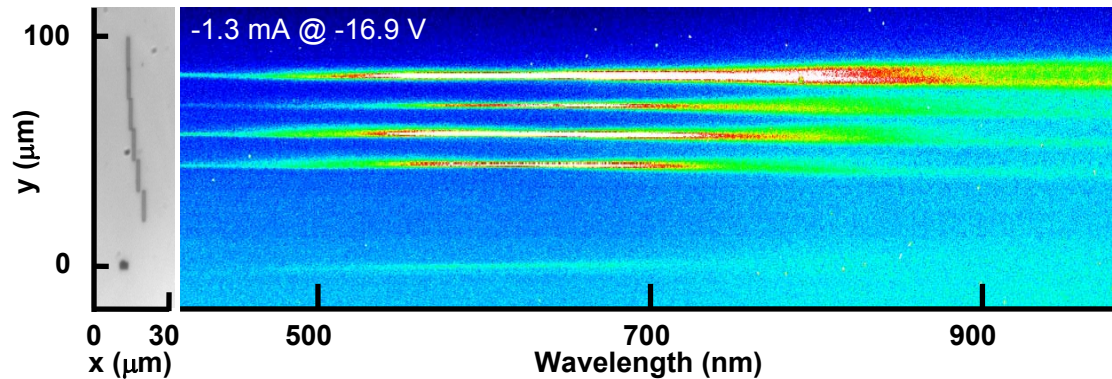


Figure 2 (color). A typical exposure shows that electroluminescence is detected from the SPP source. In the grey-scale image at left, the top surface of the membrane is imaged on the CCD camera through the spectrometer by collecting the zero-order diffraction of reflected illumination. The y-axis-aligned false color spectral map at right shows the corresponding emission spectra measured using the first order grating diffraction (with an arbitrary color-scale adjusted for contrast) at a bias of -16.9 V. The exposure time was 2000 sec and the peak signal intensity is ~20000 counts above the floor of ~600 counts.

After depositing the optically active material, 300 nm of gold was sputtered onto the wafer to form the top gold cladding and electrical contact layer. At the back surface of the substrate wafer, 300 nm of SiO₂ was deposited by plasma-enhanced chemical vapor deposition (PECVD), patterned using optical lithography, and etched in buffered hydrofluoric acid (BHF) solution to serve as a hard mask for a tetra-methyl ammonium hydroxide (TMAH) anisotropic etch solution. The wafer was back-etched to the alumina layer to create rectangular membranes of 50 μm x 100 μm in dimension. The top gold layer was then patterned using optical lithography and chemical etching with contact pads (1 mm x 1 mm) aligned to the underlying membranes. The MIM structure was completed by sputtering 300 nm of gold to the underside of the membrane through a physical mask to form the bottom cladding/contact layer. Isolation and out-coupling features were then milled by focused ion beam (FIB) into the top and bottom surfaces of the device, as shown in figure 1(a) and 1(c).

III. ELECTRICALLY GENERATED SPPs

We observe light at the out-coupling structure locations when a current is passed through the membrane device and the applied bias is greater than ~10 V in magnitude. A typical measurement is shown in figure 2. The broad, near infrared spectrum of the emitted light matches the photoluminescence and electroluminescence we measure in metal-insulator-semiconductor (MIS) diode test structures containing similar silicon nanocrystal doped alumina active layers. The emission is polarized perpendicular to the out-coupling structures. We attribute the electroluminescence to the scattering of SPPs that are generated in active regions of the device, when excitons in silicon nanocrystals excited by impact ionization decay radiatively into the plasmonic modes of the MIM waveguide.

We see significant changes in both the pattern and intensity of the out-coupled light over time-scales of a few seconds that we attribute to accumulating damage sites in the active layer of the device. These damage sites create thermally unstable “hot spots” where the local current density is much

higher than the average current density. As a result, SPPs are not generated uniformly in the active area outside the electrically isolated out-coupling structure region. In some measurements, we observe regions that show the expected intensity-decay and spectral-shift signatures of SPP propagation through the isolated section of the MIM waveguide, but the non-uniformity of SPP generation obfuscates any simple comparison of emission spectra at the different out-coupling structure locations. However by averaging in time and binning in both space and wavelength, we can recover a suggestive trend. As shown in figure 3, out-coupling structures placed at a greater distance from the isolation slit, corresponding to longer SPP propagation distances within the MIM waveguide, show a red-shift in relation to closer out-coupling structures. This corresponds well to calculations predicting that SPPs at higher energies will decay more rapidly within the waveguide.

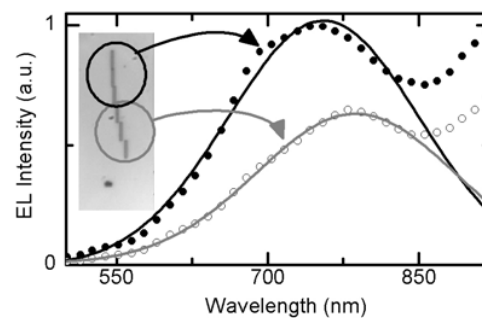


Figure 3. The overall statistics of the data suggest the spectral decay anticipated for SPPs propagating in a MIM waveguide. Here we have binned light from structures at ~1 μm and at ~5 μm from the isolation slit. Several spectra were averaged together to account for changes in the SPP illumination pattern from “hot spots”. The shoulder at long wavelengths is attributed to background Si band-edge emission. Drawn lines are guides to the eye.

IV. CONCLUSIONS

In summary, we have demonstrated that a silicon-based electrical source for SPPs can be fabricated at low temperatures using silicon nanocrystal doped alumina

within an MIM waveguide geometry. This device suggests a route forward towards high density, active plasmonic circuits that are integrated with silicon microelectronics.

V. ACKNOWLEDGEMENTS

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