A Silicon Die as a Frequency Source

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***Abstract*—A monolithic and unpackaged silicon die is presented as a frequency source suitable for quartz crystal resonator (XTAL) and oscillator (XO) replacement. The frequency source is referenced to a free-running, frequency-trimmed and temperature-compensated 3GHz RF *LC* oscillator. A programmable divider array enables the device to provide frequencies ranging from 6 to 133MHz. A post-processed Faraday shield contains fringing electromagnetic fields and enables the device to be delivered in unpackaged form such that it can be assembled into any package or via any assembly technique. The device dissipates approximately 2mA from a 1.8–3.3V power supply and drifts no more than ±300ppm over all operating conditions including a panel of industry-standard reliability tests.**

I. Introduction

Recently, silicon frequency control technologies have been developed into products targeted at replacing quartz crystal resonators (XTALs) and oscillators (XOs). These products include self-referenced RF CMOS oscillators [1]–[4] and synthesizers referenced to silicon microresonators fabricated via microelectromechanical systems (MEMS) technology, such as that presented in [5]. These new silicon frequency control devices have been introduced in packages that are pin-compatible with standard 5.0mm × 3.2mm XO packages as shown in Figure 1. However, it has been shown that the current performance of these silicon devices is inferior to that of quartz frequency control devices [1],[6],[7]. Thus, the advantage gained by selecting a silicon device versus a quartz device cannot be performance. Further, considering Figure 1 again, there is no obvious product differentiation when the various technologies are assembled into packages that are pin-compatible with quartz devices.

Consequently, a variety of concepts have been proposed in an effort to differentiate silicon frequency control devices from the entrenched quartz technology. These include reduced lead-time, smaller packages and lower cost than quartz devices. In fact, all of these concepts relate to cost as short lead-time addresses time-to-market and inventory management. Similarly, a myriad of small packages is already supported by the quartz industry [7]; thus silicon frequency control devices simply enable those same form-factors at lower cost.

Compounding the challenge for silicon devices further, the performance level currently achieved by these recently introduced devices limits them primarily to consumer electronics. In such applications, performance requirements are more relaxed than that which is achieved with standard quartz-referenced devices. For example, data interface protocols, such as HS/SS-USB, S-ATA, PCIe, and 10/100/1000 Ethernet, require the reference frequency source to maintain an accuracy of ±500/±300, ±350, ±300 and ±100ppm respectively. All of these, and related interfaces, also include noise performance requirements such as phase noise and timing jitter limits. Beyond these performance requirements, selection of frequency control devices in the consumer space tends to be driven by price. Thus, performance is a threshold and price is the criterion for device selection in these products. Considering this, frequency control devices in consumer applications are often lumped together with passive devices at very low average selling prices.

This work has been motivated by an effort to differentiate silicon frequency control technology from quartz devices. Thus, rather than develop the technology into packages that are pin-compatible with XOs, the authors have considered the

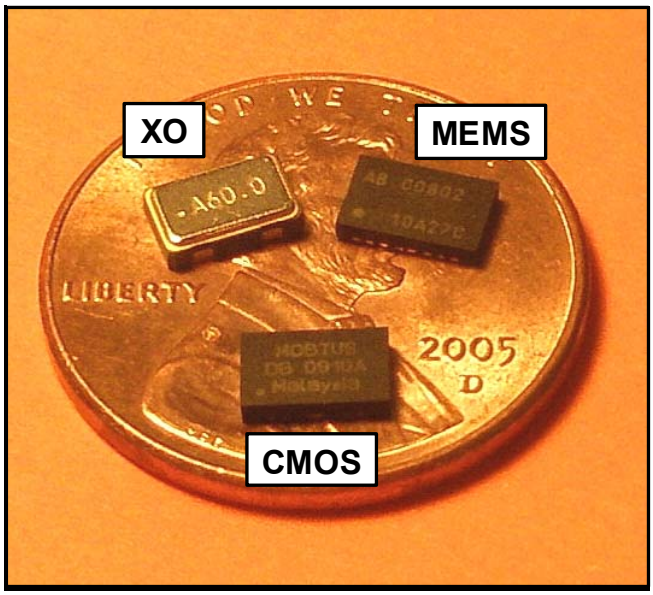

Figure 1. MEMS and CMOS oscillators compared to a typical XO. All devices are assembled in pin-compatible 5.0mm × 3.2mm packages.

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unique aspects of a silicon frequency reference. As opposed to silicon microresonators, self-referenced CMOS oscillators are uniquely positioned for silicon integration into any device as an intellectual property (IP) macro, just as the authors have presented in [2]. However, the development of such macros is often impractical due to added cost from increased silicon area and additional production test requirements for calibration of the frequency reference. Further, specific process options are required for implementation, many of which may not be available in the target device.

Addressing these challenges, in this work, a programmable and self-referenced unpackaged silicon die is presented as a new frequency source which can be integrated into nearly any package or via nearly any assembly technique. The die is fabricated in a standard 0.13µm RF CMOS process and measures 920µm × 880µm. A free-running, frequency-trimmed and temperature-compensated 3GHz *LC* oscillator (LCO) serves as the reference. A Faraday shield is post-processed over the die to contain fringing electromagnetic fields which, if perturbed by the package or external fields, would introduce frequency drift. Additionally, the back of the wafer is ground to yield a die height of either 200µm or 350µm at the edges and 250µm or 400µm in the center. This low profile and the Faraday shield enable the die to be assembled in a multichip module (MCM), with a chip-on-board (CoB) process or stacked into a multichip package (MCP). The resulting device does not require an external XTAL or frequency reference. Additionally, to the end-user, the product appears to contain IP though, in fact, the frequency generation function has been optimized with the appropriate process technology.

II. Self-Referenced CMOS Oscillators

A. Primary Frequency Drift Mechanisms

The natural resonant frequency, ω_o, of an LCO is given by $\omega_o = \sqrt{1/(LC)}$, where L is the net inductance and C is the net capacitance of the oscillator. In an integrated LCO, the resistive losses in the coil and the net tank capacitance are non-negligible. Thus, the zero-phase of the lossy network must be redetermined and it is given by,

$$\omega_1 = \omega_o \sqrt{\frac{CR_L^2 - L}{CR_C^2 - L}}. \quad (1)$$

In (1), R_L and R_C are real, resistive losses arising from the finite conductivity of the metal from which the components are constructed. Both exhibit temperature coefficients. Typically, R_L is much greater than R_C and (1) can be approximated by,

$$\omega_1(T) \approx \omega_o \sqrt{1 - CR_L^2(T)/L}. \quad (2)$$

$R_L(T)$ increases with temperature, thus the native temperature coefficient of frequency (TC_f) is negative, concave-down and dominated by the loss in the coil.

In [1]–[4], a myriad of higher-order effects which contribute to frequency drift have been presented. Additionally, several techniques have been introduced including frequency trimming due to process variation and temperature compensation of the native LCO TC_f. Those efforts have focussed primarily on utilizing active compensation techniques with the penalty of increased power dissipation. For example, the device in [4] dissipated approximately 15mA. Additionally, the work in [3] provided the first reported data indicating that frequency drift can arise in silicon oscillators from stress on the die and fringing electromagnetic fields into the package molding compound, both of which are considered here.

B. Reference Oscillator Architecture

In this work, a new architecture for the LCO has been developed. First, the resonant frequency has been increased from 1GHz in [4] to 3GHz to increase the quality-factor of the inductor. Next, considering (1), a simple and elegant observation is that if a lossy capacitance is introduced into the tank, such that it matches the loss in the coil, the TC_f can be cancelled. Such an approach would enable the temperature coefficient to be compensated passively, thus minimizing power dissipation while reducing noise from what would otherwise be the active compensation circuitry.

Figure 2 presents a simplified schematic of the reference oscillator. The LCO includes a cross-coupled complementary

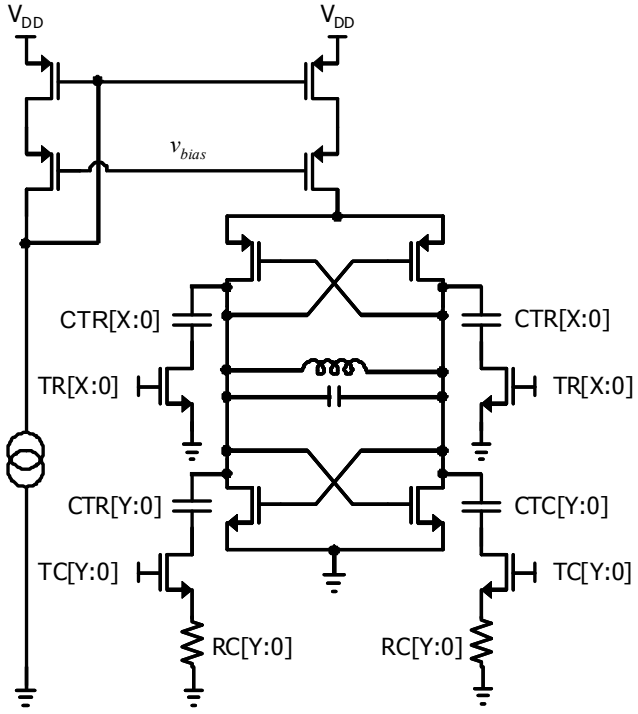

Figure 2. Simplified architecture of the reference oscillator illustrating the thin-film capacitor array for frequency trimming and the thin-film capacitor array with loss for passive temperature compensation.

negative transconductance amplifier with a pMOS bias to minimize flicker noise upconversion around the fundamental. Similar to the approaches shown in [1]–[4], an array of programmable thin-film capacitors (CTR[X:0]) serve to trim the frequency offset due to process variation through the corresponding switches, TR[X:0]. The remaining programmable array of thin-film capacitors (CTC[Y:0]) includes resistors (RC[Y:0]) in series with each capacitor such that a loss can be deliberately introduced into the capacitive network through switches TC[Y:0]. Selecting the appropriate resistor species is critical to minimizing nonlinearity in the TC_f as the TC in R_C will inevitably differ from the TC in R_L due to differences in material properties.

The system architecture includes a programmable integer divider array and nonvolatile memory (NVM) for storing trimming, compensation and configuration coefficients. Additionally, the oscillator core is buffered from the external power supply via a low drop-out regulator (LDO). Active power dissipation is approximately 2mA from an external power supply which can vary from 1.8–3.3V while the core operates at 1.2V. A programmable divider array enables the device to support frequencies from 6–133MHz with integer relationships to the reference.

III. Package-Induced Frequency Drift

A. Package-Induced Frequency Drift

The unpackaged self-referenced silicon die shown in Figure 3 is subject to several influences that give rise to frequency drift. For example, incident electromagnetic radiation can pull the self-resonant frequency. Light can introduce an undesired offset in the bias circuitry due to photo-current. Additionally, fringing magnetic (*B*) fields from the coil and electric (*E*) fields from the net tank capacitance exist as illustrated in Figure 4(a). The fields can be perturbed via several mechanisms. For example, the fringing *B*-field can be modulated by placing metal over the field. In such a case, an eddy current sets up in the metal to terminate the *B*-field while reducing the net tank inductance and causing a positive frequency shift. Similarly, the *E*-field constitutes a stray capacitance into free-space and can be modulated by any material placed over the die, including (most obviously), the molding compound of the package, as well as any changes in that material. For example, it was reported in [3] that when a free-running silicon oscillator is packaged in plastic and exposed to high relative humidity and pressure, the frequency drifts.

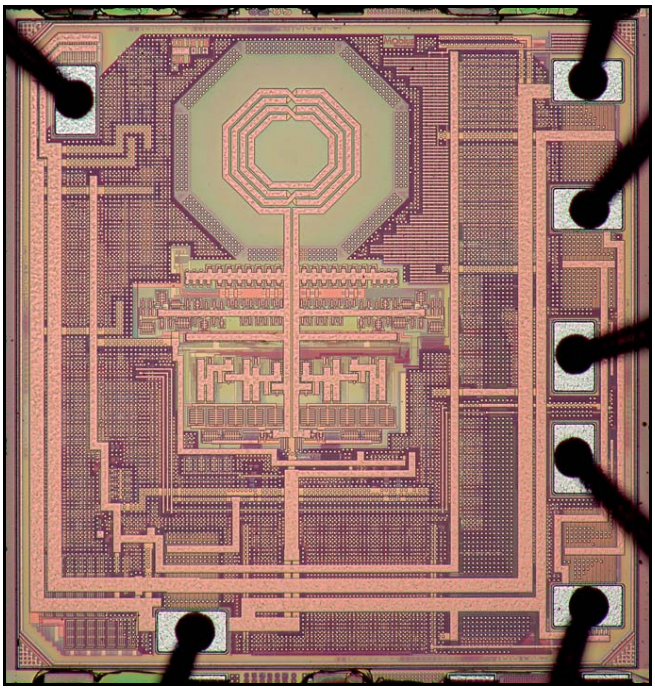

Figure 3. Die micrograph of the self-referenced silicon frequency source in a 0.13um RF CMOS process technology.

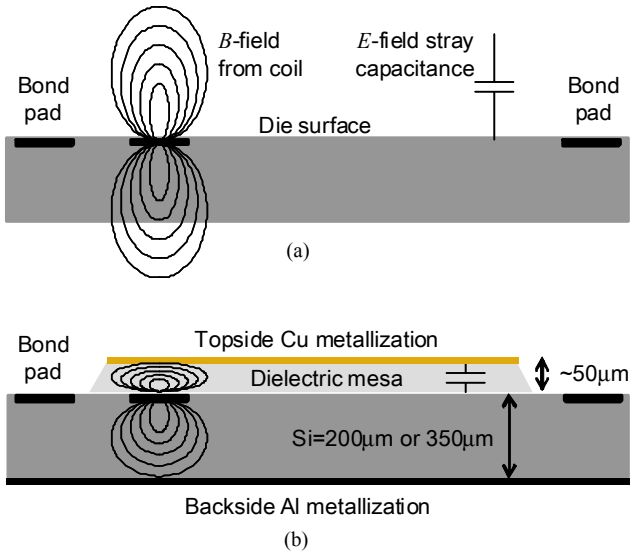

Figure 4. (a) An illustration of the uncontained fringing magnetic (*B*) and electrical (*E*) fields. (b) The same electromagnetic fields contained by the wafer-scale post-process for the Faraday shield.

B. A Wafer-Scale Post-Processed Faraday Shield

A low-cost, wafer-scale post-process has been developed to serve as a stress buffer between the top of the die and the package. Additionally, the shield contains and terminates the fringing electromagnetic fields, thus enabling the silicon die to be tested at wafer and packaged with nearly any assembly technique. As illustrated in Figure 4(b), the process includes a thick dielectric mesa which is deposited using a photo-patternable spin-on material. This dielectric layer must be deposited with the maximum possible thickness to avoid reducing the quality factor of the inductor and inducing frequency drift via eddy currents. The top of the dielectric mesa is electroplated with several microns of Cu, which is sufficiently thick to contain the fringing *B*-field at 3GHz. Similarly, the backside is

Figure 5. Scanning electron micrograph of the silicon frequency source die from Figure 3 including the wafer-scale post-processed Faraday shield illustrated in Figure 4. The die was mounted atop another die and wire-bonded in a ceramic package for initial characterization.

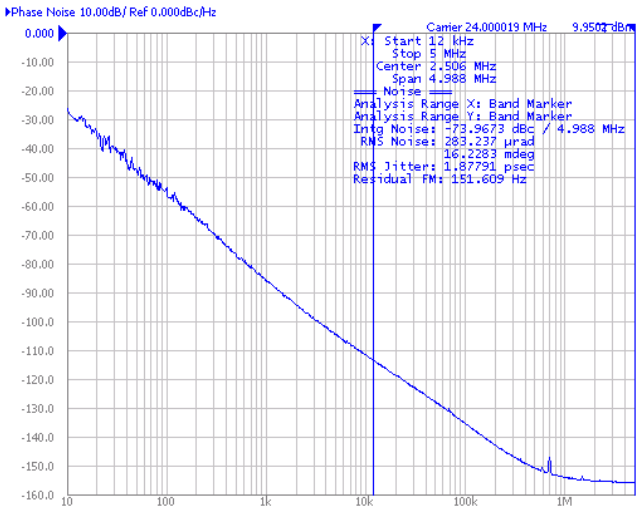

Figure 6. Measured SSB phase noise PSD from 10Hz to 5MHz for the silicon frequency source configured to 24MHz. The integrated phase jitter from 12kHz to 5MHz is less than $2ps_{RMS}$. The far-from-carrier phase noise is less than -155dBc/Hz.

metallized with several microns of Al. A scanning electron micrograph of the post-processed device is shown in Figure 5.

IV. Performance

The device shown in Figure 5 has been fully characterized and is currently in volume production. Here, only noise and frequency stability results are reported as these are the two key performance metrics which determine the applications that the device can serve.

Though the dielectric mesa is thick, there was concern that the Faraday shield might adversely affect the phase noise performance of the reference oscillator by reducing the quality-factor of the coil. Measured results of the single-sideband (SSB) phase noise power spectral density (PSD) for a device configured to 24MHz are shown in Figure 6. The noise floor is below -155dBc/Hz. The integrated phase jitter from 12kHz to 5MHz is less than $2ps_{RMS}$, using a brick-wall filter. No significant spurs were observed in the spectrum. Additionally, despite the low quality-factor of the reference oscillator, the phase noise is better than -25dBc/Hz even at 10Hz offset from carrier. Overall, the phase noise performance is superior to that reported previously in [1]–[4] while power dissipation has been reduced to approximately 2mA, primarily due to the passive temperature compensation technique introduced previously.

Production devices are tested, trimmed and configured at the wafer-level with production test hardware and a proprietary test algorithm. Thirty-two devices were selected at random and frequency stability was measured against temperature. Results are shown in Figure 7 where the TC_f for all devices is better than ±80ppm over the commercial temperature range of 0-70°C. Despite these results, TC_f is only one component of the total frequency drift. Devices were tested over voltage, temperature (0-70°C), for thermal hysteresis, wander, 1000hr. HTOL, 96hr. unbiased HAST and three passes through the JEDEC standard solder reflow profile. Each of these stress tests is independent and includes a mean offset and a standard deviation (σ). Thus, the net 3σ frequency error can be computed by adding all offsets and computing the root of the sum of each variance. Results are summarized in the Table I on the following page.

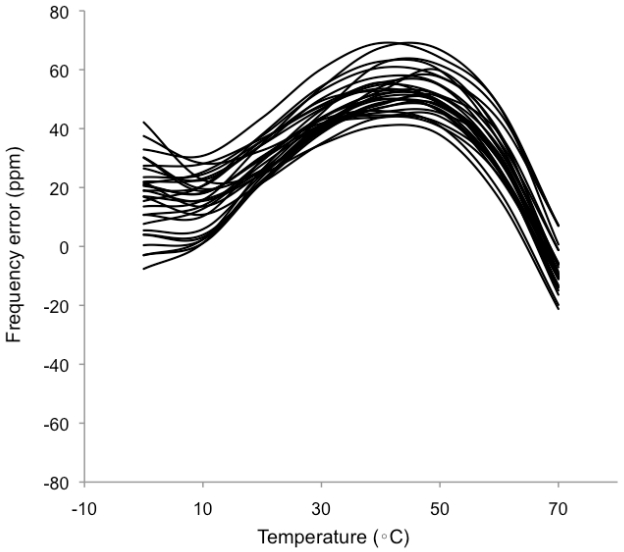

Figure 7. Measured TC_f for 32 randomly selected devices which were tested, trimmed and configured with production test equipment and the production test algorithm.

TABLE I. TOTAL FREQUENCY STABILITY

Test	Method/Conditions	μ	σ
Temperature	0-70°C	30	42
VDD	3.0-3.6	-2	2
Wander	260 readings at 80, 50, 30 10, -10 (1300 total)	0	1
Pre. vs. post 1000hr. HTOL	125C operating life test JEDEC 22-A 108-B	1	11
Pre. vs. post unbiased HAST	JEDEC EIA/JESD22-A118 96hrs	68	23
Pre. vs. post 3x solder reflow	260°C profile	24	7
Thermal hysteresis	Soak at each point, in 10°C increments, measure frequency from 100°C to -30°C back to 100°C	0	15
Total		121	52

Table I shows that the 3σ frequency stability of the device is ±277ppm (121ppm + 3 × 52ppm), which has been rounded to the aforementioned specification of ±300ppm. This frequency stability can be achieved in any JEDEC moisture-sensitivity level one (MSL1) plastic package over all conditions. Process, voltage and temperature frequency stability are determined by the silicon design while frequency drift due to the remaining stress tests is due to the package, which is constructed of epoxy molding compound. Interestingly, the stress test with the largest offset and the second largest standard deviation is HAST. It has not escaped the attention of the authors that if frequency drift due to HAST were eliminated, the total frequency stability would improve dramatically and approach ±100ppm. Nevertheless, these drift mechanisms reported here are generally not observed by the end-user as the *in situ* environment required to cause such drift is hostile and unlikely to be a represent any reasonable operating condition. Nevertheless, and unlike much related work in this area, the authors have elected to measure and report all of the measured statistics for all of the possible frequency drift mechanisms in the developed technology.

V. APPLICATIONS

±300ppm frequency stability meets the technical requirements for many common wireline interfaces found in consumer electronics including HS/SS-USB, PCIe and S-ATA. Many of these applications are currently in production at very high volume. For example, USB ports exceed over one billion units annually. In these applications, there typically exists a controller that contains a sustaining circuit to support an external XTAL resonator. Rarely are active XOs utilized in such systems due to cost-constraints. These passive resonators can be surface mount devices (SMD) or packaged in metal cans. The former enables platforms to be assembled with standard solder reflow equipment while the latter requires manual assembly. Additionally, SMD XTALs are much lower-profile than metal can XTALs. Considering these factors, SMD XTALs are often selected for low-profile consumer devices such as USB flash drives (UFD), USB flash card readers (UFCR) and solid-state drives (SSD). However, the price point of SMD XTALs is significantly higher than that of metal can XTALs.

The cost structure of the silicon die frequency source is such that it can compete with typical prices for SMD XTALs, even at very high volumes. Additionally, the silicon die offers the opportunity to differentiate end-products. For example, the 200μm-thick silicon die can be assembled into an MCP as shown in Figure 8, where a standard quad-flat package (QFP) has been dissolved. The die on the bottom of the stack is the wireline controller while the die on the top of the stack is a previous version of the silicon frequency source first presented in [4]. The process of dissolving the package has also dissolved the Faraday shield. The silicon die frequency source has been mounted with standard die-attach material and wire-bonded to the lead-frame such that it can be powered and drive the output clock signal onto the XTAL input (XIN) pin on the controller.

MCP assembly enables the controller to appear as though the it contains silicon IP such that an external XTAL is not required. However, the silicon die is a far superior embodiment than IP. First, there is no additional non-recurring engineering, capital investment in a new mask set or risk associated with IP integration. The die can be assembled into

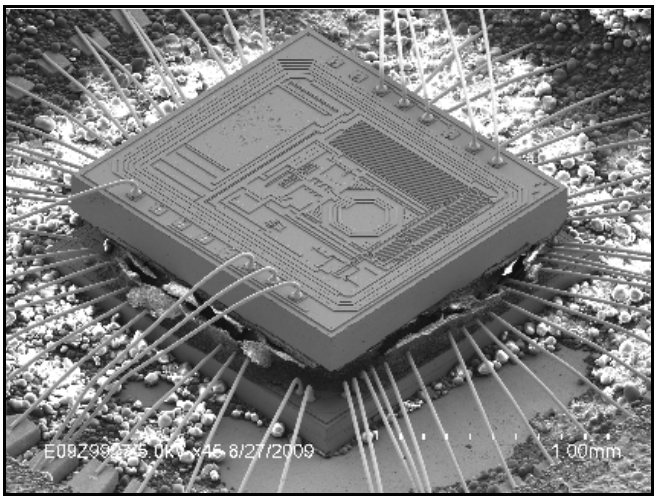

Figure 8. Scanning electron micrograph of the 200μm-thick silicon die frequency source stacked in a dissolved QFP MCP on top of a wireline controller. The die shown here was first presented in [4]. The Faraday shield has been dissolved along with the package.

the MCP immediately. Next, complicated analog test is captured at the wafer-level and only a simple, low-cost final post-assembly trim is required. Last, no silicon area, or associated cost, is sacrificed on the controller, which is likely fabricated in a deeper submicron technology node than the frequency source. In the end, the device "appears" similar to a passive XTAL which is simply wire-bonded inside the package.

Consistent with that, products where CoB assembly is common are another application for the silicon die frequency source. Figure 9 presents a dissolved USB drive-in-package (UDP) including the 350µm-thick device. In this application, there are no packaged components. The controller, memory and the silicon frequency source are assembled on a substrate as bare die and wire-bonded as shown. Passives are populated and the device is reflowed. Then epoxy molding compound is injection-molded over the entire substrate so as to protect the silicon content. Of course, XTAL resonators can, and are, used in applications such as this, but the silicon die frequency source enables lower cost and the smallest possible form-factor while maintaining consistency with the assembly process for the remaining silicon content in the product. Additionally, the 350µm-thick die does not require post-assembly test or frequency-trimming. That is because the final trim can be performed at the wafer-level when the wafer is 350µm thick. The 200µm-thick device requires a frequency offset to be estimated at the wafer-level because it warps after post-processing and further test cannot be conducted. Thus, the final trim must be performed in the package. The authors are developing techniques to manage the wafer warpage and ultimately execute final test on 200µm, and potentially thinner, wafers.

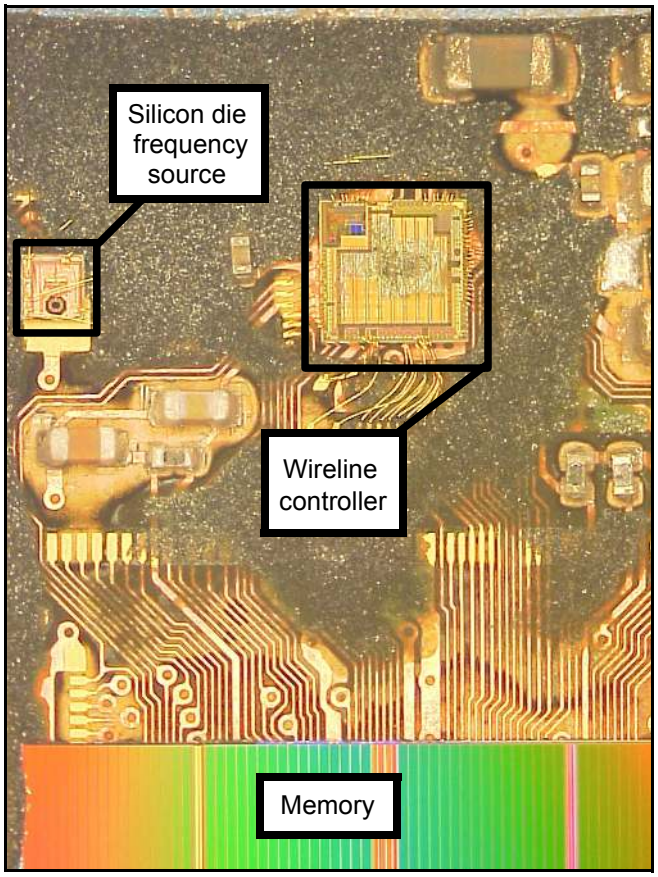

Figure 9. The silicon frequency source assembled via a CoB process in a USB drive-in-package (UDP). The Faraday shield has been dissolved with the package. Post-assembly test is not required because the die is 350µm thick.

VI. Conclusions

It was shown that silicon frequency control devices that are pin-compatible with quartz devices possess little differentiation. Addressing that, an unpackaged silicon die was introduced as a new frequency source. A frequency-trimmed and temperature-compensated 3GHz LCO serves as the frequency reference. In contrast to previous work by the authors, a new passive temperature-compensation technique was demonstrated where a lossy capacitance was deliberately introduced into the LCO to cancel the loss in the coil. It was shown that this technique enables the device to operate with a bias current of approximately 2mA. Further, the effects of fringing electromagnetic fields from the die were discussed. A wafer-scale post-processed Faraday shield was introduced to contain and terminate these fields while not degrading performance. It was shown that with this process, this silicon die frequency source can replace passive XTAL resonators in many applications. Both MCP and CoB assembly of the silicon die were presented. The authors intend to expand this work and introduce devices with significantly higher frequency accuracy and lower noise in the future.

VII. Acknowledgement

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