1500 K/ps. We performed the simulations on a massively parallel computer (*29*), using a time step of 0.7 fs, for a total time of ~30 ps.
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A Silicon Single-Electron Transistor Memory Operating at Room Temperature

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A single-electron memory, in which a bit of information is stored by one electron, is demonstrated at room temperature. The memory is a floating gate metal-oxide-semiconductor transistor in silicon with a channel width (~10 nanometers) smaller than the Debye screening length of a single electron and a nanoscale polysilicon dot (~7 nanometers by 7 nanometers) as the floating gate embedded between the channel and the control gate. Storing one electron on the floating gate screens the entire channel from the potential on the control gate and leads to (i) a discrete shift in the threshold voltage, (ii) a staircase relation between the charging voltage and the shift, and (iii) a self-limiting charging process. The structure and fabrication of the memory should be compatible with future ultralarge-scale integrated circuits.

To increase the storage density of semiconductor memories, the size of each memory cell must be reduced. A smaller memory cell also leads to faster speeds and lower power consumption. One of the widely used nonvolatile semiconductor memories is the metal-oxide-semiconductor (MOS) transistor that has a floating gate between the channel and the control gate. Information is represented by storing charges on the floating gate. The information can be read by using the transistor because different amounts of charge on the floating gate shift the threshold voltage of the transistor differently. The ultimate limit in scaling down the floating gate memory is to use one electron to represent a bit, the so-called single electron MOS memory (SEMM). To make such memory practical requires a proper design of device structure, so that the voltage for charging a single electron is discrete and well separated (as compared to the noise level), as is the shift in threshold voltage caused by the storage of a single electron.

One of the two previous approaches to SEMM is to build the device in a tiny polysilicon strip (*1*). An electron percolation path in the strip forms the channel, and one of polysilicon grains near the conduction path acts as the floating gate. Such a structure intrinsically prevents precise control of the channel size, floating gate dimension, and tunnel barrier. The other approach is to replace the floating gate of conventional floating gate transistor memory with nanocrystal grains, while keeping the rest of the device unaltered (*2*). The size of the silicon nanocrystals and the tunnel barriers intrinsically have a broad distribution. Both approaches intend to alleviate the challenges in nanofabrication, but the statistical variations in their structures lead to large fluctuations in the shift of the threshold voltage and in the charging voltage, making them unsuitable for large-scale integration.

Here we present a SEMM in crystalline silicon that has a well-controlled dimension. Charging a single electron to the floating gate leads, at room temperature, to a quantized shift in threshold voltage and a staircase relation between the shift and the charging voltage. Furthermore, the charging process is self-limited.

There are two key features of our SEMM (Fig. 1): (i) the channel width of silicon MOS field-effect transistor is narrower than the Debye screening length of a single electron and (ii) the floating gate is a nanoscale square (hence, it is called a dot) (*3*). Otherwise, the device is similar to an ordinary floating gate MOS memory. The narrow channel ensures that the storage of a single electron on the floating gate is sufficient to screen the entire channel (that is, the full channel width) from the potential on the control gate, which leads to a significant shift in threshold voltage. A small floating gate is used to significantly increase electron quantum energy (due to the small size) and electron charging energy (due to the small capacitance); hence, the threshold voltage shift and the charging voltage become discrete and well separated at room temperature. The control gate in our device is long, but the device's threshold is determined by the section where the floating gate is located.

In fabrication, an 11-nm-thick polysilicon film (for the floating gate) was deposited on a silicon-on-insulator wafer that had a 35-nm-thick top layer of crystalline silicon (for the channel). The polysilicon film and the silicon layer were separated by a layer of native oxide ~1 nm thick. The first level of electron beam lithography (EBL) and reactive ion etching (RIE) patterned the width of the floating gate and the narrow silicon channel, which is under the gate (that is, they are self-aligned). The initial channel width varied from 25 to 120 nm. A second level of EBL and RIE patterned the length of the floating gate, making it square (Fig. 2). An 18-nm-thick layer of oxide was then thermally grown, partially consuming the silicon, which reduced the thickness of the polysilicon dot by ~9 nm and the lateral size of the dot and the width of the silicon channel by ~18 nm. A 22-nm-thick layer of oxide was deposited by plasma-enhanced chemical vapor deposition, making the total thickness of the control gate oxide 40 nm. Next, polysilicon was deposited, and the control gate was patterned to a length of 3 μm, which covered the floating gate and part of the narrow channel.

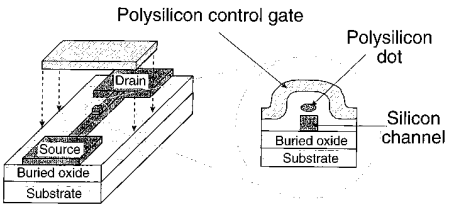

Fig. 1. Schematic of a SEMM that has a narrow silicon channel and a nanoscale polysilicon dot as the floating gate. The cross-sectional view details the floating gate and the channel region.

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After making the final contacts, the devices were sintered in a forming gas to reduce the interface states. Many of the fabrications described here are similar to our previous work (*4*).

No tunnel oxide was intentionally grown between the channel and polysilicon floating gate. The reasons are twofold: to allow fast charging and to minimize the potential difference between the channel and the floating dot during the charging process, so that for a given charging voltage, the Coulomb blockade effect can regulate the number of electrons stored on the floating gate. In these devices, a potential barrier still exists between the channel and the floating gate, because of the grain boundary in polysilicon and the thin native oxide.

The devices were characterized at room temperature in a two-step process. First, a voltage pulse that was positive relative to the grounded source was applied to the control gate, while the drain voltage was maintained at 50 mV. This process caused electrons to tunnel from the channel to the floating gate. The drain current of the transistor was then measured as a function of the gate voltage (*I-V*) with a 50-mV source drain voltage, from which the threshold voltage (V_{th}) shift was obtained. A simple switching circuit was used to allow measurement of the *I-V* characteristics within 1 s after the completion of the charging process.

A SEMM that had an ~10-nm-wide channel and an ~7 nm by 7 nm square, 2-nm-thick floating gate—the smallest in our fabrication—was characterized under different charging voltages. The device dimension was estimated from measurements made with a scanning electron microscope and from the oxidation rate. However, self-limiting oxidation may have occurred (*5*), making it difficult to assess the exact size. We measured the *I-V* characteristics of the device after the control gate was pulsed by charging voltages ranging from 0 to 14 V (Fig. 3). Although the charging voltage was continuous, the threshold voltage of the device (defined as the gate voltage at which the drain current reaches 100 pA) always made a discrete shift of 55 mV, and each shift corresponded to a charging voltage interval of ~4 V (Fig. 4A). Moreover, for a given charging voltage, the threshold shift was self-limited; that is, the shift in threshold voltage was independent of the charging time (Fig. 4B). Because no tunnel oxide was intentionally added, the charge stored at the floating gate could be held for ~5 s after the control gate potential was set back to the ground, and the threshold voltage of the device returned to its original value (leftmost trace in Fig. 3).

The behavior of the device can be explained by the single electron charging effect. Because the tunnel oxide between the channel and the floating gate was thin, the charging voltage dropped primarily between the control gate and the floating gate. To add one electron to the floating gate requires an increment of e/C_{dg} in charging voltage to be applied to the control gate, where e is the magnitude of a single electron charge and C_{dg} is the capacitance between the control gate and the floating gate (Fig. 5). The capacitance C_{dg} for the 7 nm by 7 nm floating gate and a 40-nm-thick layer of control oxide was about 4.4×10^{-20} F, giving a single electron charging voltage of 3.6 V, close to the experimental value of 4 V.

The shift in the SEMM's threshold voltage caused by one electron stored in the floating gate is given by

$$\Delta V_{th} \approx e/(C_{dg} + C_{frg}) \quad (1)$$

Here C_{frg}, the fringe capacitance, accounts for the partial wrapping of the control gate around the channel so that the channel is only partially screened by the floating gate. For a conventional floating gate MOS memory, $C_{frg} = 0$, and ΔV_{th} is reduced to the usual form $\Delta V_{th} \approx e/C_{dg}$. In our devices, C_{frg} is about two orders of magnitude greater than C_{dg}. The value of C_{frg} can be estimated from the single electron Debye screen length (~70 nm) and the channel thickness (26 nm) in a parallel-capacitor model. For the control oxide thickness of 40 nm and the area of 70 nm by 26 nm, the C_{frg} is about 2.5×10^{-18} F, and hence, $\Delta V_{th} \approx 64$ mV, which is again consistent with the experiment.

The self-limiting charging process can be explained by three facts: (i) The energy level spacing in the floating gate, which must be overcome to charge one more electron into the floating gate, is large compared with k_BT (the thermal energy, Boltzmann's constant k_B times temperature T) at room temperature. For a 7 nm by 7 nm silicon square embedded in SiO_2, the quantum energy spacing is ~30 meV, and the

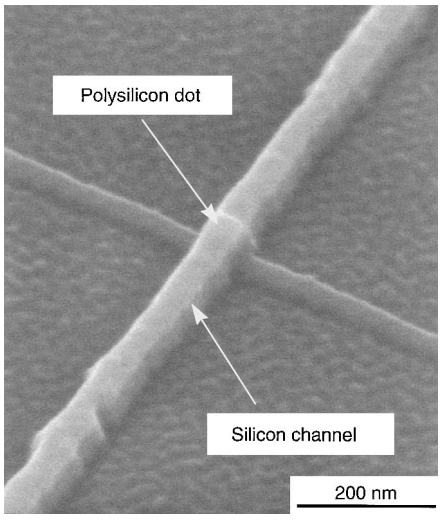

Fig. 2. Scanning electron micrograph of the narrow silicon channel with the polysilicon dot on top, before size reduction by thermal oxidation. The width of the channel and the size of the dot are both 50 nm. The lines in the buried oxide, included for easy alignment, come from the second-level EBL and have no effect on device behavior.

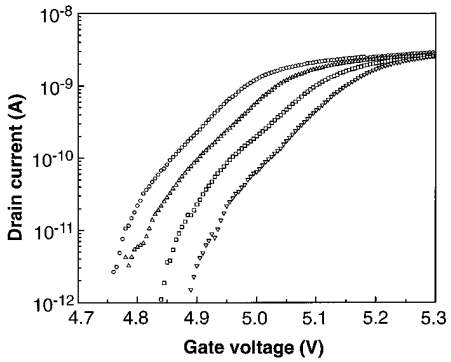

Fig. 3. The *I-V* characteristics of a SEMM device before and after the charges were stored in the floating dot. For charging voltage pulses from 0 to 14 V, the shift in threshold voltage was quantized with an increment of ~55 mV. The leftmost trace (0 2-V charging voltage) represents the case where no charge was being stored in the dot, and the other three traces show the results after positive gate pulses had been applied with progressively larger magnitude (from left to right: 7, 10, and 14 V). Data recorded at room temperature; drain-source voltage, 50 mV.

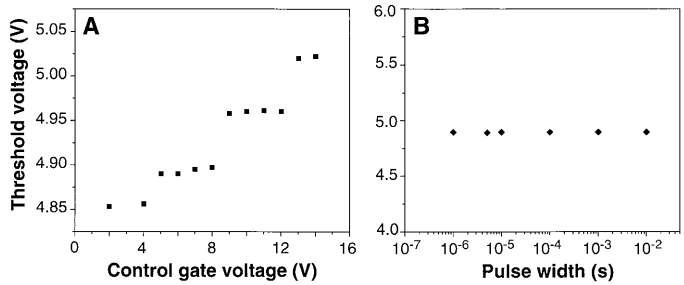

Fig. 4. Threshold voltage of the SEMM as a function of (**A**) the charging voltage on the control gate (voltage pulses of 10 ms), showing a staircase relation with an interval of ~4 V, and (**B**) the charging time while the charging voltage pulse is fixed at 10 V, indicating a self-limited process.

Coulomb energy spacing is 50 meV (assuming that the oxide layer between the dot and channel is 1 nm thick) (6); (ii) because the barrier layer is thin, the voltage drop between the channel and the floating gate is very small; and (iii) once an electron is added to the floating gate, the potential of the floating gate rises, further reducing the voltage difference between the channel and the floating gate and preventing another electron from tunneling into the floating gate. Therefore, for a fixed charging voltage, the charging process is self-regulated and stops once the floating gate is charged with a fixed number of electrons, leading to a threshold shift independent of charging time and a staircase relation between the charging voltage and the threshold shift.

The discrete threshold shift is not a result of interfacial traps. The threshold shifts due to the traps will not be equally spaced (because the charge will be trapped at different locations of the channel), and the charging process will be time dependent (*7*).

Despite the small floating gate and the low level of channel doping, the device has a good subthreshold slope of 108 mV per decade, because the inversion layer induced by the control gate effectively acts as an ultrashallow source and drain for the device. This characteristic is also attributable to the low source and drain voltage.

As indicated by Eq. 1, the threshold voltage can be much larger than the present 55 mV if the thickness of the control gate oxide is increased or the fringing gate capacitance can be reduced. Also, if a thicker tunnel oxide is used between the channel and the floating gate, the charge on the floating gate can be held much longer than the current 5 s.

The SEMM should be investigated more thoroughly before being put into manufacturing. One of the most important questions to be studied is the effects of variations of device size and stray charges on the threshold voltage. Nevertheless, the SEMM presented here is orders of magnitude smaller than the conventional floating gate MOS memory, has properties that conventional memories do not have, and is a major step forward in taking advantage of single electron effects to build ultrasmall and ultrahigh density transistor memories.

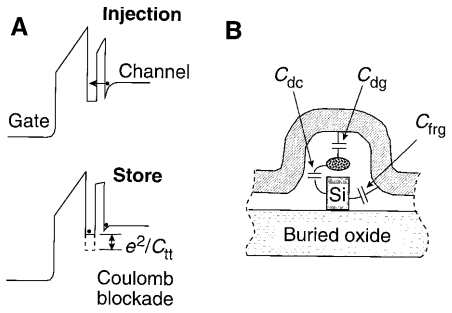

Fig. 5. (**A**) Schematic band diagram before and after injection of an electron into the dot. A single electron stored in the dot can raise its potential by e^2/C_{tt}, blocking the entry of other electrons from the channel (C_{tt} is the total capacitance of the floating gate). (**B**) Schematic cross section of the device showing the capacitive coupling between various elements.

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Micropatterning Fluid Lipid Bilayers on Solid Supports

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Lithographically patterned grids of photoresist, aluminum oxide, or gold on oxidized silicon substrates were used to partition supported lipid bilayers into micrometer-scale arrays of isolated fluid membrane corrals. Fluorescently labeled lipids were observed to diffuse freely within each membrane corral but were confined by the micropatterned barriers. The concentrations of fluorescent probe molecules in individual corrals were altered by selective photobleaching to create arrays of fluid membrane patches with differing compositions. Application of an electric field parallel to the surface induced steady-state concentration gradients of charged membrane components in the corrals. In addition to producing patches of membrane with continuously varying composition, these gradients provide an intrinsically parallel means of acquiring information about molecular properties such as the diffusion coefficient in individual corrals.

The patterning of surfaces into defined regions of contrasting properties has recently received considerable attention. Successes in this field include the development of micrometer-scale patterns in surface wettability (*1*) and microcontact printing, which has produced patterned self-assembled monolayers with submicrometer features (*2*, *3*). At the same time, light-directed synthesis has been used to generate spatially addressable combinatorial libraries of DNA and protein sequences on solid substrates (*4*). Here, we describe patterning of surfaces with properties resembling those of living cells: fluid bilayer membranes on solid supports. This work has been stimulated by the desire to create integrated devices capable of manipulating molecules in a bilayer membrane and to pattern spatially addressable libraries of chemically distinct, fluid membrane patches.

Supported membranes are self-assembling, two-dimensional (2D) fluid systems (Fig. 1). The bilayer membrane consists of two opposed leaflets of phospholipid molecules and is the basic structure central to all living cell membranes. Bilayers on solid supports were originally developed for studies of interactions between living cells, where they have proven highly useful (*5*, *6*). Supported membranes can be formed by spontaneous fusion of lipid bilayer vesicles with an appropriate hydrophilic surface such as oxidized Si (*7*, *8*). Interactions between membranes and surfaces involve electrostatic and hydration forces as well as attractive contributions from long-range van der Waals forces. An energetic minimum tightly traps the membrane near the surface. Supported bilayers are typically separated from the solid substrate by a thin (~10 Å) film of water (*9*–*11*) and retain many of the properties of free membranes, including lateral fluidity. The fluidity is long range, with mobile components of both leaflets of the bilayer freely diffusing over the entire surface of the substrate.

The lateral fluidity of supported membranes is a key feature that distinguishes them from other surfaces. Although fluidity provides the membrane with a variety of unique properties, it presents an intrinsic difficulty in that membrane components are continually

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