A Simple Accurate Bridge-Transducer Interface with Continuous Autocalibration

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***Abstract*—This paper presents a one-chip simple and accurate transducer interface for resistive bridges. A key part of this interface is formed by a novel dynamic voltage divider. In this divider the bridge supply voltage is measured for reference purposes in small parts (piece-wise measurement) which are within the range of the bridge output voltage. The use of an autocalibration technique, the three-signal method, eliminates influence of linear parameters and errors. Moreover, the effects of the nonidealities of the applied switches are also eliminated. The circuit has been realized in a 3 μm BiCMOS process and shows an uncertainty of only 10 μV for a bridge supply voltage of 5 V.**

***Index Terms*—Bridge circuits, calibration, intelligent sensors, resistance measurement, sensor interface, transducers.**

I. Introduction

RESISTIVE-BRIDGE transducers are used for the measurement of a large variety of physical signals, such as pressure, force, displacement, etc. Because of the elimination of common-mode effects, the accuracy of bridge transducers can be rather high, in the order of 10^{-4} to 10^{-6}. A resistive bridge transducer is often applied in a ratiometric mode, where the ratio of the output voltage $V_{\rm out}$ and the bridge supply voltage VBS represents the physical signal. These voltages both have to be measured. Recently, some interesting new circuits have been described. In the circuit given by Kerth *et al*. [1], two third-order delta-sigma converters are used to process these voltages. Huijsing *et al*. [2] realized several types of two-wire bridge-to-frequency converters and Lehman *et al*. [3] implemented ac excitation followed by oversampling. The circuit presented in this paper combines the advantages of the earlier circuits with some new ideas. The result is that no accurate external reference or bridge supply voltage is required. Also, the accuracy of the gain of internal circuits is not based on matching of on-chip components, but on piece-wise measurements, resulting in a very accurate and long-term gain stability without calibration.

The voltages $V_{\rm out}$ and $V_{\rm BS}$ have to be measured to obtain the ratio $V_{\rm out}/V_{\rm BS}$. This ratio is a measure of the bridge imbalance. A direct measurement of $V_{\rm out}$ and $V_{\rm BS}$ using the same processing circuit would require a very large dynamic range of this circuit, because $V_{\rm BS} \gg V_{\rm out}$. Therefore, in many transducer interfaces, a voltage divider for $V_{\rm BS}$ or a voltage amplifier for $V_{\rm out}$ is used. A major drawback of these solutions is that the accuracy of such a divider or amplifier is limited by resistor matching and that, even after a calibration procedure, long-term drift and temperature dependence will cause inaccuracy. In [4], Klaassen proposed a method to increase the accuracy of voltage dividers by using the principle of dynamic element matching (DEM). The accuracy of the type of divider presented is limited by the mismatch of the switch ON resistance. This problem can be solved by using piece-wise measurements [5].

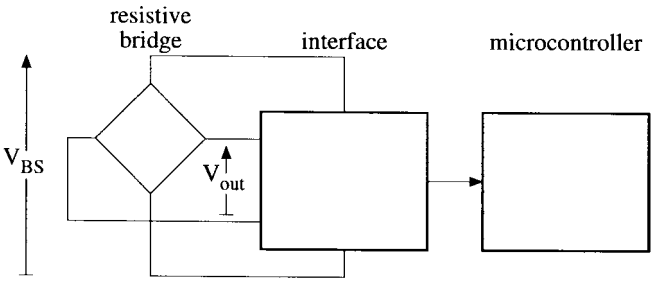

Fig. 1. System setup of the bridge-readout circuit.

In this paper, we introduce a novel bridge interface in which an improved version of this measurement method has been applied. The improved method requires much fewer switches and wires than the older one.

It will be shown that the effect of many of the nonidealities, such as transients, switch-feedthrough, offset, etc., are eliminated by the continuously applied autocalibration technique: the three-signal technique [5]–[7]. The output circuitry of the interface includes a modulator that generates a period-modulated output signal, which can be read out directly by the microcontroller (Fig. 1). Full advantage is taken of the memory and processing facilities of the microcontroller.

The design objectives for the transducer interface are:

- Self-calibrating interface circuit with an absolute accuracy of better than 0.1% (10 bits) for ratiometric measurements over a large temperature range.
- Resolution of 14 bits.
- Processing time of less than 0.1 s.
- Single-chip implementation.

II. Principles of Operation

To make the circuit immune to temperature changes, drift, and resistor mismatch, an auto-calibration (three-signal technique) is used [3]–[5]. In addition to the measurement of the unknown signal E_x, two reference signals E_1 and E_2 are measured in an identical way, where the reference signal E_1 is allowed to be zero or equal to $-E_2$. The final measurement

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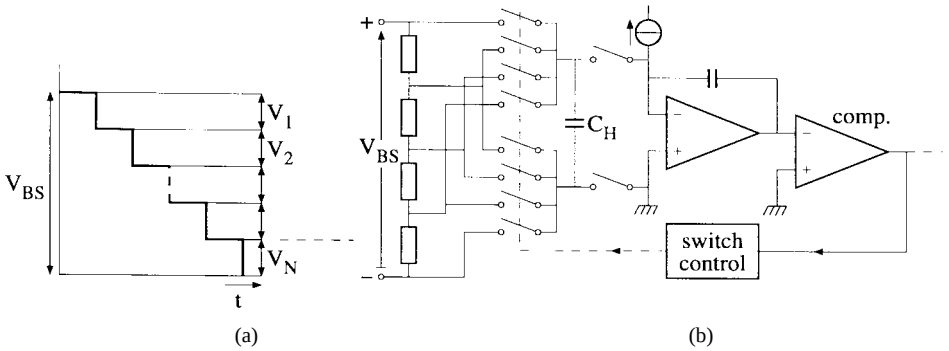

Fig. 2. Principles of piece-wise measurement. (a) A large output voltage $V_{\rm BS}$ is measured using (nonequidistant) samples $V_i (i = 1, 2, \cdots N)$. (b) A simple circuit with a 1:4 divider.

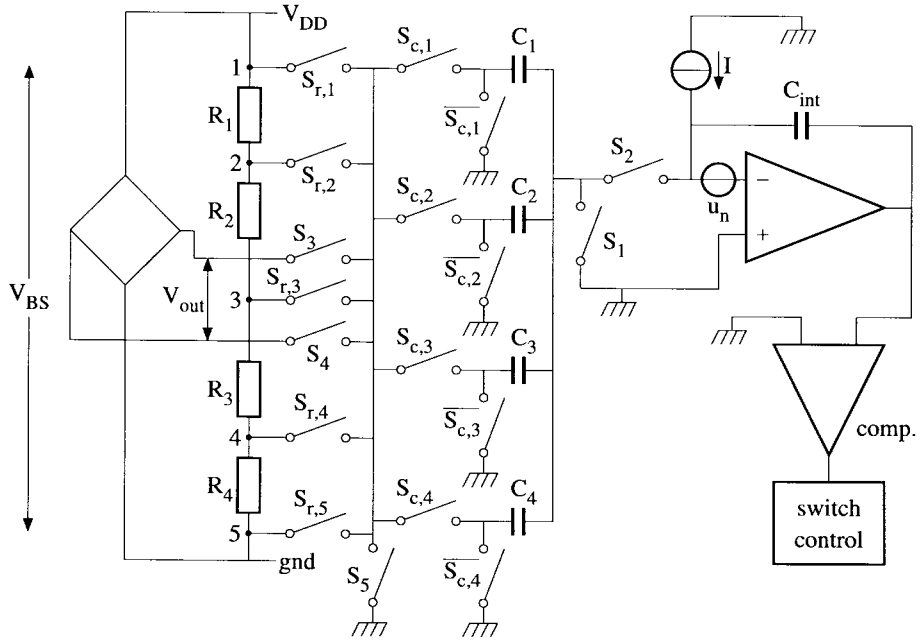

Fig. 3. The principle of the new circuit.

result is involved in the ratio M_3

$$M_3 = \frac{E_x - E_1}{E_2 - E_1}. \tag{1}$$

To enable easy processing by a microcontroller, the signals are converted to the time domain, using a signal-controlled oscillator. This oscillator generates a square-wave output voltage with a period T, which is related to the signal according to a set of first-order equations

$$T_i = aE_i + b, \qquad (i = x, 1, 2). \tag{2}$$

Substitution of (2) in (1) gives

$$M_3 = \frac{T_x - T_1}{T_2 - T_1}. \tag{3}$$

In (3), the unknown parameters a and b are eliminated. Therefore, drift and temperature dependence of the oscillator parameters do not affect the final result M_3, provided that changes during a single measurement (of about 0.1 s) can be neglected. For the application of the three-signal technique according to (2), it is required that the signal-controlled oscillator has a linear transfer characteristic. This demand is difficult to meet when the dynamic range of the signals is high. In our case, the bridge supply voltage $V_{\rm BS}$ is much larger than the output voltage $V_{\rm out}$. Direct processing of both voltages would require an extremely linear signal-controlled oscillator with ultra-low noise. To eliminate this problem, the larger voltage $V_{\rm BS}$ is measured in small pieces (samples), where each is within the range of the bridge output voltage $V_{\rm out}$ [Fig. 2(a)].

Fig. 2(b) shows a simple circuit [3] in which the parts of the voltage $V_{\rm BS}$ are sampled by the floating capacitor $C_{\rm H}$. The charge on $C_{\rm H}$ is transferred to the integrator and converted into the time domain.

A major drawback of the basic circuit shown in Fig. 2(a) is that for high values of the division ratio N switches and wires are required. Another serious drawback is related to the effect of voltage-dependent parasitic capacitors [not indicated in Fig. 2(b)], which are connected to the input components. These drawbacks are overcome in the new circuit presented here (Fig. 3).

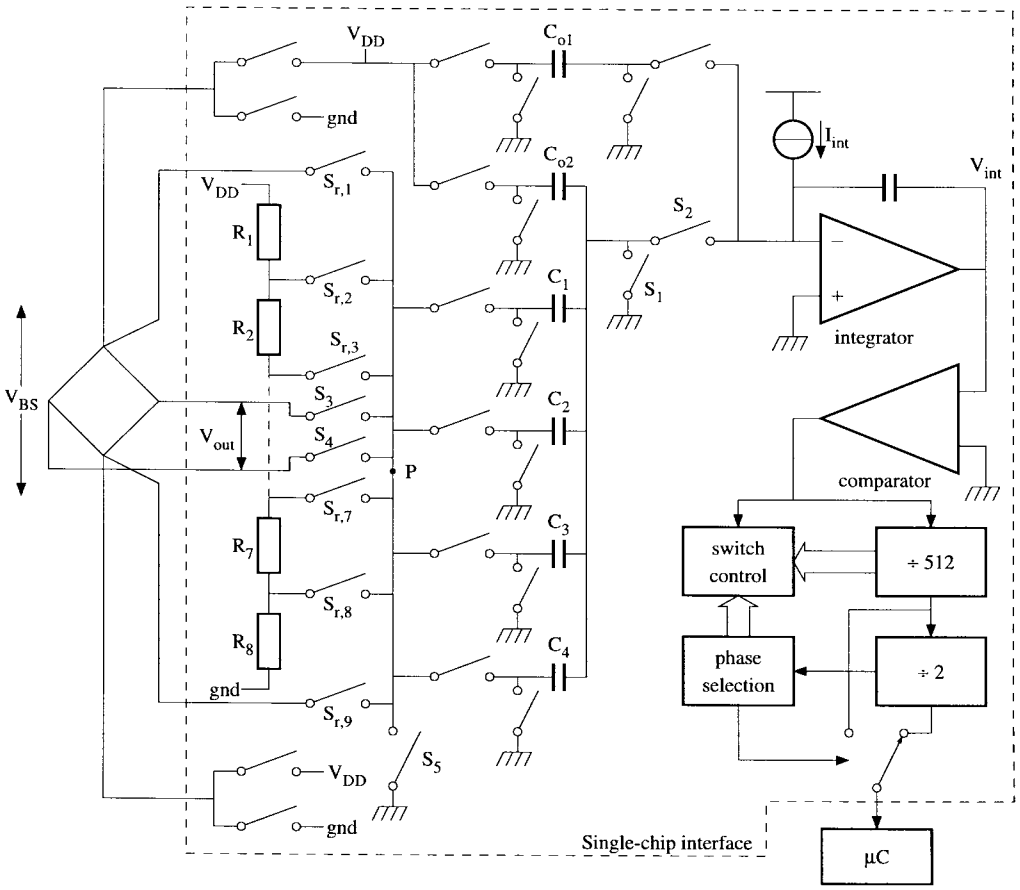

Fig. 4. The complete bridge interface.

The divider is realized with N_{R} resistors and N_{C} capacitors, resulting in a division ratio $N_{\mathrm{R}}N_{\mathrm{C}}$. The output of the divider is a charge which is transferred to the integrator and converted into a voltage.

A complete measurement consists of three measurement phases in which $V_{\mathrm{BS}}, V_{\mathrm{out}}$ and the offset voltage are measured respectively. During the start of the measurement of $\mathrm{V_{BS}}$ (switches $\mathrm{S_3}$, $\mathrm{S_4}$, and $\mathrm{S_5}$ are nonconducting and $\mathrm{S_{r,1}}, \cdots \mathrm{S_{r,5}}$ are sequentially conducting), one of the capacitors, for instance $\mathrm{C_1}$, is connected between node 1 of the voltage divider and ground ($\mathrm{S_1}$, $\mathrm{S_{r,1}}$ and $\mathrm{S_{c,1}}$ conducting). Next, $\mathrm{S_1}$ and $\mathrm{S_{r,1}}$ are opened and $\mathrm{S_2}$ and $\mathrm{S_{r,2}}$ closed (in this paper a closed switch is considered to be conductive, an open switch is nonconductive). As a consequence, a charge $\mathrm{C_1(V_1 - V_2)}$ is transferred to the integrator. During the next sampling steps, the capacitor is successively connected to the nodes 3, 4, and 5. During N_{R} charge samples (in Fig. 3 $N_{\mathrm{R}} = 4$) a total charge transfer of $\mathrm{C_1V_{BS}}$ is transferred to the integrator. Next, this procedure is repeated with sampling capacitor $\mathrm{C_2}$, and so on. After $N_{\mathrm{R}}N_{\mathrm{C}}$ samples, all capacitors have been used to sample V_{BS}. The total transferred charge amounts to

$$Q_{\mathrm{BS}} = V_{\mathrm{BS}} \sum_{\mathrm{i}} C_{\mathrm{i}} + N_{\mathrm{R}}N_{\mathrm{C}}Q_{\mathrm{off}} \tag{4}$$

where Q_{off} represents a charge which is also transferred to the integrator during each sample. This charge is constant for every sample, independent of i, even when the sampling capacitors have different values. Included in this charge is the offset of the active part of the integrator and a special contribution, as explained in Section IV. In the next measurement phase, the small voltage V_{out} is sampled with all of the sampling capacitors C_i in parallel. The switches $\mathrm{S_3}$ and $\mathrm{S_4}$ are active now. The charge transfer of $N_{\mathrm{R}}N_{\mathrm{C}}$ samples amounts to

$$Q_x = N_{\mathrm{R}}N_{\mathrm{C}}\left(Q_{\mathrm{off}} + V_{\mathrm{out}} \sum_i C_i\right). \tag{5}$$

Every sample of V_{out} lies in the same range as samples of V_{BS}. Note that the offset charge is the same as during the measurement of the divider.

In the final measurement phase, the offset voltage and other additive nonidealities are measured. In this phase $\mathrm{S_5}$, $\mathrm{S_{c,1}} \cdots \mathrm{S_{c,4}}$ are closed, while all of the switches $\mathrm{S_{r,1}} \cdots \mathrm{S_{r,5}}$, $\mathrm{S_3}$, and S_4 are open. Also, the offset sampling is performed $N_{\mathrm{R}}N_{\mathrm{C}}$ times. The total transferred charge amounts to

$$Q_{\mathrm{os}} = N_{\mathrm{R}}N_{\mathrm{C}}Q_{\mathrm{off}}. \tag{6}$$

With (4)–(6) it is found that

$$M_3 = \frac{Q_x - Q_{\mathrm{os}}}{Q_{\mathrm{BS}} - Q_{\mathrm{os}}} = \frac{N_{\mathrm{R}}N_{\mathrm{C}}V_{\mathrm{out}}}{V_{\mathrm{BS}}}. \tag{7}$$

With $N_{\mathrm{R}} = 8$ and $N_{\mathrm{C}} = 4$, the amplification factor for V_{out} amounts to 32. In Section IV, we explain how the charge packages are transferred to the time domain and further processed.

III. NONIDEALITIES

The accuracy of the interface circuit is limited by stochastic nonidealities such as noise and interference and by systematic nonidealities such as offset, switch-charge injection, the voltage dependence of the applied resistors and capacitors etc. In this section we show that the effect of many of the systematic nonidealities is eliminated or considerably reduced by the application of the three-signal method. Further we discuss the main noise sources.

A. Offset of the Charge Amplifier

The offset voltage of the integrator is directly eliminated by the three-signal method as shown in (7).

B. Finite dc Gain

The output voltage of the integrator is a ramp wave. Since the dc gain is finite, a ramp also appears on the inverting node of the integrator. The circuit in Fig. 3 is part of an oscillator, as discussed in Section IV. The threshold level of the comparator is a fixed voltage. The result is that the voltage at the inverting node of the integrator at the end of an oscillator period is always the same. This holds for all measurements. The effect of the finite dc gain can therefore be considered as an offset, which is eliminated by the three-signal technique.

C. Switch-Charge Injection

The MOS switches S_1 and S_2 (Fig. 3) are operated in a break-before-make mode to guarantee that no charge in $C_{\rm int}$ is lost. Further, care has to be taken that the capacitors $C_i (i = 1, 2 \cdots 4)$ have at least one node connected to a fixed voltage, to eliminate the undesired effect of parasitic capacitors. Therefore the switches on the left side of C_i are operated after S_1 and S_2. Thus switch-charge injection into $C_{\rm int}$ only originates from the switches S_1 and S_2. As the channel charge of S_1 and S_2 does not depend on $V_{\rm BS}$ or $V_{\rm out}$, even when the dc gain of the opamp is finite, the charge injection only contributes to $Q_{\rm off}$. This effect is eliminated by the three-signal method.

D. Voltage Dependence of the Resistors and Capacitors

The voltage dependence of the resistors does not influence the measurement, since $Q_{\rm BS}$ in (4) does not depend on the nodal voltages of nodes 2, 3, or 4 (Fig. 3). However, the voltage dependence of the capacitors can introduce some inaccuracy:

Let us assume that the sampling capacitors are given by

$$C_i(V) = C_{i,0}(1 + a_1 V + a_2 V^2 + a_3 V^3) \tag{8}$$

where V is the voltage across the capacitor, and $C_{i,0}$ is the zero-voltage capacitor value. To eliminate the odd-order terms, a pair of identical capacitors connected in anti-parallel is substituted for each capacitor in the circuit. The remaining even-order terms result in an inaccuracy: when the common-mode voltage of $V_{\rm out}$ and the voltage at the noninverting input of the integrator both equal $V_{\rm BS}/2$, then the final measurement result M_3 has a nonlinear part (see the Appendix)

$$M_3 = \frac{N_{\rm R} N_{\rm C} V_{\rm out}}{V_{\rm BS}} \left(1 - \frac{1}{4} a_2 V_{\rm BS}^2\right). \tag{9}$$

Example: For capacitors such as the poly/oxide/high-doped silicon the coefficient $a_2 < 2 \times 10^{-6}$ V^{-2}. When $V_{\rm BS} = 5$ V is applied to such capacitors then the inaccuracy due to the second-order voltage dependence is less than 13×10^{-6}, which is acceptable.

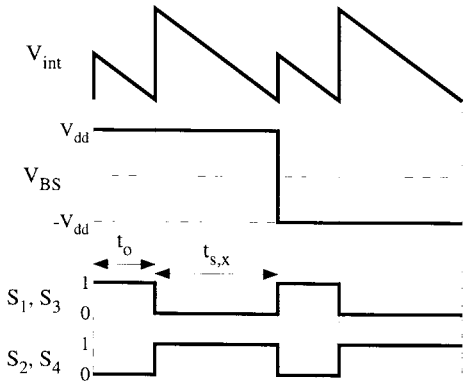

Fig. 5. Signals in the interface during a signal measurement.

E. The ON Resistance of the MOS Switches and Transients

The ON resistance $R_{\rm on}$ of the switches cause an increase in the time needed to charge or discharge the sampling capacitors C_i. Usually this effect does not cause significant problems.

Example: When $C_i = 12.5$ pF, $R_i = 6$ kΩ and $R_{\rm on} = 1$ kΩ, the maximum time constant $C_i(\frac{1}{4} N_{\rm R} R_{\rm i} + R_{\rm on})$ of the sampling circuit amounts to about 160 ns. When the sampling time is 10 μs, this time constant causes an error of less than 10^{-5}, which is acceptable.

The fact that rather high values for $R_{\rm on}$ are allowed is helpful in limiting the chip area.

F. Parasitic Capacitors

The on-chip sampling capacitor pairs $C_{\rm i}$ have parasitic capacitances to the substrate. The systematic effect of these capacitors is eliminated in the following way. The voltage at the inverting input of the integrator at the sampling moment is constant for all three measurement phases, even when the dc gain of the opamp is finite. Therefore, the charge transfer due to the parasitic capacitances is also the same for the three measurement phases. According to (7), this effect is eliminated. However, the parasitics can degrade the noise performance of the circuit, as explained below. The parasitic capacitors at the divider/bridge side of the sampling capacitors only affect the time constants during the sampling process (see also Section III-D). The MOS switches also have parasitic capacitances. Because of the applied switching sequence and timing these capacitors only contribute to $Q_{\rm off}$, which is eliminated by the three-signal method.

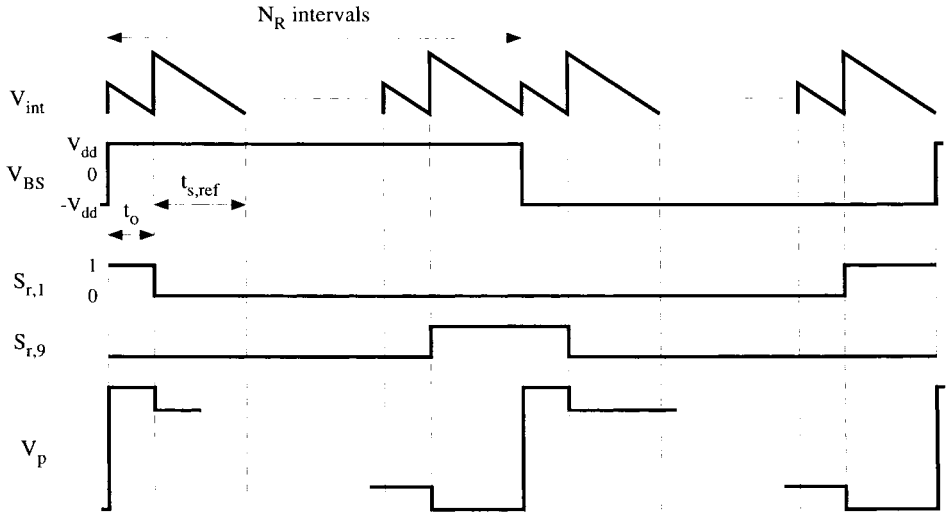

Fig. 6. Signals in the interface during the reference measurement.

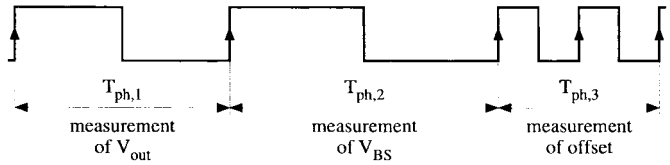

Fig. 7. The output signal of the interface.

G. Stochastic Errors

The interface contains a first-order oscillator which converts the reference signal and the bridge output voltage into a period. This period is measured by the microcontroller by counting the number of microcontroller clock cycles that fit into a period. This analog-to-digital conversion results in quantization noise. The equivalent noise $u_{\mathrm{eq,q}}$ with respect to V_{out} due to quantization process can be calculated using a more detailed expression of (2). For instance, for the period T_{x} for a signal measurement holds

$$T_{\mathrm{x}} = \frac{Q_{\mathrm{x}}}{I_{\mathrm{int}}} = N_{\mathrm{R}} N_{\mathrm{C}} \frac{Q_{\mathrm{off}} + V_{\mathrm{out}} \sum_i C_i}{I_{\mathrm{int}}}. \tag{10}$$

The noise $u_{\mathrm{eq,q}}$ can be calculated by using the derivative $dT_{\mathrm{x}}/dV_{\mathrm{out}}$ [8]

$$u_{\mathrm{eq,q}} = \frac{1}{\sqrt{6} N_{\mathrm{p}} f_{\mathrm{s}}} \left(\frac{dT_{\mathrm{x}}}{dV_{\mathrm{out}}} \right)^{-1} = \frac{1}{\sqrt{6} N_{\mathrm{p}} f_{\mathrm{s}}} \frac{I_{\mathrm{int}}}{N_{\mathrm{R}} N_{\mathrm{C}} \sum_i C_i} \tag{11}$$

where f_s represents the sample frequency and N_{P} the number of periods T_{x} to be measured.

Example: With $N_{\mathrm{P}} N_{\mathrm{R}} N_{\mathrm{C}} = 1024, f_{\mathrm{s}} = 3$ MHz, $I_{\mathrm{int}} = 600$ nA and $\Sigma\ C_i = 50$ pF, the equivalent input noise $u_{\mathrm{eq,q}} = 1.6\ \mu$V.

Another important noise source is thermal noise from the bridge, the switches (both included in kT/C noise), the integration current, the opamp, and the comparator. We only discuss the thermal noise of the opamp, the bridge, and the switches. A thorough noise consideration is beyond the scope of this paper, but can be found in [8].

The opamp noise voltage u_{n} is sampled on $\Sigma\ C_i$, as can be seen in Fig. 3. This holds for all measurement phases. The sampled noise charge amount to $u_{\mathrm{n}} \Sigma\ C_i$ and is transferred to the integrator. The noise power on $\Sigma\ C_i$ due to thermal noise of the bridge and switches amounts to $kT/\Sigma\ C_i$. The equivalent input noise with respect to the bridge output voltage is given by $u_{\mathrm{eq,th}}$

$$u_{\mathrm{eq,th}}^2 = \frac{BS_{\mathrm{u_n}} + \dfrac{kT}{\sum C_i}}{N} \tag{12}$$

where B is the closed loop bandwidth of the integrator, $S_{u_{\mathrm{n}}}$ the power spectral density of u_{n}, T the absolute temperature and N the number of samples.

Example: With $B = 1$ MHz, $S_{u_{\mathrm{n}}} = 10^{-15}$ V^2/Hz, $N = 1024$ and $\Sigma\ C_i = 50$ pF, the input noise $u_{\mathrm{eq,th}} = 1\ \mu$V.

Noise is also sampled on the parasitic capacitances of C_i, resulting in an increase of $u_{\mathrm{eq,th}}$. The paracitics do not contribute to the signal transfer so the SNR is degraded.

IV. The Complete Circuit

Fig. 4 shows a schematic of a complete bridge interface, which operates as follows. The comparator monitors the output voltage V_{int} of the integrator. When the threshold level is reached, the logic circuitry is put in a new state, where certain switches are set in an alternate position. A new state starts with the transfer of charge to the integrator. The dc current I_{int} is continuously being integrated. After a certain time, the transferred charge is completely removed and a new logic state is entered. This process results in periodic signals. In our circuit $N_{\mathrm{R}} = 8$ and $N_{\mathrm{R}} = 4$.

The bridge is ac excited; that is, the excitation voltage for the bridge is a square wave. By using this technique, the effect of parasitic thermocouple junctions and low-frequency disturbing signals is removed after demodulation within the chip.

We first consider the measurement of the bridge output voltage $V_{\rm out}$. The voltage $V_{\rm int}$ for a signal measurement is displayed in Fig. 5. This picture also displays the control signals (0 = open, 1 = closed) of several switches. To guarantee that the charge flow to the integrator is always positive, for both polarities of $V_{\rm out}$, an offset capacitor C_{02} is added. Charge on this capacitor is transferred to the integrator at the beginning of $t_{\rm s}$. The time t_0 is necessary to settle correctly after inversion of the bridge excitation voltage. To generate this time interval, an offset capacitor C_{01} is added and charge on this capacitor is transferred to the integrator at the beginning at t_0. For the time intervals $t_{\rm s,x}$ and t_0 it holds that

$$t_{\rm s,x} = \frac{V_{\rm dd}C_{02} + V_{\rm out}\sum_{i=1}^{N_{\rm c}} C_i}{I_{\rm int}}$$
$$t_0 = \frac{V_{\rm dd}C_{01}}{I_{\rm int}}. \tag{13}$$

Since the current through switches S_3 and S_4 is zero at the sample moment (the end of t_0 and t_s), switch ON resistance and lead wire resistance have no effect on these two time intervals.

We now discuss the reference measurement during which the bridge supply voltage is being measured. Also, during this measurement, the four-wire measurement technique is being used, since the sampling capacitors sense the voltage across the bridge, via $S_{r,1}$ and $S_{r,9}$. The output voltage of the integrator, the voltage at node P (the right-hand side of switches S_r), and some switch control signals are shown in Fig. 6. Note that the bridge-excitation frequency is reduced by a factor of $N_{\rm R}$ in comparison with the signal measurement.

For the time interval $t_{{\rm s,ref},i,j}$ we obtain

$$t_{{\rm s,ref},i,j} = \frac{V_{\rm dd}C_{02} + (V_j - V_{j+1})C_i}{I_{\rm int}} \tag{14}$$

where $V_j - V_{j+1}$ is the voltage across resistor $R_j (j = 1, 2 \cdots N_{\rm R})$.

The effect of both offset charges $V_{\rm dd}C_{01}$ and $V_{\rm dd}C_{02}$ is additive and is independent of the signal to be measured, so that it is eliminated by the three-signal method. A single measurement phase with duration $T_{{\rm ph},k}$ $(k = 1, 2,$ or $3)$ consists of 1024 intervals $(t_0 + t_{\rm s})$. At the end of a measurement phase, the interface automatically starts a new one. To enable the identification of the offset measurement phase, the frequency of the square wave output signal is doubled during this measurement phase, resulting in the signal displayed in Fig. 7.

After completion of the three measurement phases, the final result is calculated in the microcontroller using an equation which is found from (13) and (14) which yields

$$M_3 = \frac{T_{\rm ph,1} - T_{\rm ph,3}}{T_{\rm ph,2} - T_{\rm ph,3}} = \frac{N_{\rm R}N_{\rm C}V_{\rm out}}{V_{\rm BS}} \tag{15}$$

where $T_{\rm ph,1}, T_{\rm ph,2}$ and $T_{\rm ph,3}$ are the signal, reference and offset measurement phase respectively.

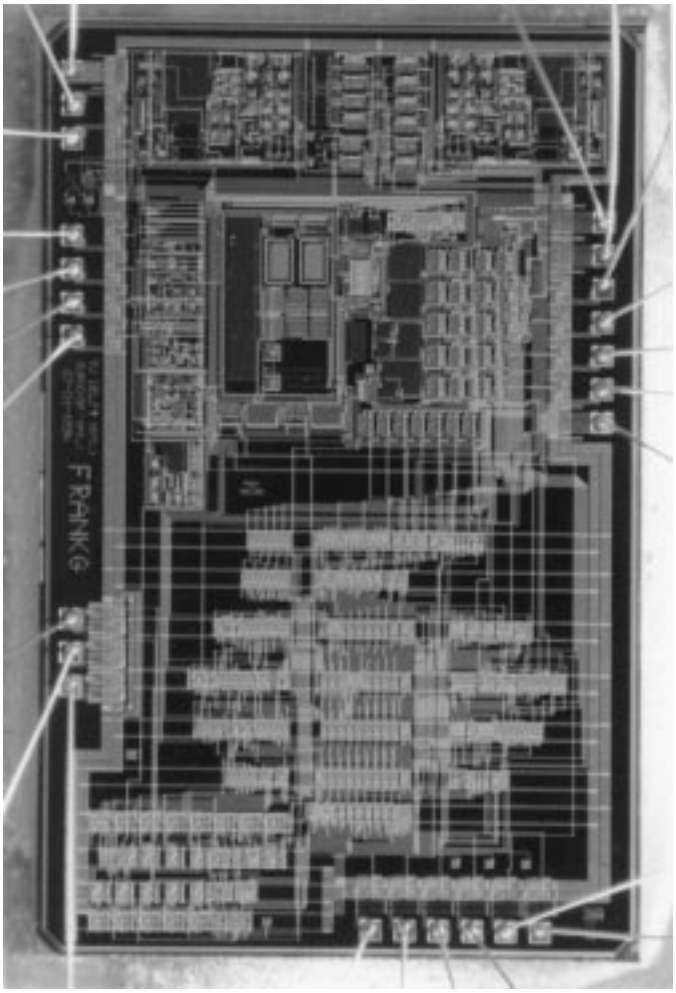

Fig. 8. A photomicrograph of the chip.

TABLE I
THE MAIN CONDITIONS AND MEASUREMENT RESULTS

Item	Value
Supply voltage	4-6 V
Measurement time	100 ms
$T_{{\rm ph},i}$	17 ms to 40 ms
VCO frequency	26 kHz to 60 kHz
Temperature range	-20 °C to 70 °C
Uncertainty (@ $\lvert V_{\rm out}/V_{\rm BS}\rvert$<2 %)	10 µV (10^{-4})
Total eq. Noise	4 µV

V. MEASUREMENT RESULTS

The complete circuit is implemented on a single chip (Fig. 8) in a 3 μm BiCMOS process.

The following component values and parameters have been used:

$$N_{\rm R} = 8, \quad N_{\rm C} = 4, \quad C_i = 12.5 \text{ pF}, \quad C_{01} = 1 \text{ pF},$$
$$C_{02} = 2 \text{ pF}, \quad C_{\rm int} = 10 \text{ pF}, \quad I_{\rm int} = 600 \text{ nA} \quad \text{and}$$
$$R_i = 6 \text{ k}\Omega.$$

The applied microcontroller is of the type 87C51FA with internal 8 kilobytes EPROM and 256 bytes RAM. The clock frequency is 12 MHz and the sampling frequency of the interface output is 3 MHz. The internal oscillator frequency varies between 26 kHz to 60 kHz. The phase times $T{\rm ph}, i$

are in the range 17 ms to 40 ms. The total measurement time varies between 80 ms to 100 ms. The supply voltage amounts to 5 V. The main measurement results are listed in Table I.

The accuracy of the bridge interface has been tested using accurately-known bridge resistors, configured to a 3 kΩ bridge. The maximum range for the ratio $V_{\rm out}/V_{\rm BS}$ amounts to $\pm 2\%$. The error in this range is less than 10^{-4} of the maximum output voltage, which corresponds to 10 μV. This error does not significantly change over the temperature range from -20 °C to $+70$ °C. The standard deviation of M_3 for a constant bridge imbalance is about 40×10^{-6}, corresponding to 4 μV. This deviation originates from quantization and thermal noise.

VI. Conclusions

The new bridge interface circuit does not need any calibration and is insensitive to long-term drift and temperature changes. These characteristics are a consequence of the applied measuring methods: the three-signal technique and a novel divider method called "piece-wise measurement." The complete interface has been implemented in a BiCMOS process. The total uncertainty amounts to about 10^{-4} of the maximum bridge imbalance. This figure includes the noise which has a standard deviation of $4 \times 10^{-5}(4\ \mu\text{V})$, but is exclusive of the error of the bridge itself. The measurement is insensitive to the resistance of the connecting bridge wires and also insensitive to the switch ON resistance of the applied (on-chip) switches. The total time required to measure the bridge imbalance amounts to about 0.1 s.

Appendix

In this appendix, we calculate the effect of the voltage dependence of the sampling capacitors on the measurement result M_3. This voltage dependence is modeled by

$$C_i(V) = C_{i,0}(1 + a_1 V + a_2 V^2 + a_3 V^3). \qquad (16)$$

The odd-order terms can be eliminated by the connection of two equal capacitors in anti-parallel. The remaining even-order terms contribute to the nonlinearity.

During a reference measurement, the capacitors C_i sample $V_{\rm dd}$ and GND. The charge flow through the sampling capacitors is only determined by the voltage of nodes 1 and 5 in Fig. 3. During $N_{\rm R}N_{\rm C}$ oscillator periods this charge equals $Q'_{\rm BS}$

$$Q'_{\rm BS} = V_{\rm BS}(1 + \tfrac{1}{4}a_2 V_{\rm BS}^2)\sum C_i. \qquad (17)$$

The charge flow through the sampling capacitors during $N_{\rm R}N_{\rm C}$ oscillator periods for the signal measurement is given by $Q'_{\rm x}$

$$Q'_{\rm x} = N_{\rm R}N_{\rm C}V_{\rm out}(1 + \tfrac{1}{4}a_2 V_{\rm out}^2)\sum C_i. \qquad (18)$$

Since we omitted the offset, the measurement result M_3 is approximated by

$$M_3 = \frac{Q'_{\rm x}}{Q'_{\rm BS}} \cong \frac{N_{\rm R}N_{\rm R}V_{\rm out}}{V_{\rm BS}}\left(1 - \frac{1}{4}a_2 V_{\rm BS}^2\right). \qquad (19)$$

This approximation is valid if $V_{\rm BS} \gg V_{\rm out}$.

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