A Simple MOSFET Model for Circuit Analysis

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Abstract—**A simple, general, yet realistic MOSFET model, namely the *n*th power law MOSFET model, is introduced. The model can express *I–V* characteristics of short-channel MOSFET's at least down to 0.25-μm channel length and resistance inserted MOSFET's. The model evaluation time is about 1/3 of the evaluation time of the SPICE3 MOS LEVEL3 model. The model parameter extraction is done by solving single variable equations and thus can be done within a second, being different from the fitting procedure with expensive numerical iterations employed for the conventional models. The model also enables analytical treatments of circuits in short-channel region and plays a role of a bridge between a complicated MOSFET current characteristics and circuit behavior in the deep-submicrometer region.**

I. Introduction

SHOCKLEY model for MOSFET [1] is widely used in analytical treatments of MOSFET circuits. However, the model is not accurate in the short-channel region because it neglects the velocity saturation effects of carriers as shown in Fig. 1. On the other hand, there are more precise MOS models like the SPICE LEVEL3 model [2], [3], BSIM [4], table look-up models [5], and so on [6], [7]. However, some of them are time-consuming in evaluating models [3] and some of them need a special system with a hardware/software combination for extracting model parameters [4]–[6] and the number of parameters is large. Moreover, most of the precise models [3], [4], [6], [7] need a model parameter extraction procedure with expensive numerical iterations [8], [9], and once the extracted model parameters happen not to give satisfactory results, there is no way to know whether the problem lies in the model itself or in the extracting procedure. Sometimes it takes hours to extract the parameter set.

In order to fill the gap between the simple Shockley model and the more precise models, a new model, namely, the *n*th-power law MOSFET model, is proposed in this paper. The model is an extension of the alpha-power law MOSFET model [10] but much more accurate in the linear region and in the treatment of drain saturation voltage. The model parameter is compact and the model parameter extension is done by solving single-variable equations and thus can be done within a second. The model is implemented in SPICE3c1 circuit simulator and speed-up of the simulation time is observed. Since the model equation is simple, an analytical treatment of circuit operations can be carried out using the model, which helps to understand the circuit behavior in the submicrometer region. The objective of the proposed model is not to compete with the existing more precise models but rather to provide a simple model which is placed just above the Shockley model.

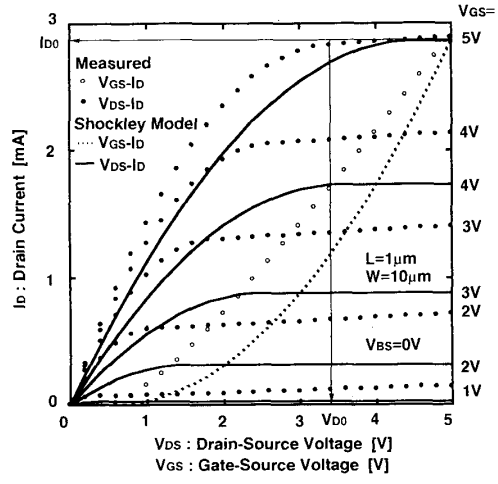

Fig. 1. NMOS *I–V* curves with Shockley MOS model.

The model is presented in Section II and the model parameter extraction procedure is described in Section III. Section IV is dedicated to the results when the model is implemented in SPICE3. The application of the model to the analysis of an inverter delay is given in Section V followed by the conclusion in Section VI.

II. Model Description

The proposed model equations are as follows. I_D is the drain current.

$$V_{TH} = V_{T0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}) \tag{1}$$

$$V_{DSAT} = K(V_{GS} - V_{TH})^m \tag{2}$$

$$I_{DSAT} = \frac{W}{L_{EFF}} B(V_{GS} - V_{TH})^n \tag{3}$$

$$I_D = I_{D5} = I_{DSAT}(1 + \lambda V_{DS}) \qquad \lambda = \lambda_0 - \lambda_1 V_{BS}$$
$$(V_{DS} \geq V_{DSAT}\text{: saturated region}) \tag{4}$$

$$I_D = I_{D3} = I_{D5}\left(2 - \frac{V_{DS}}{V_{DSAT}}\right)\frac{V_{DS}}{V_{DSAT}}$$
$$(V_{DS} < V_{DSAT}\text{: linear region}) \tag{5}$$

where V_{GS}, V_{DS}, and V_{BS} are gate-source, drain-source, and bulk-source voltage, respectively. W is a channel width and L_{EFF} is an effective channel length. V_{TH} denotes a threshold voltage, V_{DSAT} a drain saturation voltage, and I_{DSAT} a drain

Manuscript received March 27, 1990; revised September 23, 1990. This work was supported by Toshiba Corporation under a grant. The review of this paper was arranged by Associate Editor P. K. Ko.

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IEEE Log Number 9041654.

0018-9383/91/0400-0887$01.00 © 1991 IEEE

saturation current. V_{T0}, γ, and $2\phi_F$ are parameters which describe the threshold voltage. Parameters K and m control the linear region characteristics while B and n determine the saturated region characteristics. λ_0 and λ_1 are related to the finite drain conductance in the saturated region. The subscript 3 and 5 for I_D denotes a triode and a pentode operating region, respectively, and they are totally different from $I_{D,3}$ and $I_{D,5}$ defined in Fig. 7 and used in (8). The validity of (3) for various MOSFET's is shown in Fig. 2.

The model is reduced to the Shockley model if $K = 1$, $m = 1$, $B = 0.5\beta$, and $n = 2$. The model can also express an I-V characteristic where V_{DSAT} is proportional to $\sqrt{V_{GS} - V_{TH}}$ and I_{DSAT} is proportional to $(V_{GS} - V_{TH})$, which is predicted by a short-channel MOSFET theory [11]. An application of the model to 0.25-μm MOSFET's [6] is shown in Figs. 3 and 4. The results are satisfactory.

In (5), drain current in the linear region is assumed to quadratically depend on V_{DS}. Several other forms have been tried including third-order and fourth-order polynomials but the difference was less than 2% of I_{D0} (the drain current observed when $V_{GS} = V_{DS} = V_{DD}$). Similar description is found in [13]. Consider a mathematical problem: "what is the maximum error when the following $f(x)$ is approximated by $g(x) = Ax^2 + Bx$?"

$$f(x) = \frac{(2 - x)x}{1 + \theta' x}, \qquad \text{for } 0 \le x \le p$$

$$= f(p), \qquad \text{for } x > p$$

where $p(=(-1 + \sqrt{1 + 2\theta})/\theta)$ gives a peak in $f(x)$ and the error is defined by $(g(x) - f(x))/f(p)$. If x is set equal to $V_{DS}/(V_{GS} - V_{TH})$ and θ' to $\theta/(V_{GS} - V_{TH})$, this function corresponds to the drain current form including high-electric field effects and θ' usually takes the value between 0 and 0.5. The upper bound of the above problem can be obtained by assuming that $g(x)$ goes through three points: $(0, 0)$, $(p/2, f(p/2))$, and $(p, f(p))$ and also assuming that $g(x)$ becomes flat after it reaches the peak point. Then the upper bound of the above problem is 2.2% when $0 \le \theta' \le 0.5$ and 3.6% when $0 \le \theta' \le 0.9$. A similar problem can be considered when x is substituted by $x - r \cdot f(x)$ in the above equation. This roughly corresponds to a situation where a resistor is inserted in series to a MOSFET. If $0 \le r \le 0.1$ and $0 \le \theta' \le 0.9$, the upper bound of the maximum error is 2.5%. Thus the quadratic approximation of the linear region drain current is reasonable.

The model parameters are listed in Table I for 0.25-μm n-channel MOSFET. The present model does not give a very good approximation near and below the threshold voltage as seen in Fig. 4. The near- and subthreshold region modeling is not important in calculating delay of most VLSI's. The modeling of the region is important in estimating the charge decay characteristic of charge storage nodes but in this case a statistical model should be used since it is very sensitive to process variation.

If the modeling of the back-gate effect is not so important in a certain circuit analysis, further simplification is possible by using the following formula:

$$V_{TH} = V_{T0} - \gamma_1 V_{BS}. \tag{6}$$

When finite output conductance is not important, γ's can be set to zero.

In the submicrometer devices, the contact resistance, drain/source diffusion resistance, and hot-carrier-induced drain resistance [12] are important. It is better for a MOS model to incorporate these resistance effects by just modifying parameters of the model. If these series resistance is modeled by spurious re-

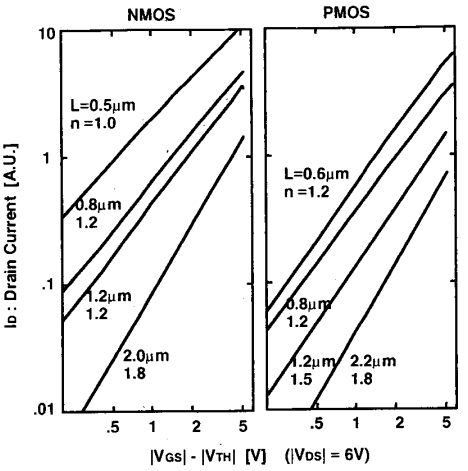


Fig. 2. Measured n value for various MOSFET's.

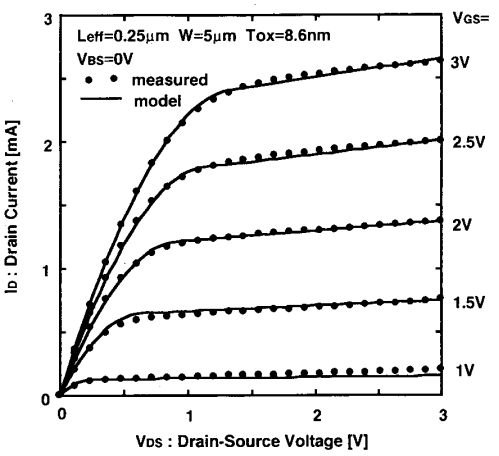


Fig. 3. V_{DS}-I_D characteristics of 0.25-μm NMOS ($V_{BS} = 0$ V).

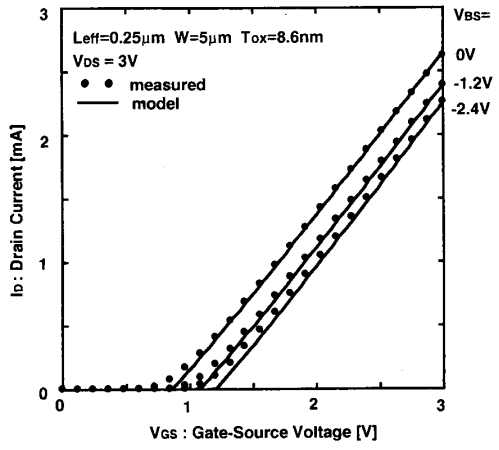


Fig. 4. V_{GS}-I_D characteristics of 0.25-μm NMOS.

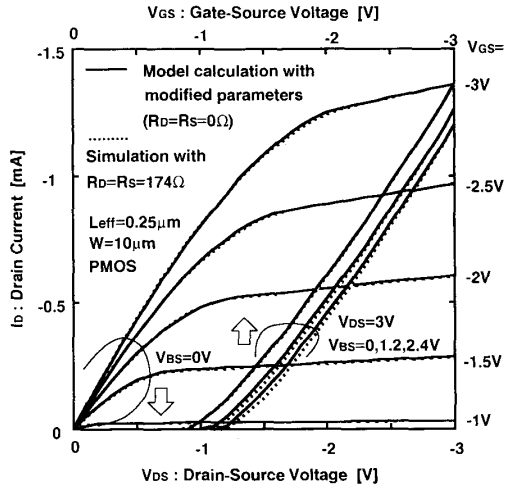


Fig. 5. 0.25-μm PMOS V_{DS}–I_D and V_{GS}–I_D characteristics with and without source and drain resistance.

TABLE I
MODEL PARAMETERS FOR 0.25 μm

Parameters	NMOSFET	PMOSFET
B	4.9721×10^{-5}	1.1151×10^{-5}
n	1.0484	1.3649
K	0.83496	1.0541
m	0.6193	0.74003
λ_0	0.066265	0.128
λ_1	0.0038573	0.012923
V_{T0}	0.85502	−0.87241
γ	0.29648	0.26074
$2\phi_F$	0.20556	0.21691

sistors, it is practically difficult to separate these resistance component, that is, the extraction of the parameter set is difficult. Moreover, the resistors increase the number of nodes and hence calculation time. Since the present model is quite general, it can reproduce the I–V curves of resistor-inserted MOSFET only by changing parameters.

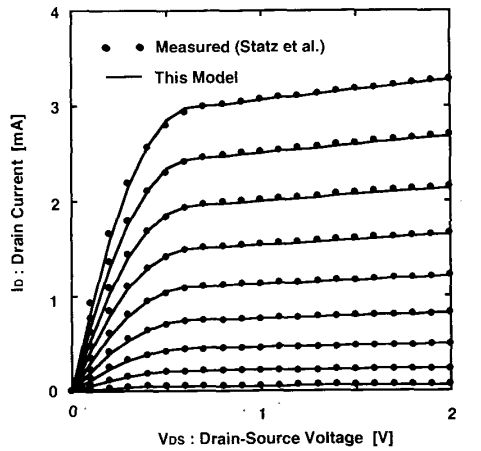
An example is shown in Fig. 5. Dotted lines in the figure are simulated I_D–V_{DS} curves of a 0.25-μm PMOSFET, which includes lumped resistors whose value is 10% of the effective MOSFET resistance inserted in the drain and the source. Solid lines in the figure are calculated I_D–V_{DS} curves using the present model with the modified parameter set and without any resistors inserted in the drain and the source. This means that the present model can be fitted to the measured MOSFET I–V characteristics which includes inseparable resistor effects, without adding extra nodes which are necessary when the resistor effects are modeled by lumped external resistors.

To demonstrate that the model is quite general, the model is applied to GaAs FET [13] in Fig. 6(a). The salient feature of the GaAs FET is that V_{DSAT} is constant and not a function of V_{GS}, which can be expressed by setting $m = 0$. Another example is shown in Fig. 6(b), where the present model is fitted to a 1-μm n-channel MOSFET I–V characteristic.

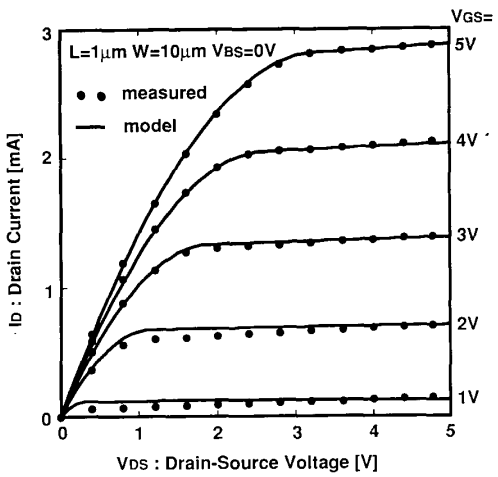
III. PARAMETER EXTRACTION

The model parameter extraction starts by selecting fitting points on the I–V curves as in Fig. 7. Then the following formulas give all the parameters. The subindex "i" (i = 1–11) corresponds to the fitting point number in the figure.

$$\lambda_0 = \frac{I_{D,2} - I_{D,1}}{I_{D,1} V_{DS,2} - I_{D,2} V_{DS,1}} \tag{7}$$



(a)



(b)

Fig. 6. (a) GaAs FET modeling and (b) 1-μm NMOS example.

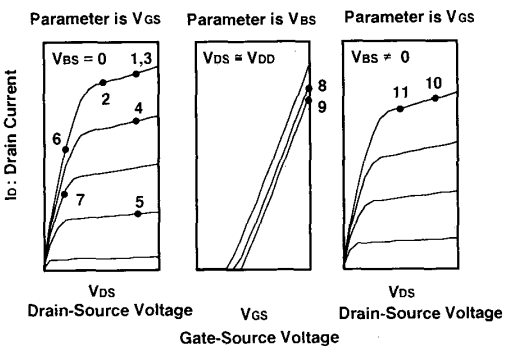


Fig. 7. Selected points for model parameter extraction.

$$I_{Z3} = \frac{I_{D,3}}{1 + \lambda_0 V_{DS,3}} \qquad I_{Z4} = \frac{I_{D,4}}{1 + \lambda_0 V_{DS,4}}$$

$$I_{Z5} = \frac{I_{D,5}}{1 + \lambda_0 V_{DS,5}}. \tag{8}$$

Then, V_{T0} can be obtained by solving the following equation. The bisection method [14] is the best choice for the solution since it finds out the root without fail within ten iterations.

$$f_V(V_{T0}) = \log\left(\frac{I_{Z3}}{I_{Z4}}\right)\log\left(\frac{V_{GS,4} - V_{T0}}{V_{GS,5} - V_{T0}}\right) - \log\left(\frac{I_{Z4}}{I_{Z5}}\right)\log\left(\frac{V_{GS,3} - V_{T0}}{V_{GS,4} - V_{T0}}\right) = 0 \tag{9}$$

$$n = \frac{\log\left(I_{Z3}/I_{Z4}\right)}{\log\left((V_{GS,3} - V_{T0})/(V_{GS,4} - V_{T0})\right)}$$

$$B = \frac{I_{Z3}}{(V_{GS,3} - V_{T0})^n} \tag{10}$$

$$E6 = I_{D,6}/\left\{B(V_{GS,6} - V_{T0})^n(1 + \lambda_0 V_{DS,6})\right\} \tag{11}$$

$$E7 = I_{D,7}/\left\{B(V_{GS,7} - V_{T0})^n(1 + \lambda_0 V_{DS,7})\right\} \tag{12}$$

$$V_{D\mathrm{SAT},6} = V_{DS,6}(1 + \sqrt{1 - E6})/E6$$

$$V_{D\mathrm{SAT},7} = V_{DS,7}(1 + \sqrt{1 - E7})/E7 \tag{13}$$

$$m = \frac{\log\left(V_{D\mathrm{SAT},6}/V_{D\mathrm{SAT},7}\right)}{\log\left((V_{GS,6} - V_{T0})/(V_{GS,7} - V_{T0})\right)}$$

$$K = \frac{V_{D\mathrm{SAT},6}}{(V_{GS,6} - V_{T0})^m}. \tag{14}$$

λ_1 is obtained from the following equation:

$$\frac{I_{D,11} - I_{D,10}}{I_{D,11}V_{DS,11} - I_{D,10}V_{DS,10}} = \lambda_0 - \lambda_1 V_{BS,10} \tag{15}$$

$$I_{D,8}/(1 + \lambda_0 V_{DS,8} - \lambda_1 V_{DS,8}V_{DS,8}) = K(V_{GS,8} - V_{\mathrm{TH},8})^n \tag{16}$$

$$I_{D,9}/1 + \lambda_0 V_{DS,9} - \lambda_1 V_{BS,9}V_{DS,9}) = K(V_{GS,9} - V_{\mathrm{TH},9})^n. \tag{17}$$

After obtaining $V_{\mathrm{TH},8}$ and $V_{\mathrm{TH},9}$ by solving the above equations which is just a manipulation of the expressions, $2\phi_F$ is obtained by solving the following equation with the bisection method:

$$f_P(2\phi_F) = (\sqrt{2\phi_F - V_{BS,8}} - \sqrt{2\phi_F})(V_{\mathrm{TH},9} - V_{T0}) - (\sqrt{2\phi_F - V_{BS,9}} - \sqrt{2\phi_F})(V_{\mathrm{TH},8} - V_{T0}) = 0. \tag{18}$$

Even if the fitting results are not satisfying at the first trial it is easy and fast to try again with slightly different fitting points, since the model parameters are appearance-oriented, that is, they have a direct meaning in controlling I–V curve shapes and they are nondegenerate. Usually, from two to four retries were enough for the satisfactory results for 2-, 1.2-, 0.8-, and 0.5-μm MOSFET's. It is even possible to extract the model parameters from an I–V plot on a sheet on paper.

The extracted parameter set is valid only for a narrow range of channel length but usually the shortest channel length is used for almost all the MOSFET's in a VLSI and two or three sets of parameters are enough in designing a whole VLSI. The separate parameter set is also required for a very-narrow-width device and a shallow V_{TH} device and an i-type (intrinsic V_{TH}) device if they are employed. Even with the more precise models, it is a good practice to use them near the condition where the model parameters are extracted, otherwise the model prediction is not guaranteed.

TABLE II
COMPUTATIONAL CHARACTERISTIC

Item	LEVEL1	Proposed Model	LEVEL3
Coding lines in C[1]	~40	~60	~210
Time required for current/derivative calculation[2]	3.4 s	7.5 s	21.1 s

[1]Including derivative calculation and excluding comment lines.
[2]Loop for $-3\ \mathrm{V} \le V_{BS} \le 0$ step 0.5 V, $0 \le V_{GS} \le 5$ V step 0.05 V, and $0 \le V_{DS} \le 5$ V step 0.05 V.

TABLE III
SPICE3 SIMULATION TIME

Circuit No.	No. of MOS's	LEVEL1	Proposed Model	LEVEL3
1	14	2.7 s	6.4 s	6.9 s
2	68	33.3 s	34.5 s	118 s
3	640	227 s	171 s	184 s
4	1060	303 s	372 s	808 s

IV. APPLICATION TO CIRCUIT SIMULATION

Some of the computational properties of the model are listed in Table II. The coding is straightforward and the model evaluation time is about 1/3 of the LEVEL3 model. The codes for LEVEL 1 and 3 are extracted from SPICE3. If the precision is not so important, the use of approximated formulas for log and exp functions [15] is effective and 30% further reduction in time is possible.

The simulation time when implemented in SPICE3 is listed in Table III. The capacitance model used is the same model as LEVEL1, LEVEL2, and LEVEL3 capacitance model based on the Meyer's model which can be improved further [16]. The present model usually shows faster total simulation time than the LEVEL3 model. The simulated waveforms are compared in Fig. 8. LEVEL1 model gives only a rough approximation of the real MOSFET I–V characteristics. Since I_{D0} (drain current observed when both of V_{GS} and V_{DS} are biased V_{DD}) is a good index for MOSFET drivability and since in [10] it has been demonstrated that I_{D0} controls the delay, I_{D0} was fitted using the LEVEL1 model in obtaining Fig. 8.

With LEVEL3 model, drain current abnormal kinks sometimes appear near the saturation point, and this gives rise to a convergence problem. The present model never show this type of kinks and hence no degradation of convergence near the drain saturation voltage.

V. APPLICATION TO CIRCUIT ANALYSIS

As an application of the model to the circuit analysis, CMOS inverter delay is analyzed here. As seen from Fig. 9, a CMOS inverter with a ramp input can be approximated by an NMOS circuit with an input waveform like $V_{\mathrm{in,ap}}$. $V_{\mathrm{in,ap}}$ is the same as

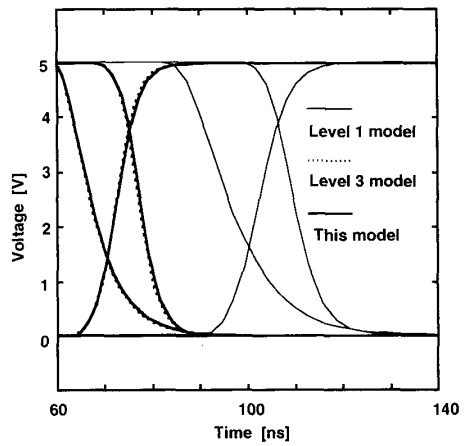


Fig. 8. Comparison of simulated waveforms by various MOS models.

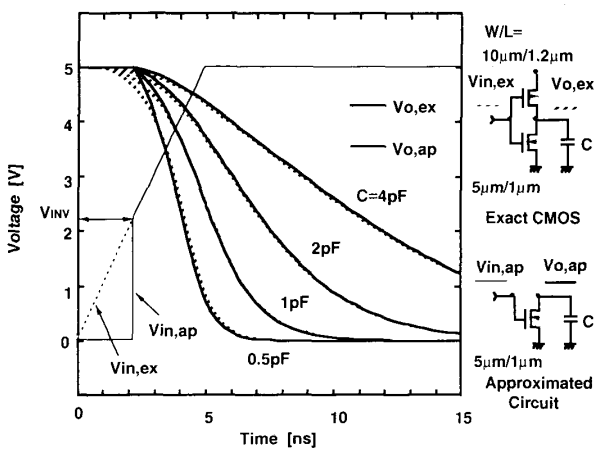


Fig. 9. Approximating CMOS by NMOS.

the real ramp input except that it remains zero until the input reaches the logic threshold voltage. The logic threshold voltage is the gate input voltage which makes the output voltage equal to a half V_{DD}.

For the extreme cases, this approximation is exact. That is, for the ultimately fast input case, the ramp input becomes a step function and $V_{\text{in,ap}}$ also becomes the step function and the current through PMOS can be completely neglected. For the extremely slow input, the output changes abruptly and comes down to $0.5V_{DD}$ when the input goes across the logic threshold voltage. The approximated circuit shows the same delay. The intermediate case is shown in Fig. 9 and this approximation greatly reduces the complexity of the system and makes it possible to treat the CMOS inverter delay analytically.

The derivation begins by setting up the differential equation which governs gate operation. This equation is then solved for the very fast input case and for the very slow input case and the two solutions are connected smoothly. A brief derivation is given in the Appendix (a detailed derivation can be found in [17]). First, define a critical input transition time t_{T0}.

$$t_{T0} = \tau \frac{(n+1)(1-v_T)^n}{(1-v_T)^{n+1} - (v_V - v_T)^{n+1}} \left(\frac{1}{2} + \frac{\lambda'}{7}\right) \quad (19)$$

where $v_T = V_{T0}/V_{DD}$, $v_V = V_{\text{INV}}/V_{DD}$, $\tau = C_O V_{DD}/I_{D0}$, $\lambda' = \lambda_1 V_{DD}$, and $v_{D0} = V_{D0}/V_{DD}$. C_O is an output capacitance and V_{DD} is an applied power voltage. I_{D0} is defined as the drain current observed when $V_{GS} = V_{DS} = V_{DD}$ and is a good index of drivability of a MOSFET (see Fig. 1). V_{D0} is defined as the drain saturation voltage when $V_{GS} = V_{DD}$. These two quantities together with the velocity saturation index n play an essential role in determining circuit behavior.

Then the delay t_d, the delay from $0.5V_{DD}$ of input to $0.5V_{DD}$ of output, and the effective output transition time t_{TOUT} can be expressed as follows. In calculating t_{TOUT}, the output waveform slope is approximated by 70% of its derivative at the half V_{DD} point [18]. t_{TOUT} can be used as t_T for the next logic gate.

($t_T \leq t_{T0}$: for faster input)

$$t_d = t_T\left\{\frac{1}{2} - \frac{1-v_T}{n+1} + \frac{(v_V - v_T)^{n+1}}{(n+1)(1-v_T)^n}\right\} + \tau\left(\frac{1}{2} + \frac{\lambda'}{7}\right) \quad (20)$$

$$t_{TOUT} = \frac{\tau}{0.7} \frac{8v_{D0}^2(1+\lambda')}{(4v_{D0}-1)(2+\lambda')} \quad (21)$$

($t_T \geq t_{T0}$: for slower input)

$$t_d = t_T\left[v_T - \frac{1}{2} + \left\{(v_V - v_T)^{n+1} + \frac{(1-v_T)^n(n+1)}{t_T/\tau}\left(\frac{1}{2} + \frac{\lambda'}{7}\right)\right\}^{1/(n+1)}\right] \quad (22)$$

$$t_{TOUT} = \frac{\tau}{0.7}\left(\frac{1-v_T}{t_d/t_T + 1/2 - v_T}\right)^n \frac{2+2\lambda'}{2+\lambda'}. \quad (23)$$

The formulas are valid in a wide range of t_T and the channel-width ratio of PMOS and NMOS (W_p/W_n) as shown in Fig. 10. In the figure, the result of the simpler model calculation of [10] is also shown. The simpler model is useful when the input transition is reasonably fast but becomes a poor approximation in a very slow input transition region where the present model is still effective.

The logic threshold voltage V_{INV} was calculated by the following expression:

$$v_V = \frac{V_{\text{INV}}}{V_{DD}} = \frac{I_{D0N}^{1/n} v_{TN} + I_{D0P}^{1/n}(1-v_{TN})}{I_{D0N}^{1/n} + I_{D0P}^{1/n}(1-v_{TN})/(1-v_{TP})},$$

$$n = \frac{n_N + n_P}{2} \quad (24)$$

where subindexes N and P denote NMOS and PMOS, respectively. The accuracy of the formulas is shown in Fig. 11.

Another application to a circuit analysis is given in [17], where the series-connected MOSFET structures found in NAND and NOR gates are analyzed with the nth-power law MOS model. In the submicrometer region, an 8-input NAND shows only 4–5 times longer delay compared with an inverter and is not 8 times longer which is the case with the long-channel MOSFET's. It has been clarified that it is because the series-connected MOSFET's structure mitigates the V_{DS} and V_{GS} of each MOSFET and this in turn reduces the severe velocity saturation effect ob-

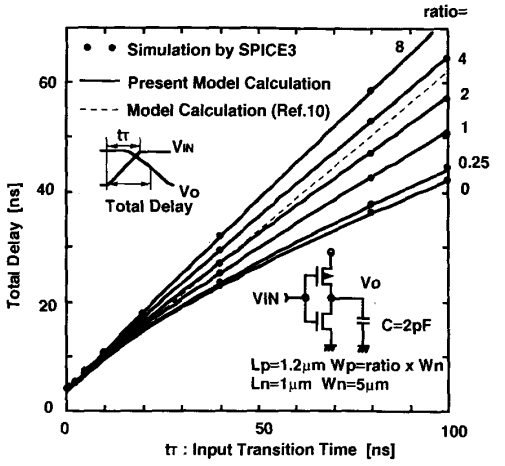


Fig. 10. Delay dependence on input transition time and W_p/W_n ratio.

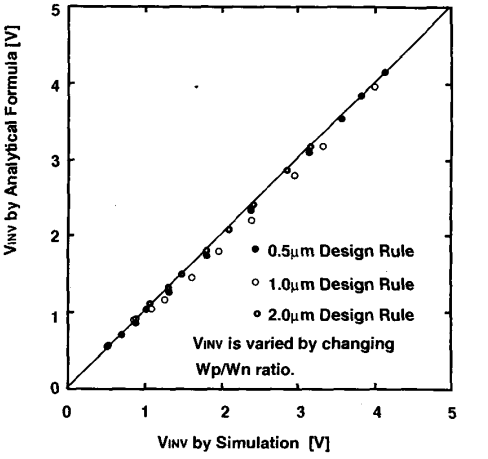


Fig. 11. Comparison of approximated formula and simulation for CMOS inverter logic threshold voltage V_{INV}.

served in the submicrometer region. Other possible applications of interest are to stability analysis of a static RAM memory cell and a sense amplifier optimization.

VI. Conclusion

A new MOS model, namely the nth-power law MOS model, is proposed. The model offers the following features:

- simple yet realistic
- fast in evaluation
- fast to extract model parameters
- general
- good for analytical treatment of circuit behavior.

The feasibility and effectiveness of the model are demonstrated by using 0.25-μm MOSFET's and SPICE3. Using the model, an analytical expression is derived for CMOS inverter delay, which includes the CMOS effects and the velocity saturation effects.

Appendix
Derivation of the Delay Expression

In the Appendix, the discharging of an output capacitance through NMOS's is explained since the discussion for the charging by PMOS's is symmetric. First, a ramp input is approximated by $V_{in,ap}$ as seen from Fig. 9. The strategy for solving the differential equation which governs the discharging process is to solve it for the very fast input case and for the very slow input case separately as mentioned in the text. The two solutions for the two extreme cases happen to be connected smoothly.

In the following, voltages are normalized by V_{DD}, currents by I_{D0}, and time by $\tau = C_O V_{DD}/I_{D0}$. The normalized voltage is denoted as v instead of V, the normalized current i instead of I, and the normalized time t' instead of t. λ' denotes λV_{DD}. First, consider a very fast input case. Before the input reaches V_{DD}, the differential equation which governs the discharging process can be written as

$$\frac{dv_O}{dt'} = -i_5 = -\left(\frac{t'/t'_T - v_T}{1 - v_T}\right)^n \frac{1 + \lambda' v_O}{1 + \lambda'} \tag{A1}$$

which should be solved with the initial condition of $v_O = 1$ at $t' = t'_V$. The solution is

$$\frac{1 + \lambda'}{\lambda'} \log \frac{1 + \lambda' v_O}{1 + \lambda'} = -\frac{t'_T}{(1 - v_T)^n (n + 1)} \left\{ \left(\frac{t'}{t'_T} - v_T\right)^{n+1} - (v_V - v_T)^{n+1} \right\}. \tag{A2}$$

v_1 is obtained by substituting t' by t'_T.

Before the output reaches V_{D0}, the differential equation is simple since the input is constant V_{DD}.

$$\frac{dv_O}{dt'} = -i_5 = -\frac{1 + \lambda' v_O}{1 + \lambda'}. \tag{A3}$$

The initial condition is $v_O = v_1$ at $t' = t'T$ and the solution is

$$\frac{1 + \lambda'}{\lambda'} \log \frac{1 + \lambda' v_O}{1 + \lambda'} = -\frac{t'_T}{(1 - v_T)^n (n + 1)} \left\{ (1 - v_T)^{n-1} - (v_V - v_T)^{n+1} \right\} - (t' - t'_T). \tag{A4}$$

t'_{D0} is obtained by letting v_O go to v_{D0} and is written as follows:

$$t'_{D0} = t'_T \left\{ 1 - \frac{1 - v_T}{n + 1} + \frac{(v_V - v_T)^{n+1}}{(n + 1)(1 - v_T)^n} \right\} - \frac{1 + \lambda'}{\lambda'} \log \frac{1 + \lambda' v_{D0}}{1 + \lambda'}. \tag{A5}$$

During the time after the output reached V_{D0}, where the MOSFET is operating in the linear region

$$\frac{dv_O}{dt'} = -i_3 = -\left(2 - \frac{v_O}{v_{D0}}\right) \frac{v_O}{v_{D0}} \frac{1 + \lambda' v_O}{1 + \lambda'} \tag{A6}$$

is the differential equation to be solved with the initial condition of $v_O = v_{D0}$ at $t' = t'_{D0}$. The solution is

$$t' = t'_{D0} + (1 + \lambda')v_{D0}\left\{\frac{\lambda' v_{D0}}{1 + 2\lambda' v_{D0}} \log \frac{1 + \lambda' v_O}{1 + \lambda' v_{D0}} + \frac{1}{2(1 + 2\lambda' v_{D0})} \log\left(2 - \frac{v_O}{v_{D0}}\right) - \frac{1}{2}\log \frac{v_O}{v_{D0}}\right\}. \quad \text{(A7)}$$

Therefore, the delay $t'_d\ (= t'_{pHL})$ can be expressed as follows:

$$t'_d = t'\left(v_O = \frac{1}{2}\right) - \frac{t'_T}{2} \approx t'_T\left\{\frac{1}{2} - \frac{1 - v_T}{n + 1} + \frac{(v_V - v_T)^{n+1}}{(n + 1)(1 - v_T)^n}\right\} + \frac{1}{2} + \frac{\lambda'}{7}. \quad \text{(A8)}$$

To derive this expression, the complicated term of v_{D0} and λ' in (A5) and (A7) is approximated by $(1/2 + \lambda'/7)$. The error of this approximation is less than 4% when $0.4 < v_{D0} < 0.8$, $0 \le \lambda' < 0.4$. The transition time of the output waveform t'_{TOUT} is calculated by differentiating (A6) and v_O is set equal to 0.5.

When the input is very slow, the output crosses $0.5V_{DD}$ before the input reaches V_{DD}. In this case, (A2) is valid, the delay $t'_d\ (= t'_{05} - 1/2t_T)$ is obtained as

$$t'_d = t'_T\left[v_T - \frac{1}{2} + \left\{(v_V - v_T)^{n+1} - \frac{(1 - v_T)^n (n + 1)}{t'_T}\frac{1 + \lambda'}{\lambda'} \log \frac{2 + \lambda'}{2 + 2\lambda'}\right\}^{1/(n+1)}\right]. \quad \text{(A9)}$$

If the log term in λ' is approximated, the delay expression of (22) can be derived. The error of the approximated formula is less than 4% when $0 \le \lambda' \le 0.4$. t'_{TOUT} is calculated by differentiating (A1) and setting $v_O = 0.5$ and $t' = t'_{05} = t'_d + t'_T/2$. The resultant formula is (23).

The solution for the fast input case, (20), and that for the very slow input case, (22), can be connected at the critical input transition time t'_{T0} given by (19). t'_{T0} can be calculated by equating (20) and (22). It should be noted that not only the values of the both equations but also the first derivatives coincide at the critical time.

Acknowledgment

The encouragement of R. Brayton, A. Sangiovanni-Vincentelli, Y. Unno, Y. Takeishi, Y. Fukuda, H. Yamada, and T. Iizuka throughout the course of this work is greatly appreciated. 0.25-μm MOSFET data were provided by M. C. Jeng and it is gratefully acknowledged together with the fruitful suggestions from him. Assistance provided by H. Ishiuchi, T. Quarles, and R. Spickelmier concerning MOS physics, SPICE, and computer environments is also appreciated.

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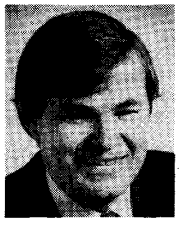

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