A Simplified Method of Generating Thermal Models for Power MOSFETs

Kandarp I. Pandya, Wharton McDaniel Vishay Siliconix 2201 Laurelwood Road. Santa Clara. CA 95054

E-mail: kpandya@vishay.com
Telephone: 408 567 8927

E-mail: wmcdaniel@vishay.com
Telephone: 408 497 5401

Abstract

There is an increasing need for designers to understand the thermal performance of the semiconductors they use because end-product case sizes are shrinking while products' power levels remain the same or increase. A simulation tool such as P-SPICE is the most commonly available tool for engineers to use in performing thermal analysis of semiconductors. However, generating the thermal model for power semiconductors represents a major hurdle in performing such an analysis. A simplified method of model generation is needed.

In this paper an Excel spreadsheet uses datasheet information published by the manufacturer to generate the R-C (resistance-capacitance) parameters for a thermal model. Implementation of the model in P-SPICE enables performance evaluation for any pre-defined operating condition. The intent is to arrive at a fair estimate of the junction temperature of the power-handling device, the MOSFET under transient highpower pulse/s. The explanation of a proposed simplified method of thermal model generation will include an example featuring a power MOSFET.

Introduction

Thermal analysis of a power MOSFET consists of three tasks: (1) developing the thermal characterization of the MOSFET; (2) generating the thermal model; and (3) running a thermal simulation using P-SPICE or a similar platform. Of these three tasks, generation of the thermal model is the most complex process.

Throughout industry and academia, extensive work attempting boundary condition independent (BCI) compact model development has been an ongoing challenge. There are two distinct approaches, one based on empirical data obtained from laboratory studies and the other based on FEA, SUNRED, CFD, or similar simulation results [1,2,3,4]. Accuracy, validation, and acceptance of various approaches have been well-addressed [5].

Practical implementation of analytical approaches requires extensive detail from device manufacturers and their suppliers. Information including the detailed internal and external dimensional structure of the MOSFET and its package, as well as the physical constants of each material used, is necessary for thermal modeling. However, data of this nature – required in the task of calculating the thermal resistance and capacitance of each section separated by different materials – often is not readily available, nor shared easily.

In constructing the thermal model, determining the heat-flow paths as closely as possible to reality is another challenge. Inclusion of multiple heat-flow paths in the thermal model adds a high degree of complexity, and still the model can be found to have holes in it [5]. Finally, the numerous and varied approaches to schematic configuration and simulation produce different end results during analysis.

The average engineer is faced with many time-consuming challenges, one of which is ensuring that the thermal limitations are not exceeded. There is a need for a simplified approach to thermal modeling and simulation that does not require extensive time, knowledge, or access to typically unavailable tools.

Methodology

The proposed simplified method of generating a thermal model employs a curve-fitting technique using the steady-state value of junction-to-case thermal resistance {Rth (j-c)} and the single-pulse curve of the transient thermal impedance characteristics. Both values are readily available in the manufacturer's published datasheet for a given MOSFET. The information is well refined and accepted [6].

Using datapoints from the single-pulse transient thermal impedance curve, an Excel spreadsheet is used to determine the values of four R-C pairs of variables that will generate a new curve matching the single-pulse transient thermal impedance curve shown on the datasheet.

Mathematically, the curve is governed by two equations:

1)
$$RT(t) = R_1(t) * \left(1 - e^{\left(-\frac{t}{\tau_1} \right)} \right) + R_2(t) * \left(1 - e^{\left(-\frac{t}{\tau_2} \right)} \right)$$
$$+ R_3(t) * \left(1 - e^{\left(-\frac{t}{\tau_3} \right)} \right) + R_4(t) * \left(1 - e^{\left(-\frac{t}{\tau_4} \right)} \right)$$

and

$$(C_x = \frac{\tau_x}{R_x})$$

RT is the steady-state value of thermal resistance junctionto- case {Rth (j-c)}. Rx and Cx are the R-C values generated by the spreadsheet. These variable-pairs represent thermal resistance and capacitance of the MOSFET assembly. The Excel spreadsheet plots both curves on one chart to facilitate comparison and to allow fine-tuning of the curve-fit through tweaking of the limits of variables (R-C).

Copyright © 2004 IEEE. Reprinted from the proceedings of IEEE SemiTherm XVIII, March 12-14, 2002, San Jose, Calif. This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Vishay Intertechnology, Inc.'s products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org. By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

The present exponential curve-fit routine leads to a Foster-type configuration for a thermal equivalent circuit in P-SPICE. Practical validation of the claim that the variable-pairs represent the thermal performance of the MOSFET assembly comes from the transient response curve generated by step input in the P-SPICE schematic circuit. This curve closely matches the transient thermal impedance curve of the MOSFET datasheet. For all practical purposes, this validates the P-SPICE schematic for use in thermal analysis.

A Practical Example

In this example a thermal model is developed for a D²PAK Power MOSFET, Vishay Siliconix part number SUB75N03-04. This process uses the datasheet information for the device and Excel spreadsheet-developed model generation. Figures 3 and 4 show the spreadsheet at various stages of the process.

Step 1

Get the datasheet for the SUB75N03-04. The thermal resistance ratings table (Figure 1) from the datasheet identifies the junction-to-case thermal resistance ($R\theta_{jc}$) as being 0.6°C/W. This value is entered into the spreadsheet and is used to change the normalized thermal impedance values to absolute values.

Step 2

Thirteen datapoints are taken from the transient thermal impedance curve (Figure 2) and entered into the Excel

spreadsheet to create the baseline curve for the curvematching process. The datapoints consist of thermal resistance and its corresponding time. Single Pulse Thermal Impedance curve is reproduced. However, at this point the R-

C variables are blank in the Excel spreadsheet (Figure 3).

Step 3

The values of the four-element R-C model are manipulated to cause the model's curve to fit the curve from the datasheet. As this can be a time-consuming step when done manually, the spreadsheet has been designed to perform this function automatically. In Figure 4, the R-C values have been calculated to fit the curve and are displayed in the corresponding cells.

Step 4

Figure 5 shows the P-SPICE schematic diagram of the thermal model. The R-C values generated by the Excel spreadsheet have been entered into the schematic. The voltage source V1 corresponds to the case temperature. Current source I10 represents the power dissipated in the device. The power profile is defined in the stimulus file. The junction temperature of the MOSFET is represented by the value of voltage, V, on Cth1.

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263)d	R _{thJA}	40	° C/W
	Free Air (TO-220AB)		62.5	
Junction-to-Case		R _{thJC}	0.6	

Figure 1: Thermal Ratings From the Datasheet

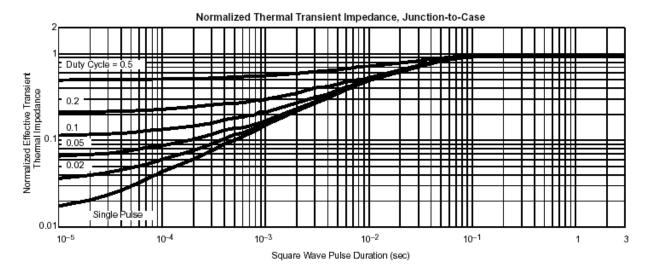


Figure 2: Transient Thermal Impedance Curve From the Datasheet

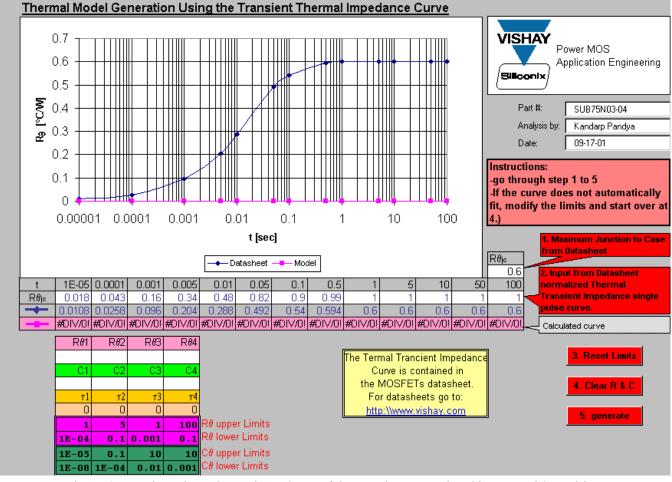


Figure: 3 Transient Thermal Impedance Curve of the Datasheet Reproduced in an Excel Spreadsheet

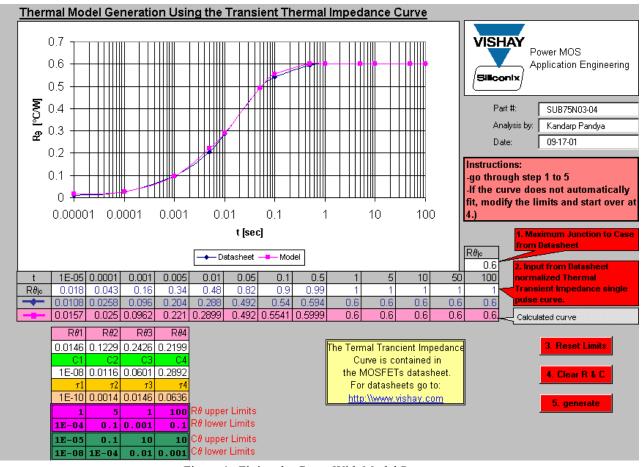
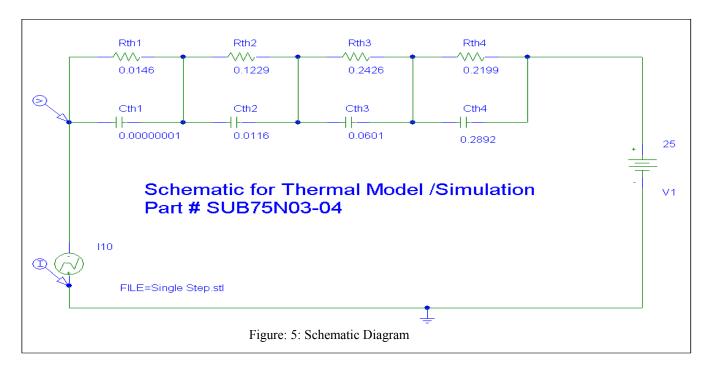


Figure 4: Fitting the Curve With Model Parameters



SUB75N03-04 Transient Thermal Impedance

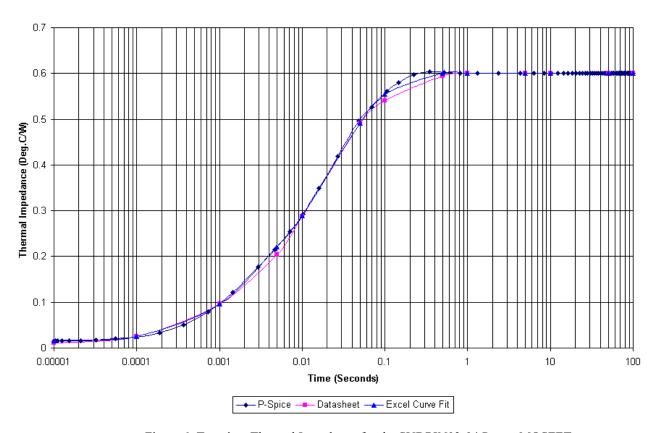


Figure 6: Transient Thermal Impedance for the SUB75N03-04 Power MOSFET

Step 5

Simulation with step-input stimulus produces a transient impedance curve for the circuit. Figure 6 shows the P-SPICE-generated curve along with the datasheet and Excel spreadsheet curves on one chart. The close fit of the P-SPICE curve to the datasheet curve validates the thermal model shown in Figure 5.

This circuit can be used with any power profile to study the thermal behavior of the MOSFET. An example is shown in Figure 7. The power pulse profile starts with a maximum amplitude of 525 W for 0.5 milliseconds, tapering down to 13 W in 40 milliseconds. The MOSFET junction temperature starts with a temperature of 25°C and rises to a maximum value of 98°C at 13.5 milliseconds.



Figure 7: Power Pulse Profile

Versatility

There are two very valuable aspects of this method of thermal modeling:

- 1) This thermal modeling approach is independent of type of package. The only information required, the transient thermal impedance curve, which characterizes the package in total, is available in the datasheet.
- 2) The model can be extended easily to include the effects of other components such as the PC board and/or heat-sink assembly. Once transient thermal characterization including additional elements is performed, the curve-fitting method of model generation can be used.

Conclusion

A simple method of generating a thermal model for a power MOSFET has been presented. The requirements for this model are readily available information from the device datasheet and commonly available tools such as Excel and P-SPICE. The validity of this simple approach is based on the model's ability to reproduce the published thermal characterization curve. Finally, this approach fulfills the need for a method of generating thermal models without requiring extensive time, knowledge, or access to typically unavailable tools.

References

- M. Rencz, V. Szekely: "A Generic Method for Thermal Multiport Model Generation of IC Packages," 17th IEEE SEMI-THERM Symposium
- H. Pape, G. Noebauer: "Generation and Verification of Boundary Independent Compact Thermal Model for Active Components According to the DELPHI/SEED Methods," SEMI-THERM '99
- Wataru Nakayama: "Emerging New Roles of CFD Simulation in Competitive Market Environment," 7th THERMINIC 2001 Workshop
- Bartosz Maj, Adam Augustin, Arno Kostka: "Heat Propagation in H-Bridge Smart Power Chips Under Switching Conditions," 7th THERMINIC 2001, Workshop
- Clemens J. M. Lasance: "The Conceivable Accuracy of Experimental and Numerical Thermal Analyses of Electronic Systems," 17th IEEE SEMI-THERM Symposium
- V. Szekely, M. Rencz, L. Pohl: "Novelties in the theory and Practice of Thermal Transient Measurements," 7th THERMINIC 2001, Workshop