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A Simplified Model Predictive Control for T-Type Inverter with Output LC Filter

Van-Quang-Binh Ngo ^{1,2} , Minh-Khai Nguyen ³ , Tan-Tai Tran ¹  and Young-Cheol Lim ¹ and Joon-Ho Choi ^{1,*}

¹ Department of Electrical Engineering, Chonnam National University, Gwangju 500-757, Korea; qbinhtam@gmail.com (V.-Q.-B.N.); trantantaikdd@gmail.com (T.-T.T.); yclim@chonnam.ac.kr (Y.-C.L.)

² Department of Physics, College of Education, Hue University, Thua Thien Hue 530000, Vietnam

³ Department of Electrical Engineering, Chosun University, Gwangju 61452, Korea; nmkhai00@gmail.com

* Correspondence: joono@chonnam.ac.kr

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Abstract: In this paper, a model predictive control scheme for the T-type inverter with an output LC filter is presented. A simplified dynamics model is proposed to reduce the number of the measurement and control variables, resulting in a decrease in the cost and complexity of the system. Furthermore, the main contribution of the paper is the approach to evaluate the cost function. By employing the selection of sector information distribution in the reference inverter voltage and capacitor voltage balancing, the execution time of the proposed algorithm is significantly reduced by 36% compared with conventional model predictive control without too much impact on control performance. Simulation and experimental results are studied and compared with conventional finite control set model predictive control to validate the effectiveness of the proposed method.

Keywords: finite control set model predictive control; T-type inverter; computational cost; LC filter; DC-link capacitor voltage balancing

1. Introduction

Recently, the multilevel converter has been widely applied to various applications such as renewable energy system, flexible AC transmission systems and electric drives thanks to its benefits: increase the power capacity of the converter and improve the quality of the system [1–3]. In particular, compared with the neutral-point-clamped (NPC) type, the T-type inverter topology has the advantage in terms of the efficiency for medium switching frequency [4–6]. Thus, the T-type inverter is considered to be an alternative solution for multilevel inverter. Like the NPC converter, the unbalance of neutral-point potential is the drawback of this topology which causes the distortion of the output voltage and current. However, several approaches have been introduced to solve this problem [7–10].

A linear controller with proportional-integral (PI) is typically applied to control the converter because of its simplicity and stability [11,12]. However, this approach has a low dynamic response and requires a complex modulation technique for balancing the DC-link capacitor voltage. Recently, direct power control [13] which uses a switching look-up table for determining the switching state has been introduced to improve the performance. Nonetheless, it requires a high sampling frequency to achieve an acceptable steady-state and high dynamic performances. To deal with this disadvantage, several control approaches have been proposed such as using direct power control with space vector modulation [14], fuzzy control [15], sliding mode control [16], and predictive control [17–19].

In recent years, a finite control set model predictive control (FCS-MPC) is considered as an attractive alternative control strategy for power converters due to its simple structure, facilitating implementation, and fast dynamic response [20–25]. Furthermore, compared with classical control,

the FCS-MPC provides the advantages such as easy inclusion of nonlinearities and constraints in the controller. However, at each sampling period, the prediction of control variables is 27, corresponding to the three-level T-type inverter, leading to producing a high computational cost. In [26], a simplified FCS-MPC for three-level voltage source converter is introduced. In order to reduce the computational time, this approach used the two-level switching state group for prediction and optimization. Another approach is presented in [27], which employs equivalent transformations in the cost function for the optimization loop. Another approach is proposed in [28,29] based on using a modified sphere decoding algorithm for multilevel converters. In [30], a sector distribution and non-zero voltage vectors are exploited with the aim to reduce the computational burden for two-level converters. Nonetheless, the main disadvantage of this method is the nonexistence of zero voltage leading to an increase of the total harmonic distortion (THD) in the load current. In [31], the control approach is suggested based on the candidate region that minimizes the sub-cost function to reduce the execution time. The presented technique in [32] combined the conventional FCS-MPC, a look-up table, and steady-state evaluation to reduce the computational burden. However, this algorithm can have a large amount of computational cost like the conventional FCS-MPC in the worst case.

With a three-level T-type inverter, control variables are predicted by using the predictive model and measured variables such as DC-link capacitor voltage, output voltage, filter current, and output current. In order to reduce the cost and complexity of this system, a simplified dynamics model is presented in this paper. Moreover, the highlight of this research is the significant computational cost reduction without decreasing the quality of control by preselecting the required inverter output voltage. The balance of DC-link capacitor voltage is guaranteed by determining the suitable small voltage vectors resulting in the elimination of the weighting factor in the cost function. As a consequence, the amount of predictive state for loop optimization is reduced from 27 to 6 compared with the conventional FCS-MPC method. This means that it is easy to implement the proposed algorithm in a real-time system with a low-cost processor and to extend with a long prediction horizon for improving the control performance. The simulation and experimental results validate the effectiveness of the proposed control strategy.

The rest of this paper is organized as follows: a reduced model predictive control for the three-level T-type inverter is presented in Section 2. Next, the proposed algorithm is explained in Section 3 for reducing the computational cost. In Section 4, a comparative study of the conventional FCS-MPC and the proposed method is examined. Finally, the conclusions are given in Section 5.

2. Model Predictive Control for a Three-Level T-Type Inverter

2.1. Topology

A simple topology of the three-level T-type inverter (3L-T-type) is shown in Figure 1. The basic principle of this configuration can be expressed by three switching states [P], [N] and [O] which correspond to three inverter output voltages $+U_{dc}/2$, $-U_{dc}/2$ and 0. Consequently, 27 possible switching configurations are considered for a 3L-T-type inverter. Table 1 presents the summary of the operating principle for 3L-T-type.

Table 1. Operating status of inverter leg $x \in \{a, b, c\}$.

State	Switch				Inverter Output Voltage
	S_{1x}	S_{2x}	S_{3x}	S_{4x}	
P	1	1	0	0	$U_{dc}/2$
O	0	1	1	0	0
N	0	0	1	1	$-U_{dc}/2$

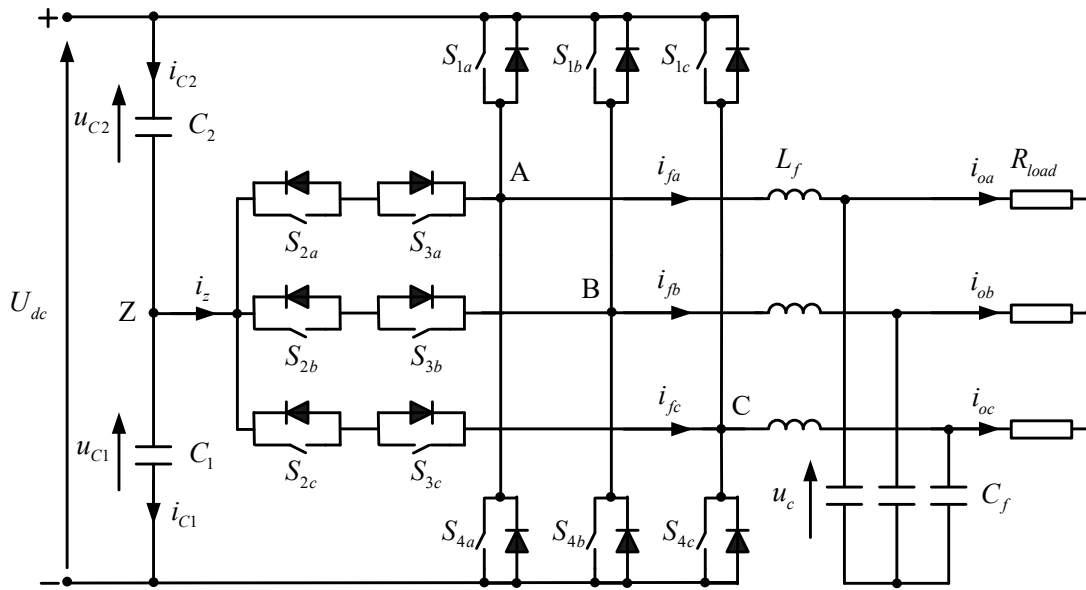


Figure 1. Three-level T-type inverter topology.

2.2. Mathematical Modeling of the System

The inverter output voltage produced by the 3L-T-type inverter is given by:

$$u_{inv} = \frac{2}{3} \left(u_{AZ} + k u_{BZ} + k^2 u_{CZ} \right), \tag{1}$$

where u_{AZ} , u_{BZ} , and u_{CZ} are the output phase voltages; $k = e^{j2\pi/3} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$.

The phase voltage u_{xZ} is calculated in terms of DC-link voltage U_{dc} and switching state S_x as [9,22]:

$$u_{xZ} = S_x \frac{U_{dc}}{2}, \tag{2}$$

where S_x represents the switching status and has three possible values: $\{-1, 0, 1\}$ with the index $x \in \{a, b, c\}$.

The dynamic behavior of LC filter can be described by the following:

$$\begin{aligned} L_f \frac{di_f}{dt} &= u_{inv} - u_c, \\ C_f \frac{du_c}{dt} &= i_f - i_o, \end{aligned} \tag{3}$$

where u_{inv} and u_c are the inverter and output capacitor voltage vectors; i_f and i_o are the filter and output load current vectors and L_f , C_f are the filter inductance and capacitance.

The control variables u_c and i_f are measured while u_{inv} is obtained from Equations (1) and (2). In general, i_o is measured or estimated by using an observer, leading to an increase in the cost and complexity of the system. In this paper, to achieve a simple model, we assume that the output load current is derived from output capacitor voltage. Thus, Equation (3) is rewritten as:

$$\begin{aligned} \frac{du_c}{dt} &= \frac{1}{C_f} \left(i_f - \frac{u_c}{R_{Load}} \right), \\ \frac{di_f}{dt} &= \frac{1}{L_f} (u_{inv} - u_c), \end{aligned} \tag{4}$$

where R_{load} is the load resistance.

In order to reduce the number of the control variable, the neutral-point voltage is taken into account in the model instead of two capacitor voltages (u_{C1} , u_{C2}). The neutral-point voltage (u_z) can be expressed based on the assumption that the DC-link voltage is kept constant and $C_1 = C_2 = C$ as follows:

$$\frac{du_z}{dt} = \frac{d(u_{C1} - u_{C2})}{dt} = -\frac{1}{C}i_z = -\frac{1}{C}\left((1 - |S_a|)i_{fa} + (1 - |S_b|)i_{fb} + (1 - |S_c|)i_{fc}\right). \quad (5)$$

Consequently, we have a representation of the dynamics model based on Equations (4) and (5) as:

$$\begin{aligned} \frac{du_c}{dt} &= \frac{1}{C_f} \left(i_f - \frac{u_c}{R_{Load}} \right), \\ \frac{di_f}{dt} &= \frac{1}{L_f} (u_{inv} - u_c), \\ \frac{du_z}{dt} &= -\frac{1}{C} \left((1 - |S_a|)i_{fa} + (1 - |S_b|)i_{fb} + (1 - |S_c|)i_{fc} \right). \end{aligned} \quad (6)$$

3. Model Predictive Control with Selection Sector Distribution

The main goal of the proposed control scheme is to minimize the error between the predicted output voltage and its reference value and to maintain capacitor voltage balancing. Furthermore, additional terms can be taken into account in the objective function such as switching frequency, current limitation, but this is not the main focus of this research and will not be developed here. As a result, the cost function for 3L-T-type inverter is expressed as [21–23]:

$$g = \left| u_{c\alpha}^*(k+1) - u_{c\alpha}^p(k+1) \right| + \left| u_{c\beta}^*(k+1) - u_{c\beta}^p(k+1) \right| + \lambda_{uz} \left| u_z^p(k+1) \right|, \quad (7)$$

where $u_{c\alpha}^*(k+1)$, $u_{c\beta}^*(k+1)$ and $u_{c\alpha}^p(k+1)$, $u_{c\beta}^p(k+1)$ indicate the real and imaginary components of the reference and predicted output capacitor voltages at instant $k+1$, respectively. λ_{uz} is the weighting factors of the capacitor voltage balancing.

To achieve the discrete-time model, the first-order Euler approximation is used as:

$$\frac{dx}{dt} = \frac{x(k) - x(k-1)}{T_s}, \quad (8)$$

where T_s is the sampling time.

By approximating Equation (6) with Equation (8), the discrete-time representation of output capacitor voltage can be obtained as:

$$u_c(k) = \frac{T_s R_{Load}}{C_f R_{Load} + T_s} i_f(k) + \frac{C_f R_{Load}}{C_f R_{Load} + T_s} u_c(k-1). \quad (9)$$

By shifting the output voltage in Equation (9) into one future sample, we have the predicted output voltage at instant $k+1$:

$$u_c^p(k+1) = \frac{T_s R_{Load}}{C_f R_{Load} + T_s} i_f^p(k+1) + \frac{C_f R_{Load}}{C_f R_{Load} + T_s} u_c(k). \quad (10)$$

The discrete-time form for the filter current is given by using the forward Euler approximation as:

$$i_f^p(k+1) = i_f(k) + \frac{T_s}{L_f} (u_{inv}(k) - u_c(k)). \quad (11)$$

Similarly, the discrete-time of neutral-point potential is expressed by:

$$u_z^p(k+1) = u_z(k) - \frac{T_s}{C} \left((1 - |S_a|) i_{fa}(k) + (1 - |S_b|) i_{fb}(k) + (1 - |S_c|) i_{fc}(k) \right). \quad (12)$$

Substituting Equation (11) into Equation (10), the predicted output voltage is rewritten as:

$$u_c^p(k+1) = \frac{T_s R_{load}}{C_f R_{load} + T_s} i_f(k) + \frac{T_s^2 R_{load}}{L_f (C_f R_{load} + T_s)} u_{inv}(k) + \frac{R_{load}}{C_f R_{load} + T_s} \left(C_f - \frac{T_s^2}{L_f} \right) u_c(k). \quad (13)$$

A control input is a sequential switch state $S_p = [S_{pa} \ S_{pb} \ S_{pc}]^T$, symbolized as a set of p vector $S_p \in \{1, \dots, 27\}$. Furthermore, the switching inputs a finite set: $S_{px} \in \{-1, 0, 1\}$ with the index $x \in \{a, b, c\}$. As a result, the optimal switching input S_{opt} is achieved as the result of Equation (14):

$$S_{opt} = \arg \{ \min g \}, \quad p = 1, \dots, 27 \\ \text{subject to (7), (12) and (13)}. \quad (14)$$

The space voltage vector of 3L-T-type inverter can be classified into four groups: zero vectors (from u_{25} to u_{27}), small vectors (from u_{13} to u_{24}), medium vectors ($u_2, u_4, u_6, u_8, u_{10}$, and u_{12}) and large vectors (u_1, u_3, u_5, u_7 and u_9), wherein the small vectors are divided into two types: positive state (P) and negative state (N) such as u_{14} and u_{13} , respectively. The neutral-point voltage is increased with the positive state and decreased with the negative state, respectively [33]. The zero, medium and large vectors do not affect the neutral-point voltage deviation. In the conventional FCS-MPC, the capacitor voltage balancing can be solved by adjusting the weighting factor in the cost function. However, it is not easy to obtain the optimal weighting factor value leading to affecting the THD of the load current. In this study, the capacitor voltages are balanced by selecting the suitable small vectors that depend on the predicted neutral-point voltage. Therefore, the proposed method is simple due to no requirement of the weighting factor for balancing capacitor voltages in the cost function.

For the 3L-T-type inverter, 27 switching states are considered to evaluate the cost function. Long prediction horizon can improve the control performance. However, the computational cost is increased exponentially corresponding to the prediction horizon. Therefore, it leads to a large computational cost which makes it difficult to implement the algorithm in common digital signal processing. In this paper, the selection of sector distribution is employed with the aim to solve this problem. The main idea of the proposed method is to determine the position of inverter reference voltage which is obtained from the predictive model. In this case, the required inverter voltage $u_{inv}^*(k)$ is achieved based on Equation (13) by replacing the predicted output voltage $u_c^p(k+1)$ with its reference. Then, the location of the reference voltage $u_{inv}^*(k)$ is determined by its components $u_{inv\alpha}^*$ and $u_{inv\beta}^*$. In the proposed method, we divide the space vector of the 3L T-type inverter into six sectors as illustrated in Figure 2. For example, when the reference voltage $u_{inv}^*(k)$ is in sector I, there are only 10 voltage vectors which are selected for the evaluation of the cost function. As previously discussed, the neutral-point voltage is predicted based on the previous optimal switching states and filter currents by using Equation (5). In order to achieve the balance of capacitor voltages, two cases are considered: the first one corresponds to $u_z \leq 0$ and the second one to $u_z > 0$. The positive small vectors (u_{14}, u_{15}) and negative small vectors (u_{13}, u_{16}) are considered with the condition $u_z \leq 0$ and $u_z > 0$, respectively. Zero vectors can reduce from 3 to 1 due to the same value and without the effect of voltage imbalance. In this case, the feasible voltage vectors are $u_1, u_2, u_3, u_{14}, u_{15}, u_{25}$ for $u_z \leq 0$, whereas they are $u_1, u_2, u_3, u_{13}, u_{16}, u_{25}$ for $u_z > 0$, respectively. Table 2 illustrates the available inverter voltage vectors for a 3L-type inverter after obtaining the appropriate sector. Thus, the prediction of the control variable for cost function loop optimization is decreased from 27 to 6 with the proposed method. As a result, compared with the conventional FCS-MPC method, the computational cost is appreciably reduced by about 77% in the proposed algorithm. It is obvious that this advantage is more attractive to real-time

implementation with low-cost digital hardware and long prediction horizon. The overall control strategy of the proposed method is shown in Figure 3. Then, the optimal switching state is applied to the inverter by minimizing this cost function:

$$g_{mdf} = \left| u_{c\alpha}^*(k+1) - u_{c\alpha}^p(k+1) \right| + \left| u_{c\beta}^*(k+1) - u_{c\beta}^p(k+1) \right|, \tag{15}$$

$$S_{opt} = \arg\{\min g_{mdf}\}, \quad p = 1, \dots, 6.$$

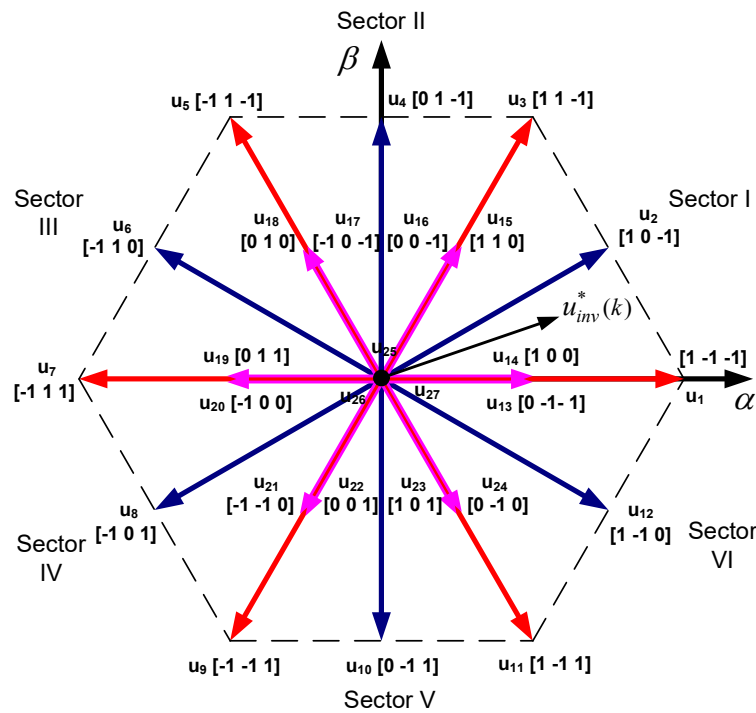


Figure 2. Voltage vectors distribution of T-type inverter.

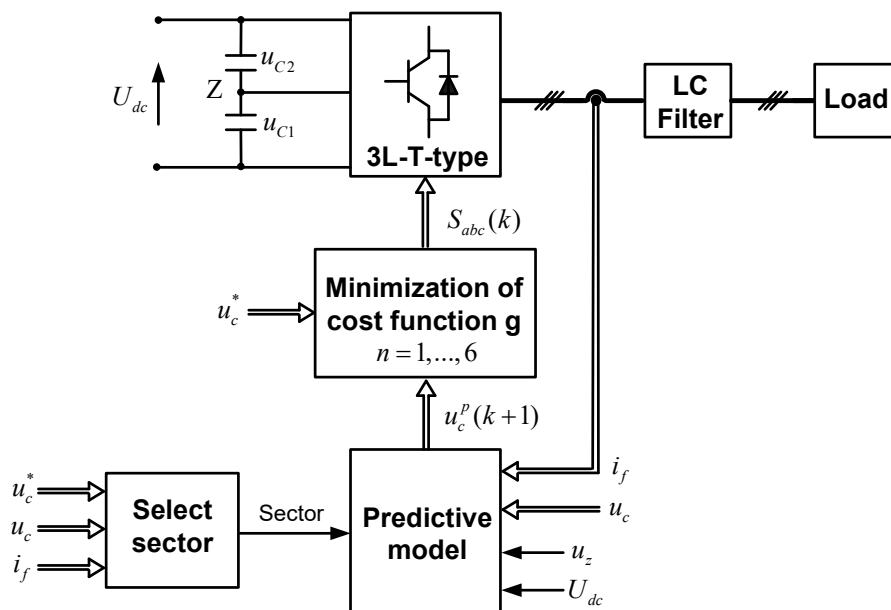
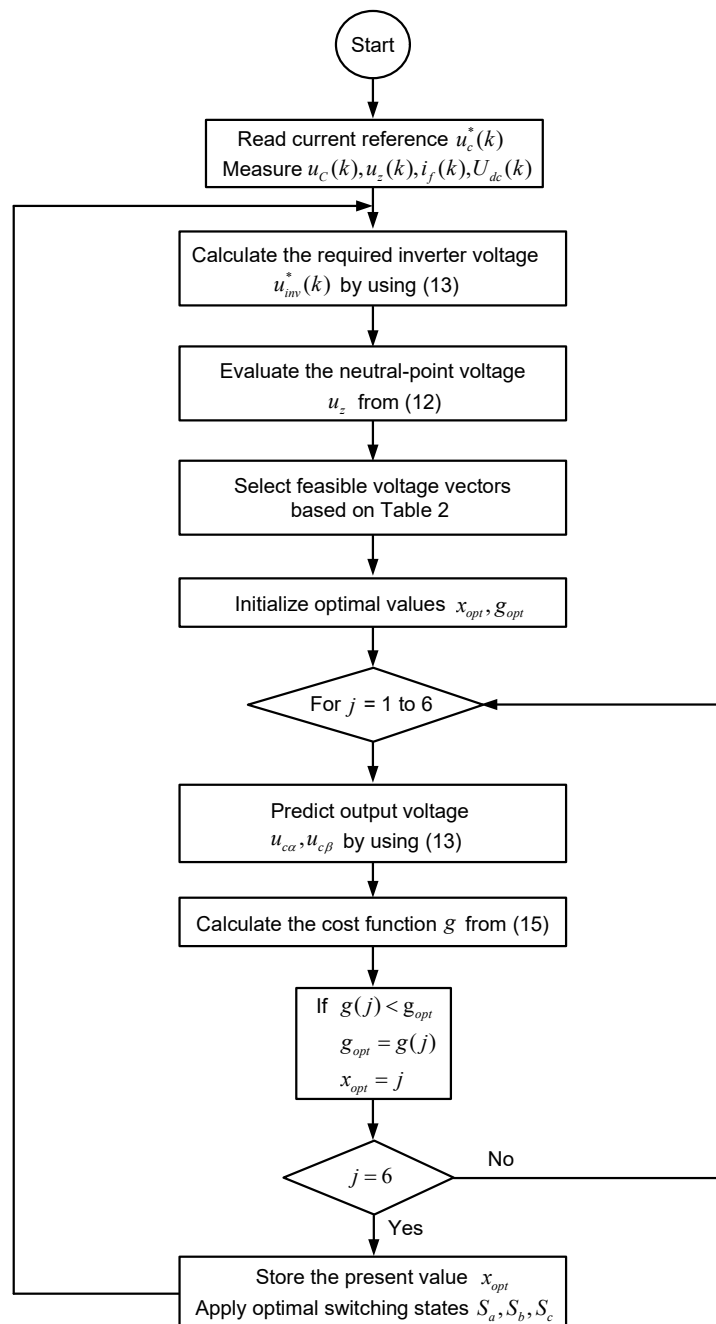


Figure 3. Block diagram of the proposed control strategy.

Table 2. Feasible voltage vectors for each sector.

Sector	Feasible Voltage Vectors	
	$u_z \leq 0$	$u_z > 0$
I	$u_1, u_2, u_3, u_{14}, u_{15}, u_{25}$	$u_1, u_2, u_3, u_{13}, u_{16}, u_{25}$
II	$u_3, u_4, u_5, u_{15}, u_{18}, u_{25}$	$u_3, u_4, u_5, u_{16}, u_{17}, u_{25}$
III	$u_5, u_6, u_7, u_{18}, u_{19}, u_{25}$	$u_5, u_6, u_7, u_{17}, u_{20}, u_{25}$
IV	$u_7, u_8, u_9, u_{19}, u_{22}, u_{25}$	$u_7, u_8, u_9, u_{20}, u_{21}, u_{25}$
V	$u_9, u_{10}, u_{11}, u_{22}, u_{23}, u_{25}$	$u_9, u_{10}, u_{11}, u_{21}, u_{24}, u_{25}$
VI	$u_{11}, u_{12}, u_1, u_{23}, u_{14}, u_{25}$	$u_{11}, u_{12}, u_1, u_{24}, u_{13}, u_{25}$

Finally, the proposed control algorithm is described in Figure 4.

**Figure 4.** Flowchart of the proposed control strategy.

4. Simulation and Experimental Results

4.1. Simulation Results

Simulation analyses were performed in a Matlab/Simulink environment with version 2015a to verify the control performance of the proposed strategy for the T-type inverter as illustrated in Figure 5. The SimPowerSystems toolbox was used to create the 3L-T-type inverter with output LC filter. The Matlab Function block is employed to easily implement the control algorithm in the simulation environment. The parameters of the system are listed in Table 3.

Table 3. System parameters.

Parameter	Value	Description
U_{dc}	600 [V]	DC-link voltage
C	1000 [μ F]	DC-link capacitance
L_f	3 [mH]	Filter inductance
C_f	40 [μ F]	Filter capacitance
R_{load}	20 [Ω]	Load resistance
f_s	20 [kHz]	Sampling frequency
f	50 [Hz]	Frequency of the grid

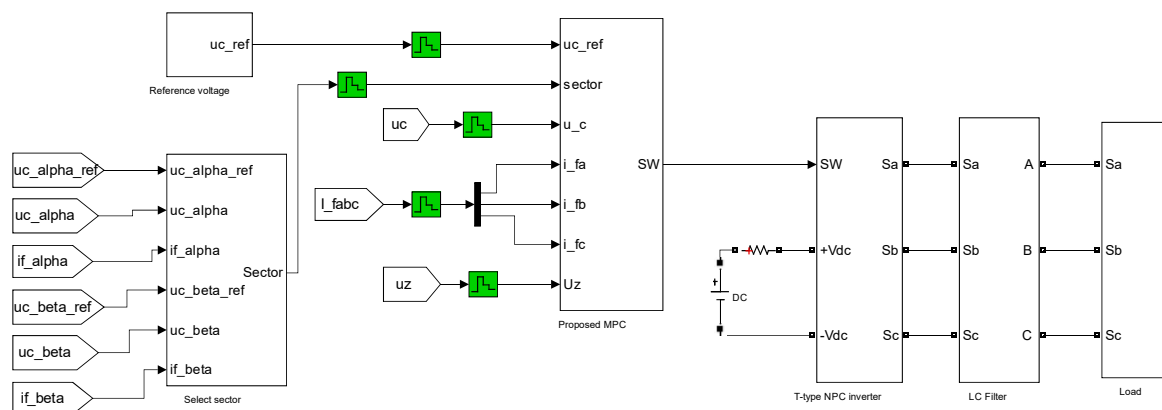


Figure 5. Block diagram of the proposed strategy in Matlab/Simulink.

Figure 6 shows the steady-state of the proposed method with the output voltage at 155 V. As depicted in Figure 6, the proposed method obtains the sinusoidal output voltage and the balance of DC-link capacitor voltage. The characteristic of the variable switching frequency is illustrated in Figure 6c. This can increase the THD of the load current, but this does not affect the control performance too much. The THD of the load current can receive further improvements by using alternative methods. However, this is not the main focus of this paper and will not be developed here.

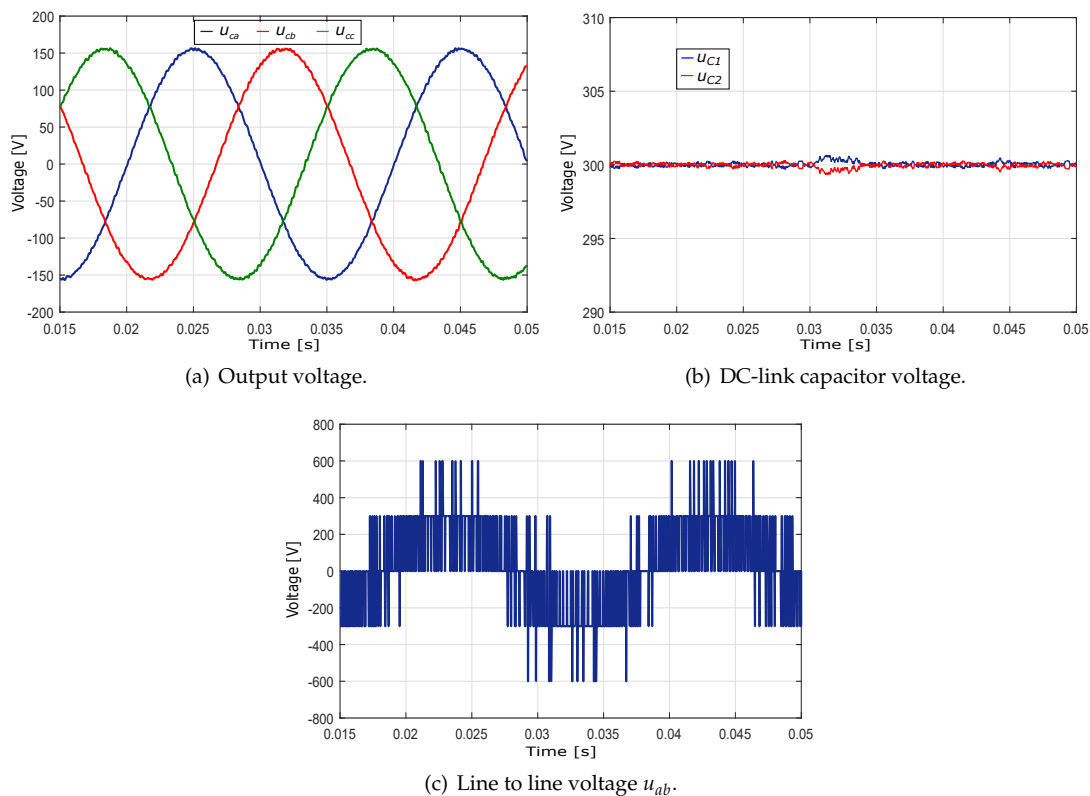


Figure 6. Steady-state of the proposed method at the output voltage of 155 V.

In order to show the efficiency of the control strategy, a comparison between the proposed method and the conventional FCS-MPC [23] were carried out under different operating conditions and the same parameters. The amplitude of the reference voltage changed from 155 to 311 V in the first scenario and stepped from 311 to 155 V at $t = 0.03$ s in the second scenario as illustrated in Figures 7 and 8. The corresponding dynamic current response is shown in Figures 7b and 8b. As can be seen, it is clear that the proposed method achieves sinusoidal current with the different reference amplitude. In addition, one important issue associated with the T-type inverter is the balance of DC-link capacitor voltage. Figures 7c and 8c indicate that the voltage of the DC-link capacitor is balanced despite the change in reference. The maximum absolute error of this voltage at steady-state are about 1 and 3 V for output voltage of 155 and 311 V, respectively. Figure 9 demonstrates single phase output voltage of the proposed and conventional FCS-MPC methods. The simulation results indicate the ability of the proposed method to accurately track and accomplish the steady-state with a fast dynamic response.

With the aim to evaluate the steady-state performance, the harmonic spectra of load current for the conventional FCS-MPC and proposed methods are also examined in Figure 10a,b. These figures show that the THD of the load current is increased slightly from 0.45% to 0.58% with the proposed method. The comparison of two control methods is summarized in Table 4. Although the THD of the load current is not perfect, we nevertheless believe that the slight increase does not affect the control performance too much. Specifically, the computation time of the proposed algorithm is greatly reduced compared with the conventional FCS-MPC as shown in Figure 11a. In fact, the minimum, average and maximum computation times of the proposed algorithm are 3, 6 and 9 μ s in a 2.0 GHz, i5 4310 CPU, while their corresponding values are 4, 10 and 16 μ s with conventional FCS-MPC. The performance of FCS-MPC method is influenced by the sampling time which is improved by choosing the smaller value. To investigate the effect of sampling time on the quality of the current, two controllers are employed with different sampling times. Figure 11b shows that the quality of load current is the best with sampling time 40 μ s and the worst with 100 μ s. However, there is a limitation of sampling time due to the requirement of execution time such as computation time and measurement of the signal.

Therefore, this method exhibits a valuable alternative to reduce the sampling time and extend with a long prediction horizon, which improves the control performance.

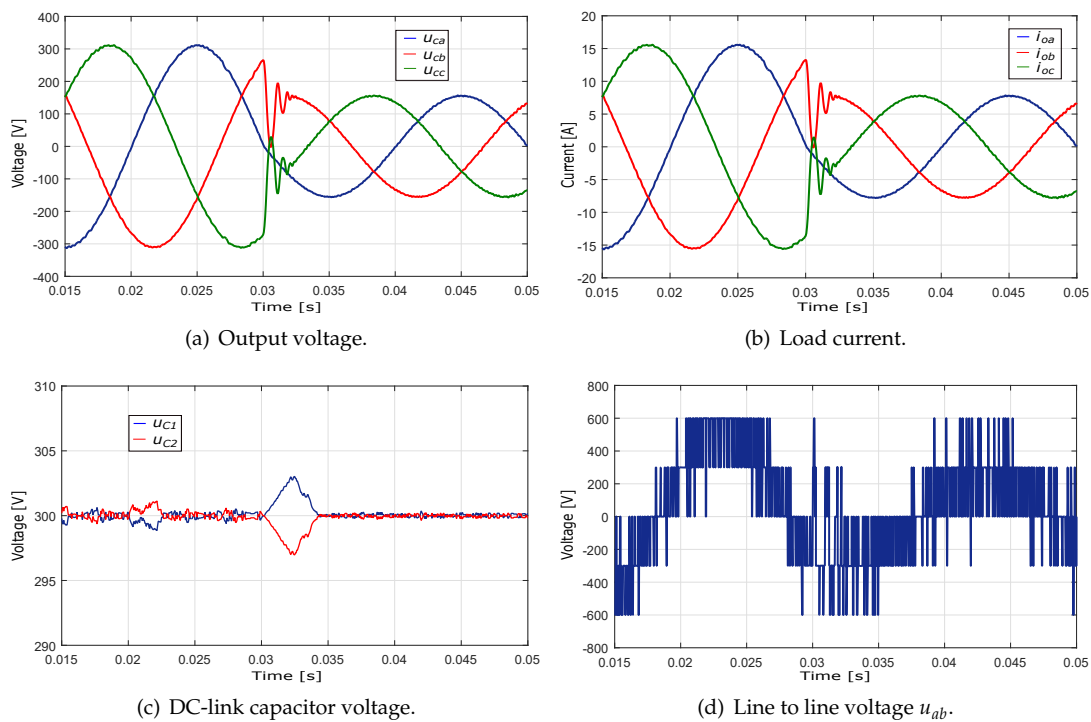


Figure 7. The dynamic response of the proposed method for step change from 311 to 155 V.

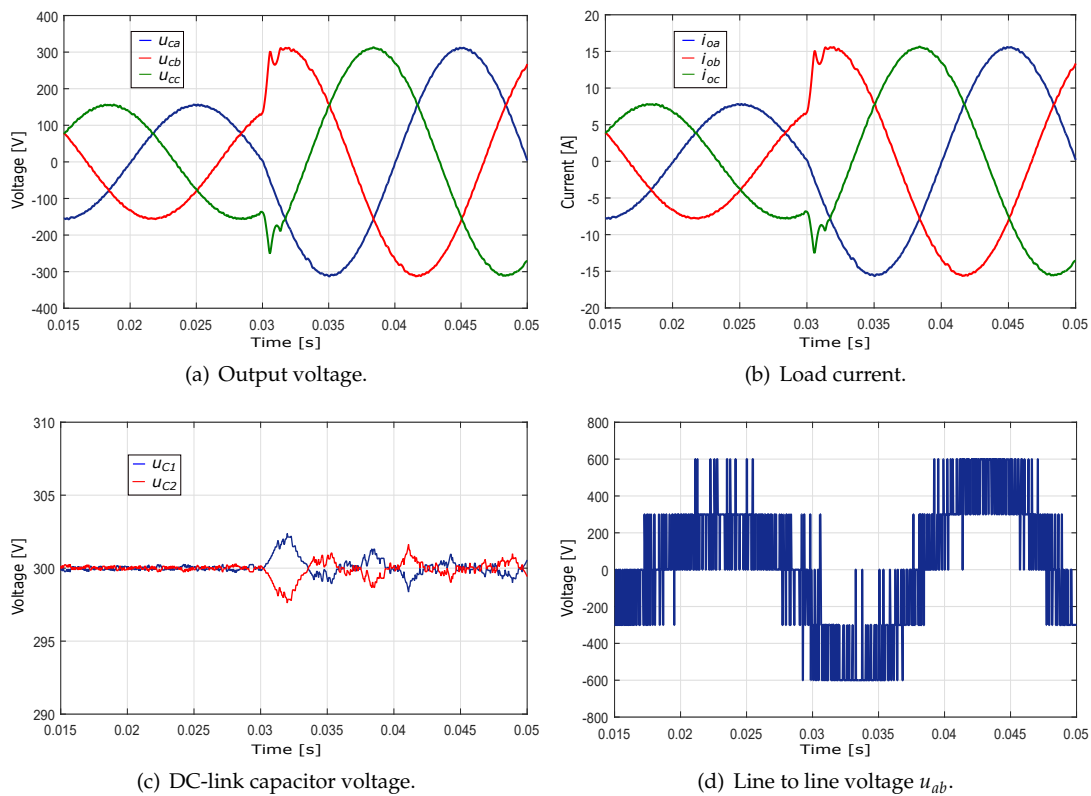


Figure 8. The dynamic response of the proposed method for step change from 155 to 311 V.

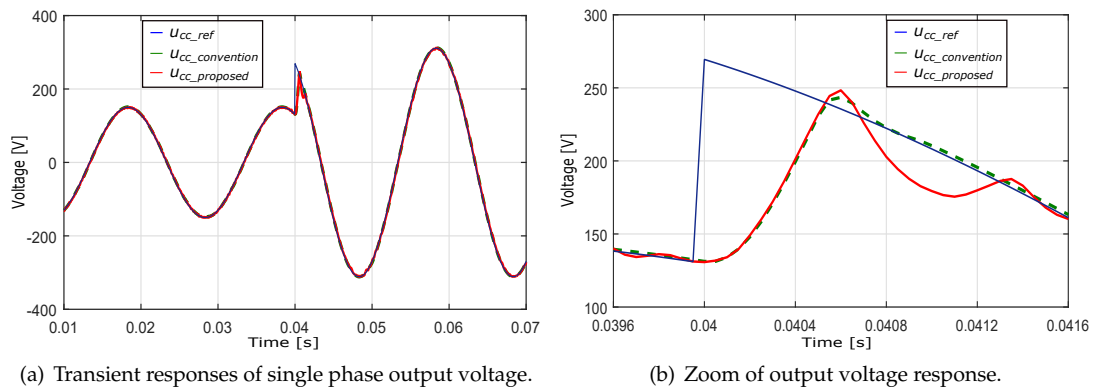


Figure 9. The dynamic response of the output voltage for the conventional FCS-MPC and proposed methods.

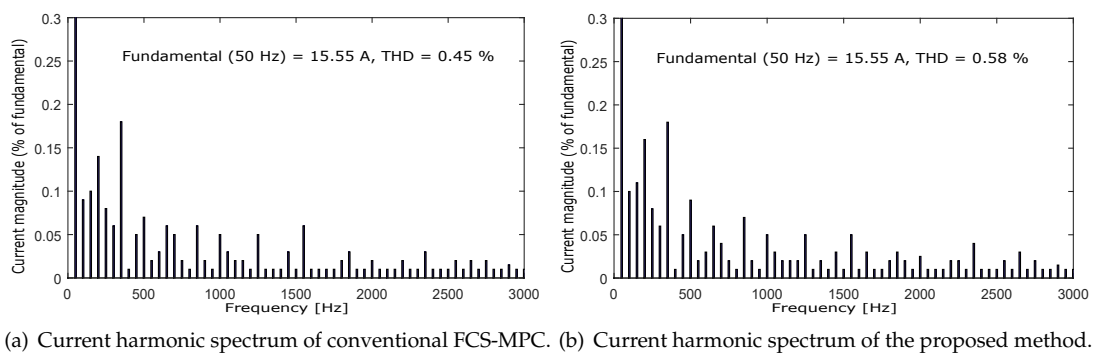


Figure 10. The harmonic spectrum of the load current for the conventional FCS-MPC and proposed methods.

Table 4. Comparison of transient performance for two controllers.

Reference Step	$u_c^* = 155 \rightarrow 311$ (V)	
	Conventional FCS-MPC	Proposed Method
State of loop optimization	27	6
Rise time (ms)	0.5	0.5
Settling time (ms)	0.7	1.3
THD of current (%)	0.45	0.58

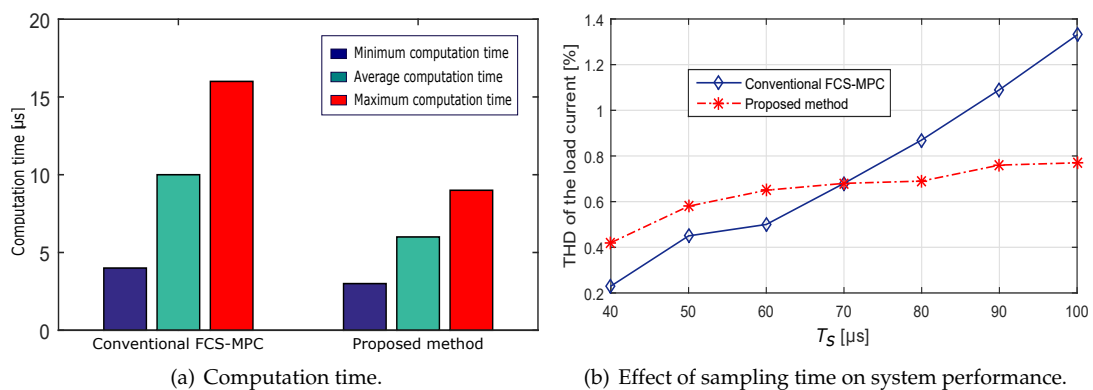


Figure 11. Comparison of two control methods.

The behavior of the system is also examined under time varying load step as illustrated in Figure 12. At the initial state, the system operates at no load condition; then, the load is set to 20 Ω at

$t = 0.02$ s. According to Figure 12, this change does not impact on the quality of the output voltages. A resistive-inductive load is imposed for the same test as shown in Figure 13. The load resistance and inductance are set to 40Ω and 10 mH, respectively. It can be seen from Figure 13 that no deterioration of output voltage is observed in this case.

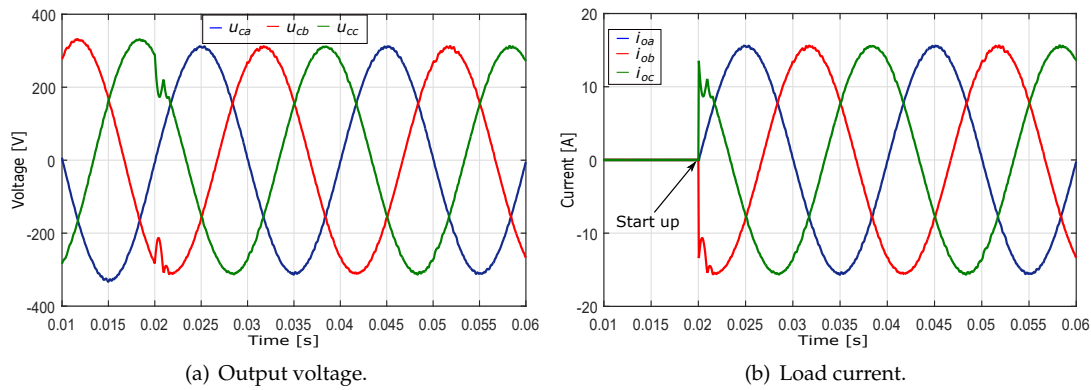


Figure 12. Output voltage and current with the resistive load step at $t = 0.02$ s.

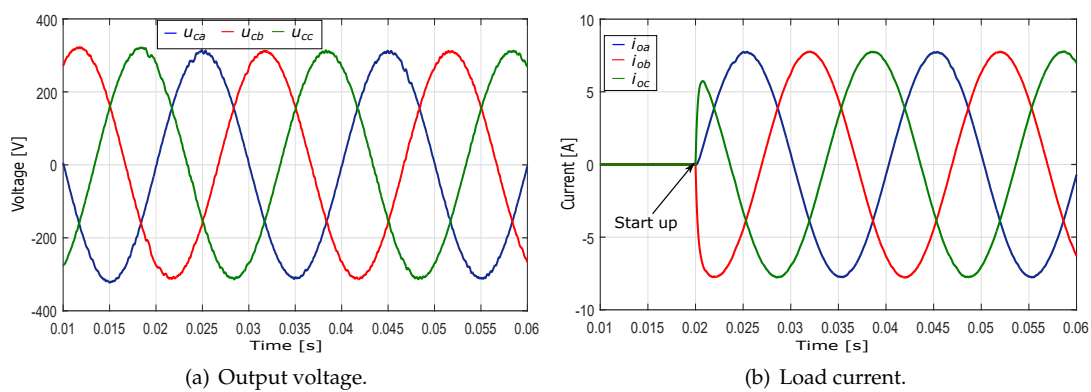


Figure 13. Output voltage and current with the resistive-inductive load step at $t = 0.02$ s.

To investigate the influence of frequency variations, a step change in the voltage from 60 Hz to 50 Hz at $t = 0.03$ s with $R_{load} = 10 \Omega$ is examined in this study. Figure 14 indicates that the proposed method can achieve a reasonable reference tracking despite the sudden change in the frequency.

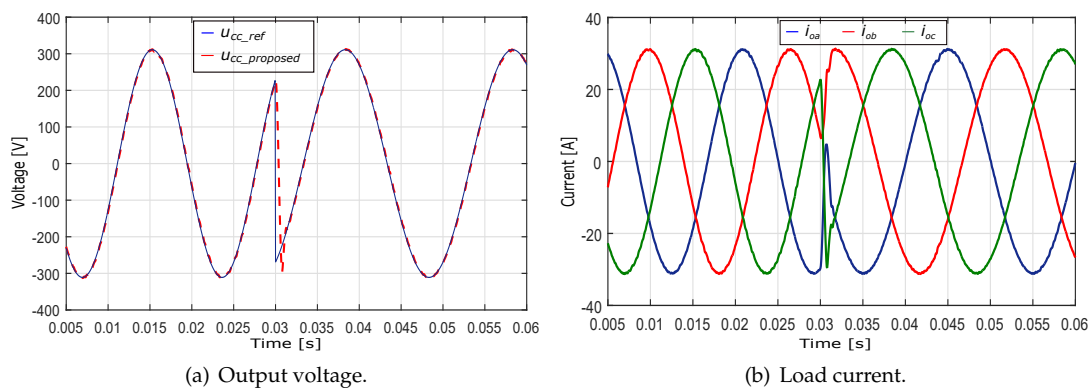


Figure 14. The output voltage and current responses under dynamic change in frequency.

A nonlinear load test is also performed in this study with a diode rectifier and resistive-inductive load ($R = 60 \Omega$, $L_{nl} = 10 \text{ mH}$) as shown in Figure 15c. Figure 15 illustrates that the output voltages give a small distortion, but it still acquires sinusoidal in spite of the high distorted load currents.

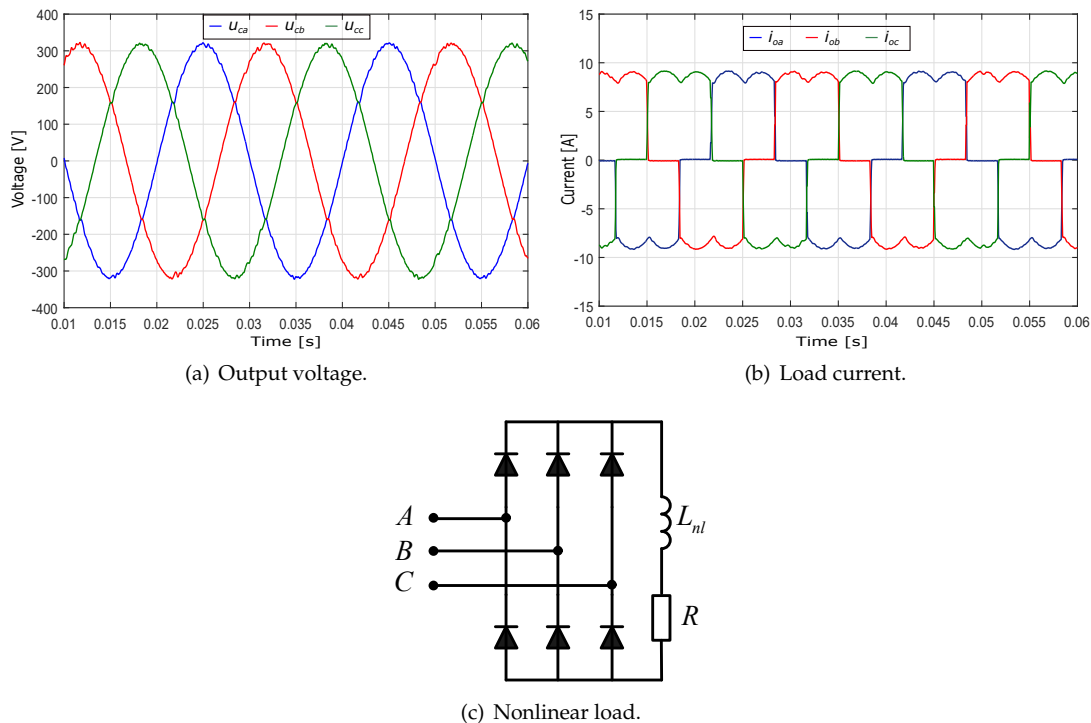


Figure 15. Output voltage and current with nonlinear load.

To confirm the robustness of the controller against parameter variations, we have considered a change of parameters with two cases. In the first case, the filter inductance and capacitance have been decreased to 40% of their real values as illustrated in Figure 16a. On the other hand, the load resistance has been increased to 50% of its value as shown in Figure 16b. It can be observed that the proposed method is continued to obtain sinusoidal current with small deviations. The load current increases from 0.58% to 1.5%, but it still meets within the limit required of the IEEE 519 standard.

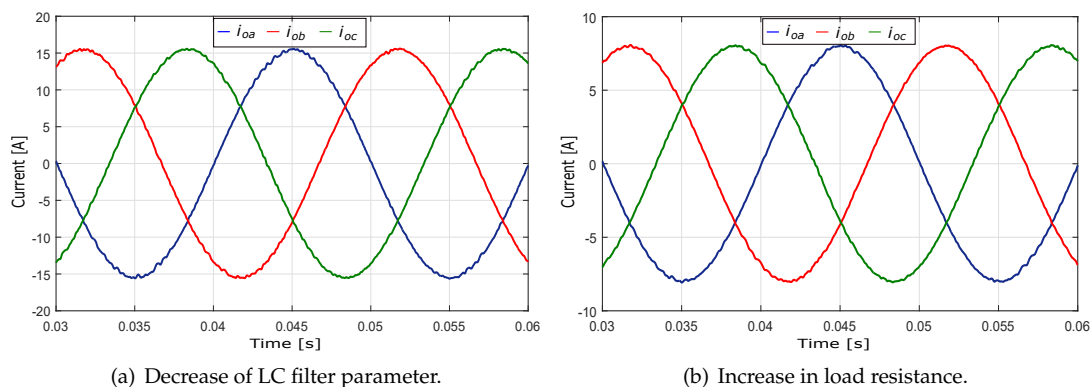


Figure 16. Output current with parameter variations.

4.2. Experimental Results

In order to validate the effectiveness of the proposed control strategy, a laboratory prototype with small power was constructed as shown in Figure 17. A digital signal processor TMS320F28335 [34] was employed to implement the control method. The algorithm was programmed using S-function builder

block in the Matlab/Simulink with embedded coder tools [35]. Twelve modules FGH40T120SMD for IGBT were applied in the three-phase inverter. Furthermore, two capacitors B43305A9108M 1000 μF -400 V were used for DC-link voltage. The parameters of the LC filter were maintained at 3 mH and 40 μF . The LV 25-P and LA 25-P sensors were used to measure the output voltage, filter current and capacitor voltages. The digital signal processing (DSP) generates the signals for 12 switches of 3L-T-type inverter via general-purpose input/output (GPIO) outputs.

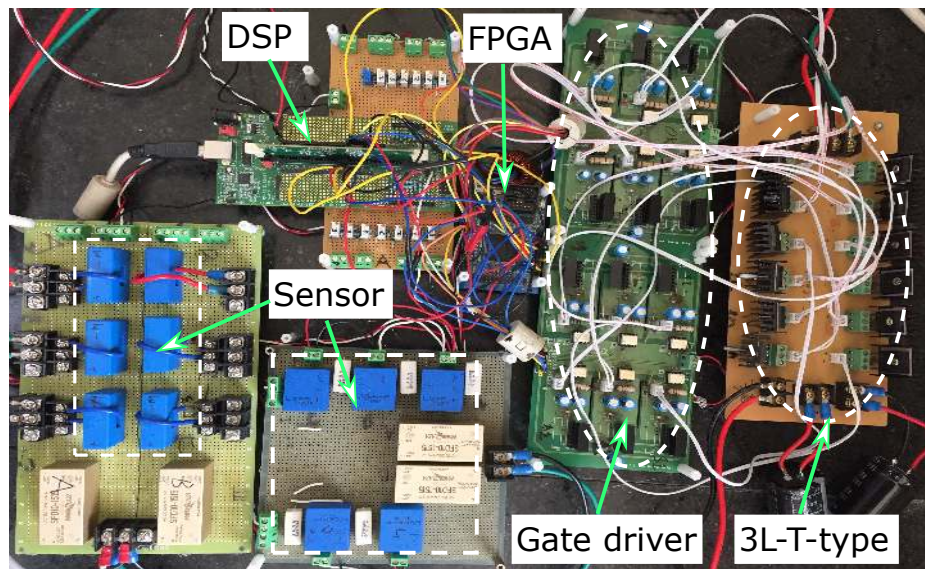


Figure 17. Experimental test bench in the laboratory.

The DC input voltage is set at 180 V while the load resistance is kept at 30 Ω . The reference of the peak phase output voltage is stepped from 90 to 60 V corresponding to the change in output current from 3 to 2 A. Figure 18 indicates that the proposed method has a fast dynamic response and a good balance of DC-link capacitor voltage. As illustrated in Figure 19, the steady-state of three-phase sinusoidal load current confirms the control performance of the proposed method. Furthermore, the execution time of the proposed and conventional FCS-MPC methods are 41 and 64 μs , respectively, as shown in Figure 20. This highlights that the execution time is effectively reduced 36% by the proposed method. Therefore, the sampling time of the conventional method is increased compared with the proposed method resulting in a decrease in the quality of control performance. The load current of the conventional FCS-MPC is depicted in Figure 21. In this case, the THD of the load current of the proposed method is reduced from 1.6% to 1.0% compared with the conventional method as illustrated in Figure 22. Thus, the better performance of the proposed algorithm can be obtained with the low-cost processor.

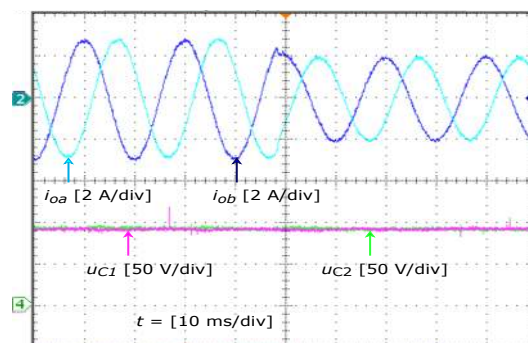


Figure 18. Experimental results for step change in the output voltage.

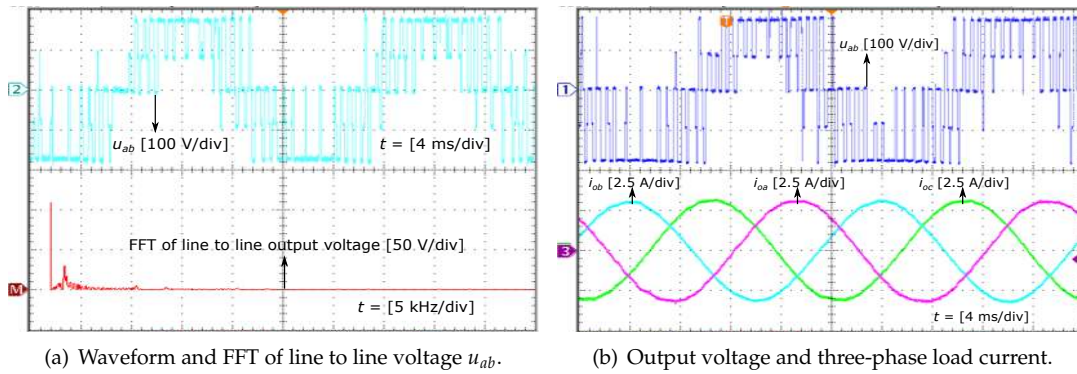


Figure 19. Experimental results of the proposed method with $I_f = 3$ A.

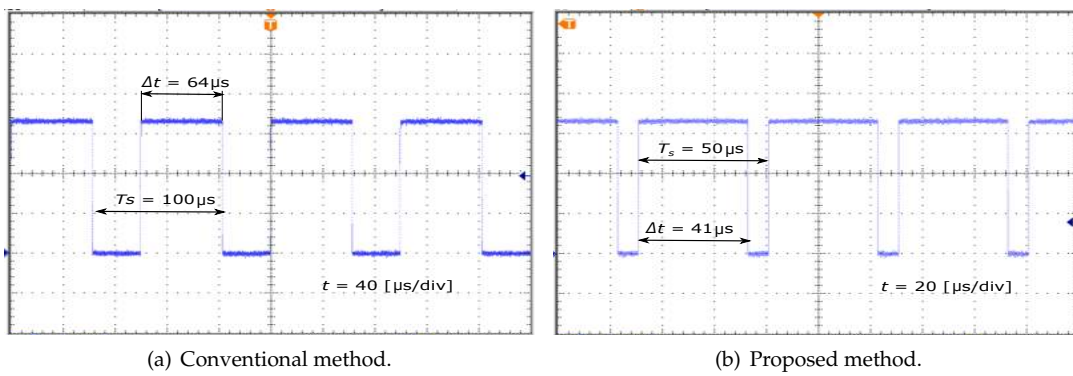


Figure 20. Execution time of the conventional and proposed methods.

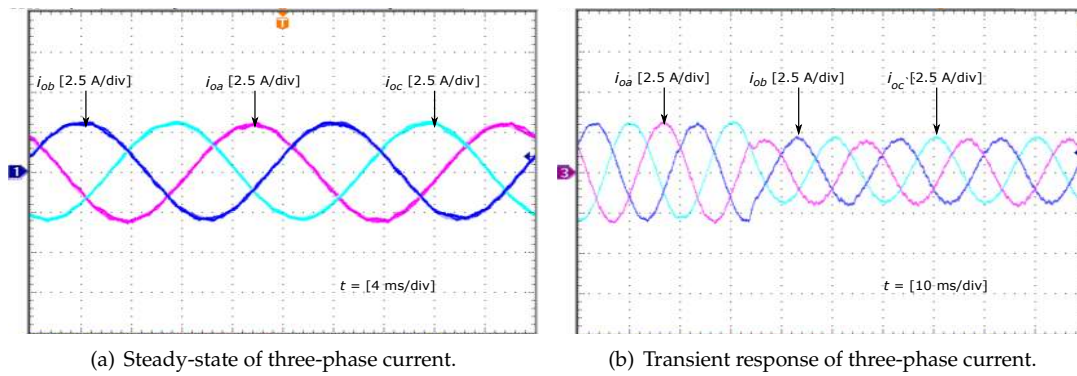


Figure 21. Experimental results of the conventional FCS-MPC.

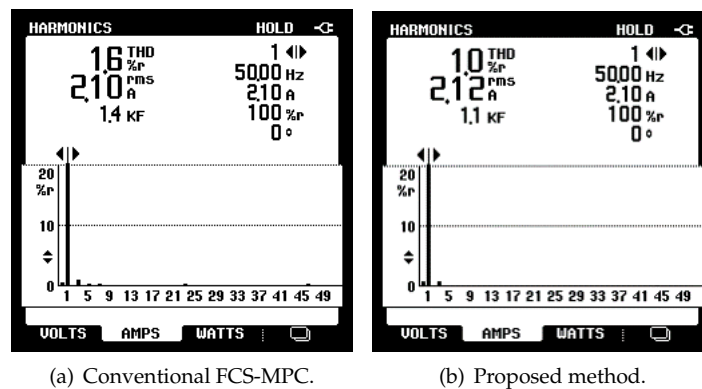


Figure 22. THD of load current.

5. Conclusions

This paper presents a simplified model predictive control method for a three-level T-type inverter. A reduced dynamics model is proposed to decrease the cost and the complexity of the system. Moreover, the execution time is greatly reduced compared with the conventional FCS-MPC by applying the preselection of reference inverter voltage and capacitor voltage balancing, allowing an easy real-time implementation. In order to show the effectiveness of the control strategy, a comparative study of the proposed method and conventional FCS-MPC is performed. Simulation and experimental results prove the feasibility of the proposed approach.

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