Influence of high-K insulator and source stack on the performance of a double gate tunnel FET: a simulation study

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Abstract

In this paper we investigate the influence of incorporating HfO_2 as a dielectric at the drain side and silicon stack at the source side on the electrical performance of a double gate tunnel FET (DG-TFET). For this, we compare a conventional TFET structure with four other structures in which their gate dielectric material is either homogenous or heterogeneous while the insulator in the drain side is either SiO_2 or HfO_2. Moreover, a structure with silicon source stack has been proposed and the device figures of merit are compared with other counterparts. Our simulation results reveal the fact that the presence of HfO_2 insulator in the drain side reduces the ambipolar conduction while heterogeneous gate dielectric enhances the drive current and transconductance. However, HfO_2 slightly deteriorates source-gate and drain-gate capacitances compared to conventional TFET. Furthermore, incorporation of silicon source stack along with heterogeneous gate dielectric and HfO_2 insulator in the drain side lead to higher I_{ON}/I_{OFF} ratio, lower subthreshold slope (S), and lower ambipolar conduction in a 50 nm channel length TFET under study.

Keywords: Double gate TFET; heterogeneous gate dielectric; ambipolar conduction; drive current; parasitic capacitance.

I. Introduction

The steady scaling-down of semiconductor devices and reducing power consumption density in integrated circuits (IC) have led to proposition of many innovative technologies for “More Moore” and “More than Moore” electronics applications [1, 2]. Due to the fact that the power dissipation in TFETs is low, recently they have attracted a lot of attention. Even they become serious candidates for ultralow power applications [3, 4]. Carrier injection mechanism in TFETs is based on Band to Band Tunneling (BTBT), thus their energy dissipation is low and for this reason, it is expected that a significant reduction of off-state current happens in these devices [5, 6]. Furthermore, subthreshold slope in TFETs can be reduced beyond 60 mV/dec; which is proved to be the theoretical limit for conventional MOSFETs [7, 8]. Therefore, TFETs are very energy efficient and can be incorporated in circuits operating at very low supply voltage targets

[9-12]. However, TFET devices suffer from low on-state current (I_{ON}) and ambipolar current conduction (I_{amb}) when utilizing them in circuits [12-14]. The low I_{ON} in TFETs is due to BTBT carrier injection mechanism during which electrons tunnel from the valence band of the source region to the conduction band of the channel region or from the valence band of the channel region to the conduction band of the drain region, whose band bending in energy gap is controlled by the gate bias [15, 16]. The ambipolar conduction in TFETs occurs due to the large BTBT at the source-channel junction as well as the drain-channel junction at different polarities of gate voltage to obtain the drive current. This can prevent the device to be turned off completely. As a result, a TFET can show n-type behavior with the electrons as majority carriers or p-type behavior with the holes as majority carriers at the same drain voltage [15, 16].

To boost the drive current in TFETs, many ideas have been proposed in the literature. Inserting source-pocket (*SP*) doping [17-19], tunneling-area engineering using high-k dielectric [6, 20, 21], double gate architecture [22], gate to source overlap [23], gate to drain underlap [24], dual material gate [25] and using strained silicon [26], are among these proposed approaches. The ambipolar conduction problem can be reduced with incorporating some techniques such as gate-drain underlap [23, 27], Gaussian or non-uniform drain doping [6, 28], work function engineering of gate electrodes [29], spacer engineering and gate material engineering [30, 31].

In this paper we show step by step in several supplementary structures that how the presence of heterogeneous gate dielectric, HfO_2 insulator in the drain side of the gate, and silicon source stack in the source side can both enhance the drive current and reduce ambipolar current conduction compared to a conventional DG-TFET. Furthermore, Transconductance (g_m), gate-drain capacitance (C_{gd}), gate-source capacitance (C_{gs}), subthreshold slope (S) and I_{ON}/I_{OFF} ratio are also analyzed for the structures under study at a given 50 nm channel length.

The rest of this paper is organized as follows: In Section II, the proposed device structures and simulation models are discussed. Section III addresses the electrical characteristics of devices under study. Finally, summaries of the principal findings and conclusions of this paper are given in Section IV.

II. Devices Structure and Simulation Parameters

Fig. 1 shows the schematic cross-section view of five devices under study. Structure (I) is a conventional DG-TFET with SiO_2 gate dielectric. Structure (II) is similar to conventional DG-TFET but with HfO_2 gate dielectric. In structure (III), both gate dielectric and drain side insulator are HfO_2 insulator. In structure (IV) heterogeneous gate dielectric and HfO_2 insulator in the drain side of gate has been utilized, and in the structure (V) a silicon source stack has been added to the structure (IV). In this work, our simulation results are evaluated in comparison to conventional TFET in the structure (I) and we have arranged the number of structures under study so that the effect of applying each modification in the structure to be sensible on the electrical performance. All simulation parameters related to the structures under study are presented in Table 1.

All the simulations have been carried out using TCAD simulator SILVACO-ATLAS version 5.22.1.R. We have used nonlocal band-to-band tunneling (BTBT) model to compute the tunneling current in the lateral direction. Bandgap narrowing (BGN) model is utilized to account for highly doped regions in the devices. Shockley-Read-Hall (SRH) and Auger models were used to consider generation/recombination in simulations. Furthermore, drift diffusion carrier transport model and Fermi-Dirac distribution function

model used in simulations. Tunneling through the gate oxide is ignored, as in works [32-34]. Since the silicon film thicknesses is 10 nm, we have not considered the quantum confinement effects arising due to thin SOI body [36]. We have calibrated the simulation setup with Boucart's work [6], shown in Fig. 2, which achieved by considering electron and hole tunneling masses of $m_e=0.07m_0$ and $m_h=0.71m_0$, respectively. The primary objective of this work is to consider the combined relative effects of heterogeneous gate dielectric, HfO_2 insulator in the drain side of the gate and source stack on the drive current and ambipolar current with respect to conventional scheme by using the qualitative trends.

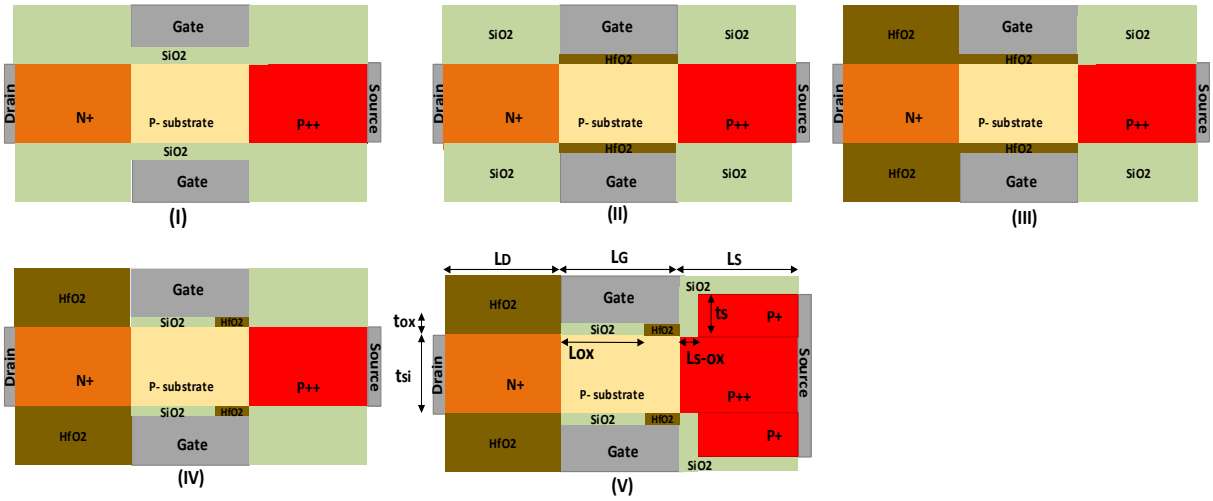


Fig. 1: Schematic representation of double gate TFETs under study; (I): conventional DG-TFET, (II) conventional DG-TFET with HfO_2 gate dielectric, (III): DG-TFET with HfO_2 dielectric in the gate and drain side, (IV) DG-TFET with heterogeneous gate dielectric and HfO_2 insulator in the drain side, (V) DG-TFET with heterogeneous gate dielectric, HfO_2 insulator in the drain side and silicon stack in the source side.

Table 1: Parameters for structures under study

Parameter	**Value**
Oxide thickness (t_{ox})	1 nm
Silicon channel thickness (t_{si})	10 nm
Channel Length (L_G)	50 nm
SiO_2 length in the gate (L_{OX})	45 nm
Source/Drain extended length (L_S/L_D)	100 nm
Source stack oxide length ($L_{S\text{-}OX}$)	4 nm
Stack thickness (t_S)	7 nm
Gate Workfunction	4.3 eV
HfO_2 permittivity	22 [37]
Channel doping (P)	1e17 cm^{-3}
Source doping (p^{++})	1e20 cm^{-3}
Drain doping (N^+)	5e18 cm^{-3}
Source stack doping (p^+)	5e19 cm^{-3}

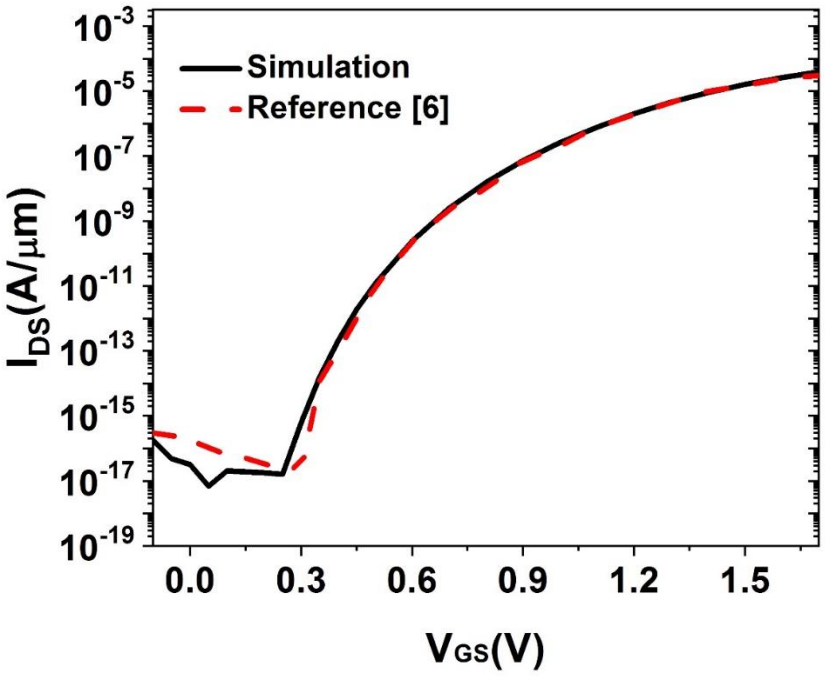


Fig. 2: Calibration of simulator against the results in ref. [6] at V_{DS}=1.0 V.

III. Results and Discussion

Fig .3 depicts transfer characteristic of five TFETs at V_{DS}=1.0 V. It is observed from this figure that conventional TFET (I) and TFET (II) have higher ambipolar conduction compared to other TFETs in the graph at negative gate voltages. At positive gate voltages is can be seen that TFETs (II), (III) and (V) have the highest drive currents. The transfer characteristics behavior of the devices under study can be explained by their energy band diagram profiles which is taken by a cutline at 1 nm below Si-oxide interface, through the silicon active region of the devices as shown in Fig.4 (a,b). According to the WKB approximation, the tunneling probability, *T(E)*, is calculated using [37]:

$$T(E) = \exp\left(-2\int_{x_{start}}^{x_{end}} K(x)dx\right) \quad (1)$$

where *K* is evanescent wave vector and x_{start} and x_{end} point to start and end points of tunneling path. Ideally, the start and end points of tunneling path should be considered in flat-band (neutral) regions of either side of junction where their influence can be calibrated by carrier effective mass. Afterward, the calculated tunneling probability in each energy level is used to calculate the current density [37]. For thinner tunneling width, tunneling probability increases [38]. Based on above theorem and Fig. 4(a), it is observed that TFETs (I) and (II) have more band bending and therefore, tunneling width is shorter in their profiles. Thus, ambipolar conduction is higher in these devices compared to TFETs (III), (IV) and (V). According to this figure, incorporating HfO_2 insulator in the drain side of gate causes the conduction band (or valance band) slope to be decreased. This slope is proportional to electric field intensity and this leads to reduced band bending and ambipolar conduction in the devices with HfO_2 insulator in the drain side. On the other hand

Fig. 4 (b) depicts that energy band diagrams of all TFETs except TFET (I) have overlap at the tunneling region. So it is expected that they have the same order of drive current as a result.

Based on Fig. 3 and Fig. 4, the role of utilizing HfO_2 above drain side or underneath the gate, heterogeneous dielectric and source stack, in the structures can be explained. It is obtained that the presence of HfO_2 dielectric in the whole gate region of TFETs (II) and (III) causes electrostatic control of gate over the channel to be strongly increased and then the drive current to enhance, while embedding HfO_2 above drain of TFET (III) has led ambipolar conduction in this device to be reduced about four orders of magnitude compared to TFET (II) with similar structure. As it is mentioned earlier, this improvement is indebted to more tunneling width formation (Fig. 4(a)) in drain-channel junction of TFET (III) compared to TFET (II) due to incorporation of HfO_2 above the drain side. The structural difference between TFETs (III) and (IV) is embedding a heterogeneous dielectric in TFET (IV) which their Id-Vg characteristic difference reveals the heterogeneous gate role in the device. As it is obvious from Fig.3, embedding of heterogeneous dielectric has reduced both the drive and ambipolar currents. If fact, utilizing HfO_2 in the source side of gate oxide reduces tunneling width by more band bending in the channel-source junction and this in turn leads to drive current enhancement. However, utilizing low-K dielectric (SiO_2) on the drain side of the gate insulator increases the tunneling width in the channel-drain junction and this reduces ambipolar conduction compared to conventional structure. The structure of TFET (V) is similar to TFET (IV) but with additional source stacks in the source side. Based on Fig. 4 (b), it is obtained that incorporation of silicon source stack reduces the effective tunneling width in the source-channel junction of TFET (V). In fact, as Fig. 4 (c) shows, the source stack leads to formation of sharper potential profile in the source-channel junction of structure (V) compared to (IV). This increases the electric field and reduces the tunneling width in the source-channel junction. Therefore, the drive current in TFET (V) enhances. It is also obvious that the ambipolar current is comparable with TFET (IV) and source stack has no effect on it.

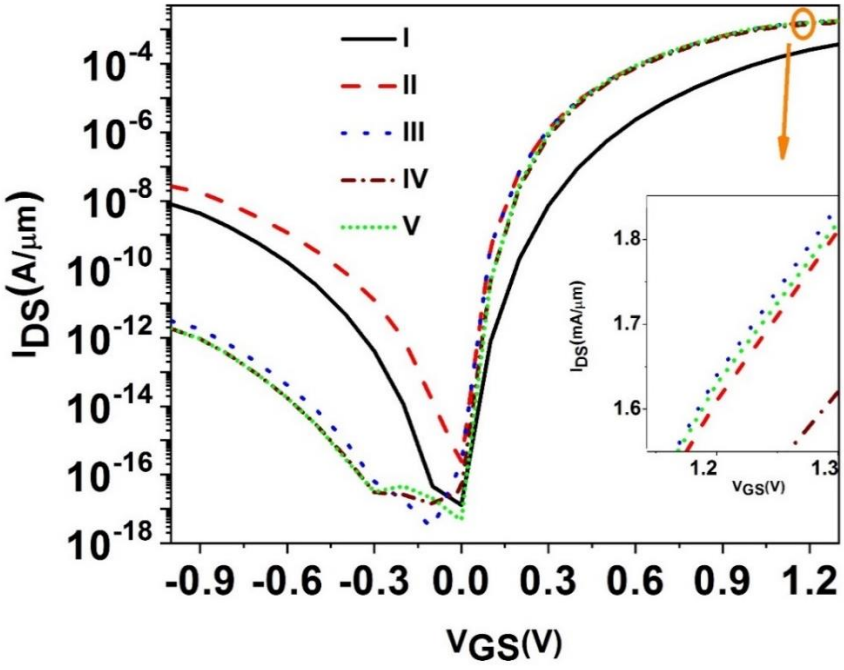
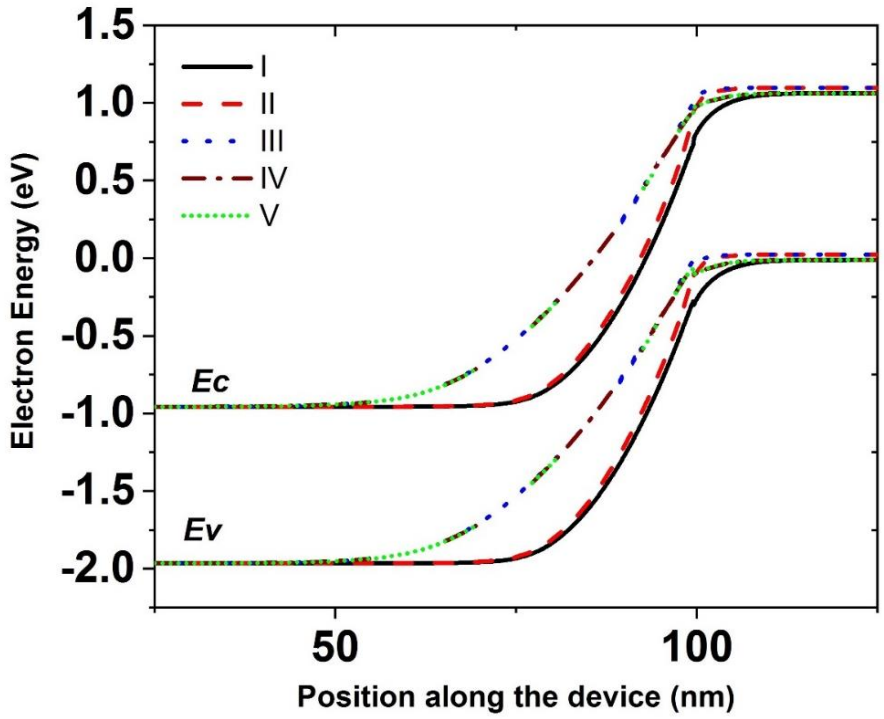
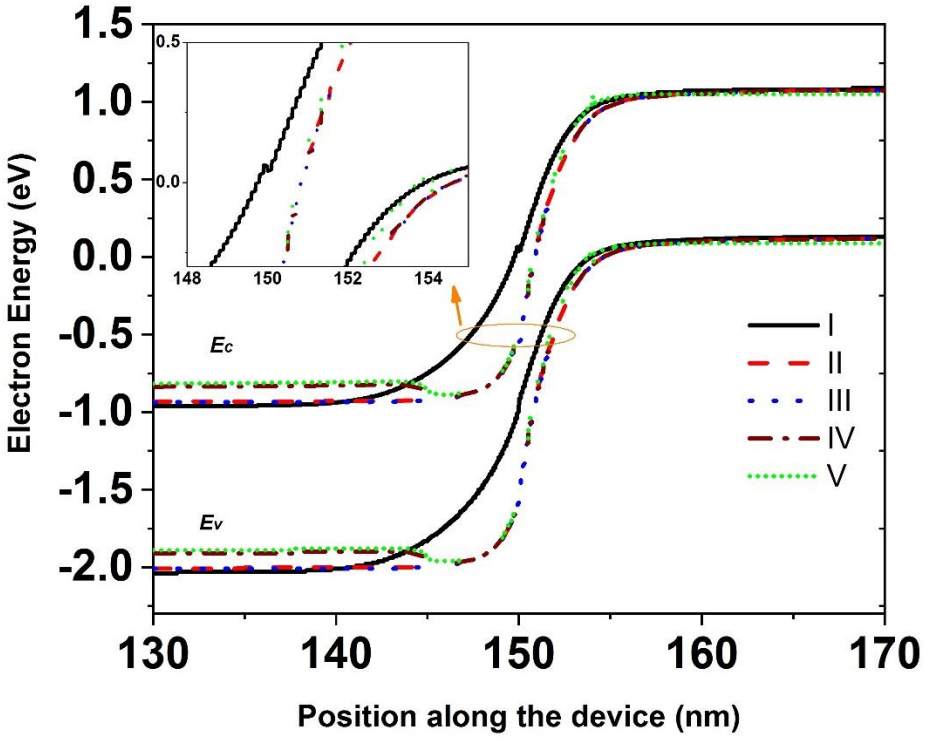


Fig. 3: Transfer characteristics (I_D-V_{GS}) of five TFETs under study at V_{DS}=1 V.


Electron Energy (eV)
Position along the device (nm)
I
II
III
IV
V
Ec
Ev

(a)


Electron Energy (eV)
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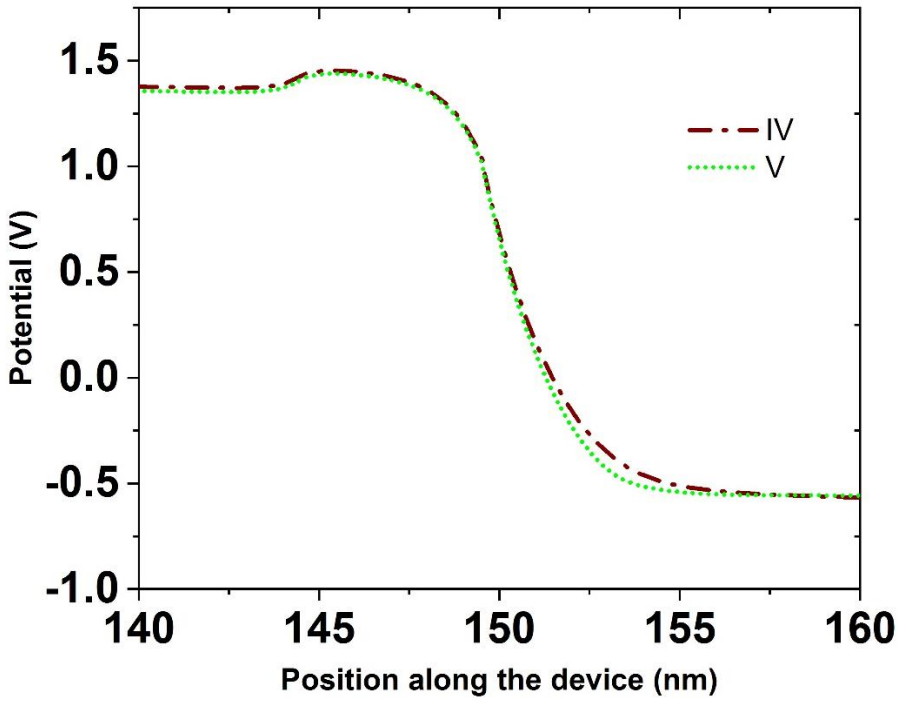
(b)



(c)

Fig. 4: Energy band diagram of five TFETs at (a) V_{GS}=-1 V and (b) V_{GS}=1.3 V; (c) The potential profile of structures IV and V at V_{GS}=1.3 V. For all cases the drain bias is V_{DS}=1 V.

In analogue devices the amount of amplification is a figure of merit. It is proportional to transconductance g_m, which is defined by $g_m=dI_D/dV_{GS}$ [39]. Higher g_m in a device means that gate has better control over device current variation. Fig. 5 shows that this parameter in TFETs (II), (III) and (V) are comparable and much higher than conventional TFET (I). Indeed, these improvements indebted to incorporation of heterogeneous gate dielectric, HfO_2 insulator in the drain side and source stack in the related TFET structures. This is due to the fact that these facilities enhance gate control over the channel as earlier explained.

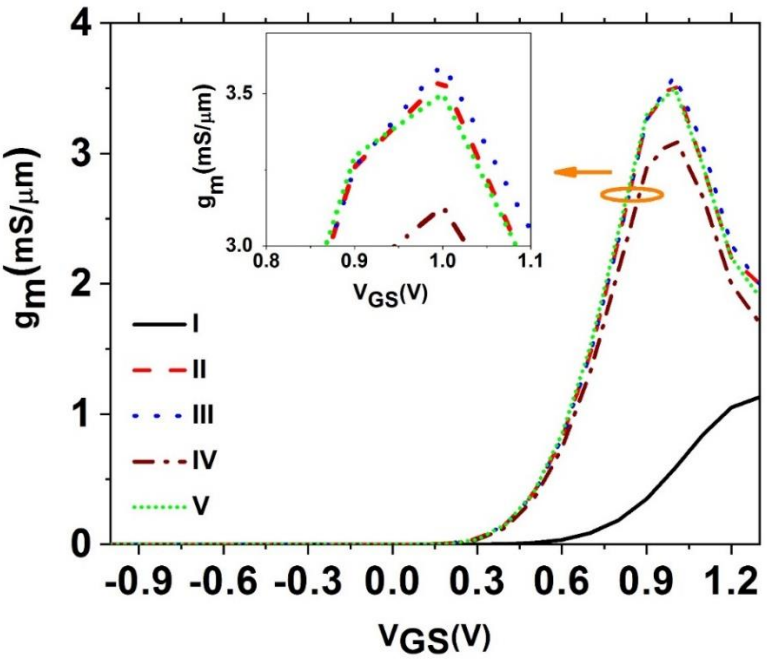


Fig. 5: Transconductance for different TFETs under study at V_{DS}=1 V.

In another investigation we considered the effect of incorporation of high-k material (like HfO_2) in the drain side on two important capacitances comprised of gate-drain (C_{gd}) and gate-source (C_{gs}) components, since it can deteriorate these parasitic capacitances [19]. Fig. 6 shows C_{gd} increases by increasing V_{GS} for all devices. This owes to enhanced coupling between the gate and drain charges at higher gate voltages. It is observed from this figure that TFETs (II) and (III) have highest parasitic components, while in TFETs (IV) and (V) the parasitic components are more comparable to conventional TFET (I). The latter is due to the fact that they have heterogeneous gate dielectric with lower permittivity (ε_{SiO2}=3.9) in the drain side of their structures and this reduces coupling between two terminals. Fig. 7 depicts C_{gs} decreases by increasing V_{GS} for all devices. This is due to reduced coupling between the gate and source terminals at higher gate voltages as indicated in [19]. Since gate dielectric in TFETs (II) and (III) is uniform with HfO_2, the parasitic capacitance C_{gs} is highest for these devices compared to all other devices. In addition, C_{gs} of TFETs (IV) and (V) is closer to that of conventional TFET (I). It emphasizes the fact that heterogeneous gate dielectric can cause this parasitic capacitance to be comparable to conventional counterpart. From Fig. 6 and Fig. 7 it is also obtained that source stack has no significant effect on the parasitic components of C_{gd} and C_{gs}.

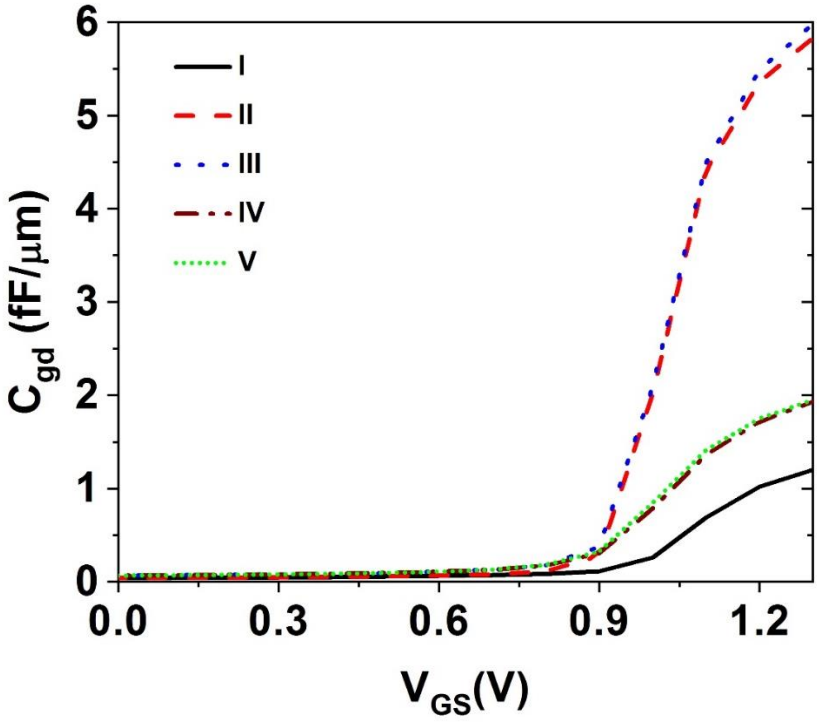


Fig. 6: Gate-drain capacitance versus gate voltage for different TFETs at V_{DS}=1 V and frequency= 1 MHz.

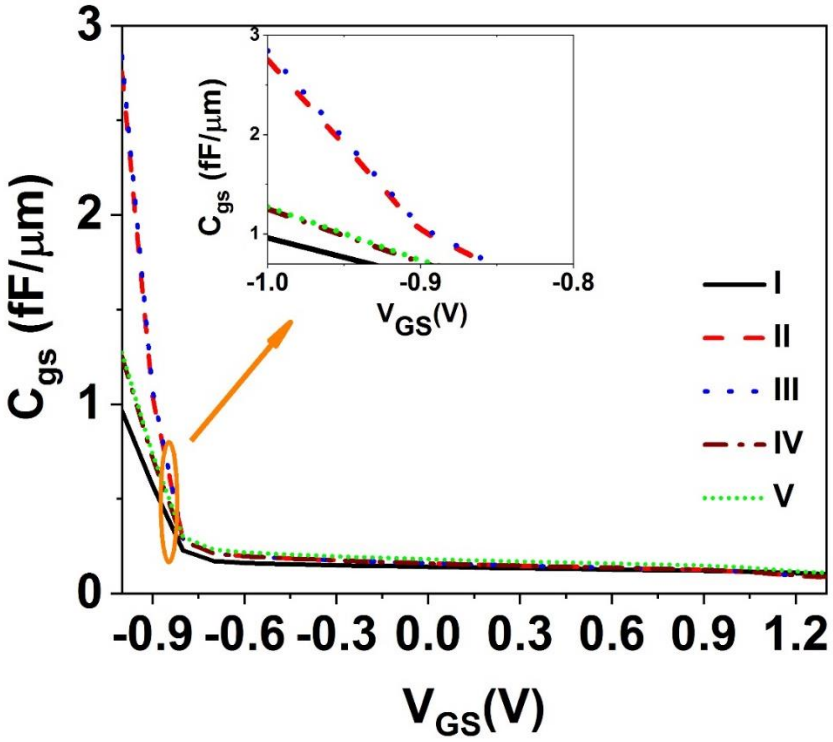


Fig. 7: Gate-source capacitance versus gate voltage for different TFETs at V_{DS}=1 V and frequency= 1 MHz.

Fig. 8 illustrates I_{ON}/I_{OFF} ratio, sub-threshold slope (S) and ambipolar conduction (I_{amb}) for five DG-TFETs under study. It is observed that incorporating heterogeneous gate dielectric (SiO_2 and HfO_2) along with source stack can enhance I_{ON}/I_{OFF} ratio and decrease S parameter. It can also be seen that for the devices with HfO_2 insulator in the drain side, I_{amb} reduces and it is obtained that TFET (V) has the best performance in terms of mentioned parameters due to its supplementary specific structure compared to its counterparts.

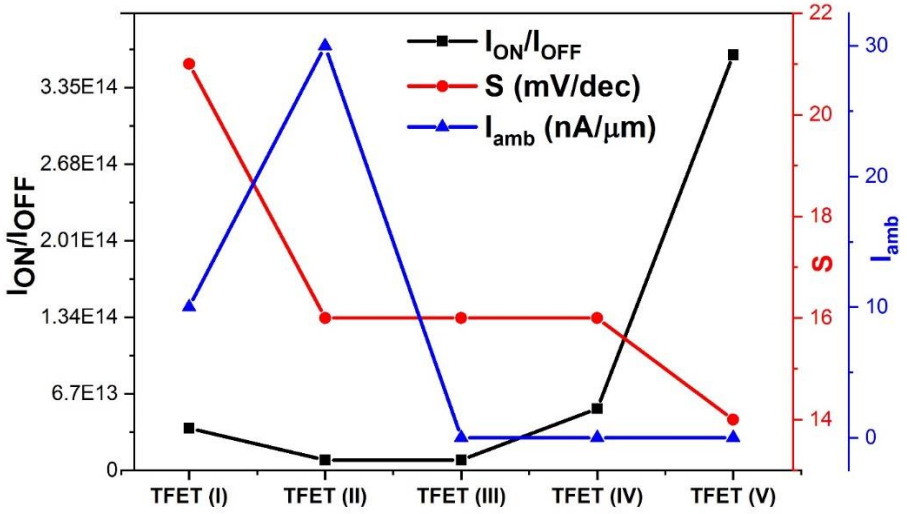
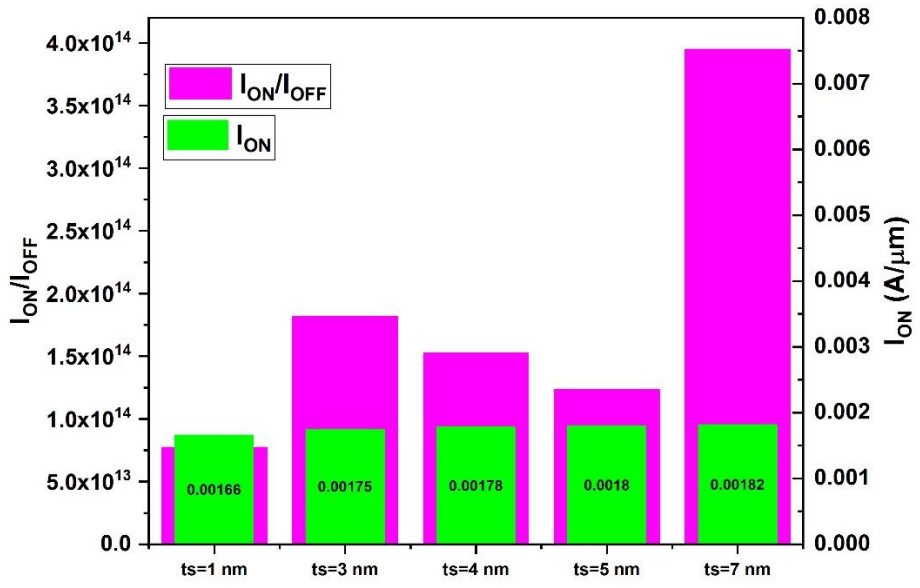
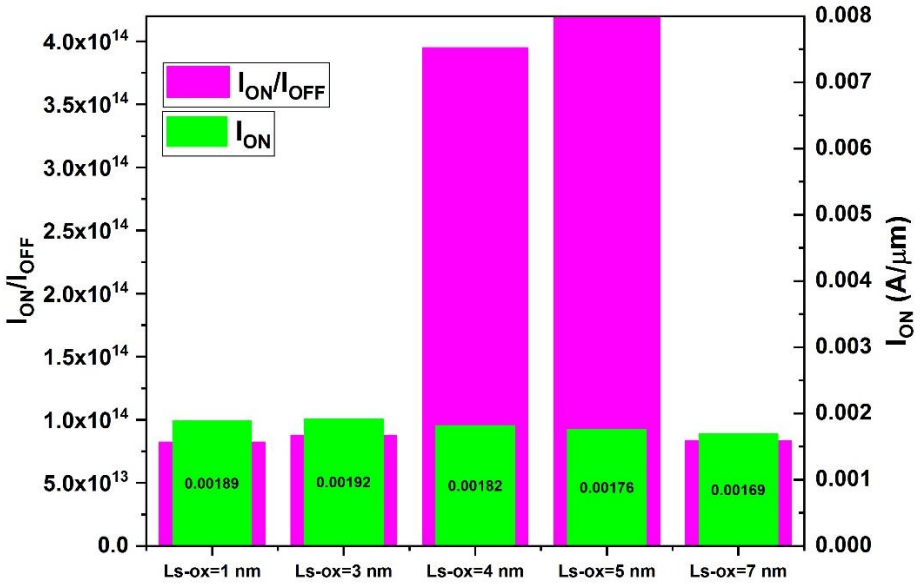


Fig. 8: I_{ON}/I_{OFF} ratio (black), subthreshold slope (red) and ambipolar drain current (blue) for five devices under study. I_{OFF} measured at bias V_{DS}=1 V and V_{GS}=0 V and ambipolar conduction (Iamb) measured at bias V_{DS}=1 V and V_{GS}=-1 V.

It is worth noting the influence of source stack parameters (t_s, $L_{s\text{-}ox}$) and its doping value on the performance of TFET (V). As Fig. 9 depicts, there is a nonlinear relation between the device current and source stack thickness (t_s) or stack oxide length ($L_{s\text{-}ox}$). Based on this figure, I_{ON} and I_{ON}/I_{OFF} current ratio will be close to optimum values at t_s= 7 nm and $L_{s\text{-}ox}$= 4 nm, compared to other source stack thicknesses and stack oxide lengths. It is also clear in Fig. 10, when silicon source stack doping value is set to 5e19 cm^{-3}, I_{ON}/I_{OFF} current ratio becomes one order of magnitude higher than two other doping values. Moreover, the subthreshold swing (S) parameter for the selected doping of 5e19 cm^{-3} is slightly lower (14 mV/dec) compared with other cases. The S parameter for source stack doping values of 1e19 and 1e20 cm^{-3} is equal to 16 and 17 mV/dec, respectively. As a result, we chose 5e19 cm^{-3} as the optimum source stack doping value.



(a)



(b)

Fig. 9: I_{ON}/I_{OFF} current ratio along with I_{ON} value obtained for structure (V) by parameter variations of (a) stack thickness, t_s and (b) source stack oxide length, $L_{s\text{-}ox}$. The measurements are all at bias of V_{DS}=1 V and V_{GS}=1.3 V.

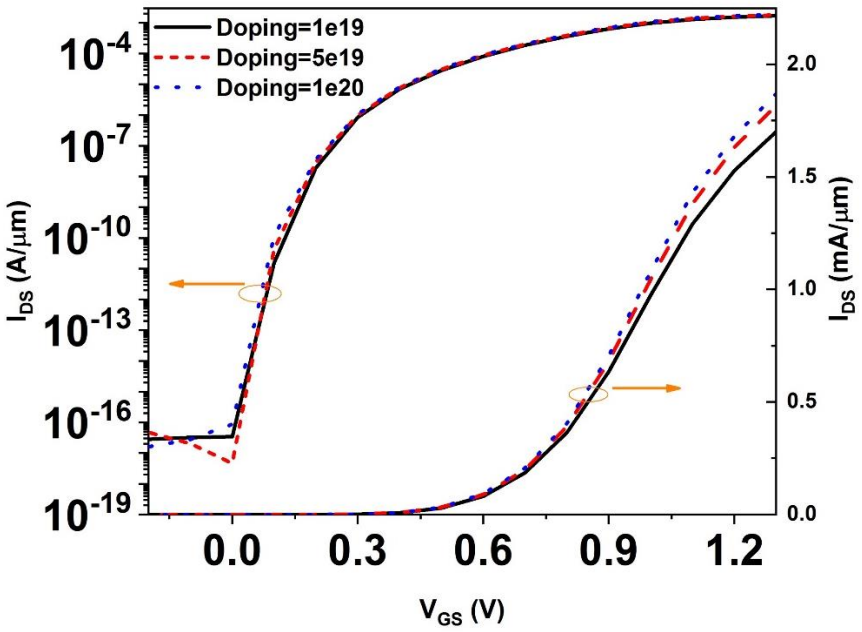


Fig. 10: Transfer characteristics of structure (V) obtained for different source stack doping values at V_{DS}=1 V.

IV. Conclusion

In this work we considered the effects of incorporating heterogeneous gate dielectric, HfO_2 insulator in the drain side of gate and silicon source stack on the electrical characteristics of double gate TFET. We observed that incorporating heterogeneous gate dielectric along with HfO_2 insulator in the drain side can reduce ambipolar conduction and keep low gate-drain and gate-source parasitic capacitances with respect to conventional double gate TFET by making strong barrier in the drain-channel and channel-source junctions. Embedding silicon source stacks can further enhance drive current along with I_{ON}/I_{OFF} ratio and reduce *S* parameter while having no intensive effect on mentioned parasitic capacitances. Thus, it seems TFET (V) has promising electrical behavior for low power applications.

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