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A Single Channel IGBT Gate Drivers for Medium Voltage Converters

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Abstract: This article treats the gate driver system for IGBT modules in Medium-Voltage (MV) applications. The study focuses principally on two functions of an IGBT gate driver: an impulse signal transmission and a power transmission. For each function, the suitable topology is proposed. Then, for safety and device's protection reason, all gate driver functions must sustain the high and very high galvanic insulation voltage capabilities. For low-cost design, the insulation system can be achieved with the help of the insulating material in a pot core planar transformer. Therefore, for each function, the optimized design of a pot-core transformer and its associated electronics components is performed with the help of a virtual prototyping tool (a genetic algorithm: GA code in MATLAB^{TM}). The first section focuses on optimization design of a selected topology for an impulse signal transmission function. A bi-objective (maximize the output voltage v_{out} and minimize the input current i_{mos}) problem of this function that leads to a Pareto front is presented. Several Pareto fronts' results are obtained assuming different insulation layers thickness. The second part focuses on optimization design of a selected topology for a power transmission function. Maximize the converter efficiency (η_{con}) and minimize the output power (P_{out}) are considered as a bi-objective. Thus, numerous Pareto fronts' results are achieved for a few different insulation thicknesses. Finally, the prototype of a single channel IGBT gate driver is invented to validate the proposed design.

Keywords: IGBT Gate Driver, Medium-Voltage Converter, Insulated Transformer, Dielectric Material

1. Introduction

Nowadays, the power converter for MV application is mostly used in electric ship, railway electrification, electrical power distribution [1-8]. According to works of literature, numerous modular voltage source converters (VSC) are proposed such as: Multilevel Converter [9], Neutral Point Clamp [10], Flying Capacitors [11], Cascaded Half-Bridge [12], and series connection of IGBT modules [13]. Amongst them, the modular multilevel converter is technically recommended as shown in Figure 1a.

For safety and protection purposes, IGBT gate drivers for IGBT modules in the MV-MMC converter must support the insulation voltage which equals input DC voltage $V_{in,DC}$ (can reach few of 10kV as mentioned in Figure 1b and [4]). Figure 1c illustrates the main four functions of the IGBT gate driver system [5-8]. In this research paper, the authors address the optimization design of the impulse signal transmission function and the power supply function. The insulation technology is done through the air-gap of the pot core planar transformer (cf. Figure 1d) [22]. With the air gap thickness of 0.5mm with a dielectric polyetherimide, the few of 10kV of insulation voltage level is achieved [14, 15].

The optimization methodology for these functions: geometric of transformer is performed with finite element (FEMM^{TM}) software and transient simulation is done by the simulator (LTSpice^{TM}). Hence, the optimization results under Pareto fronts are obtained by the help of a genetic algorithm (GA) coded in MATLAB^{TM} script which can run FEMM^{TM} and LTSpice^{TM} software.

The structure of this paper is divided into three sections: Section 2 presents the optimization for these two functions. Section 3 and Section 4 illustrate the validation results and the conclusions/perspectives, respectively.

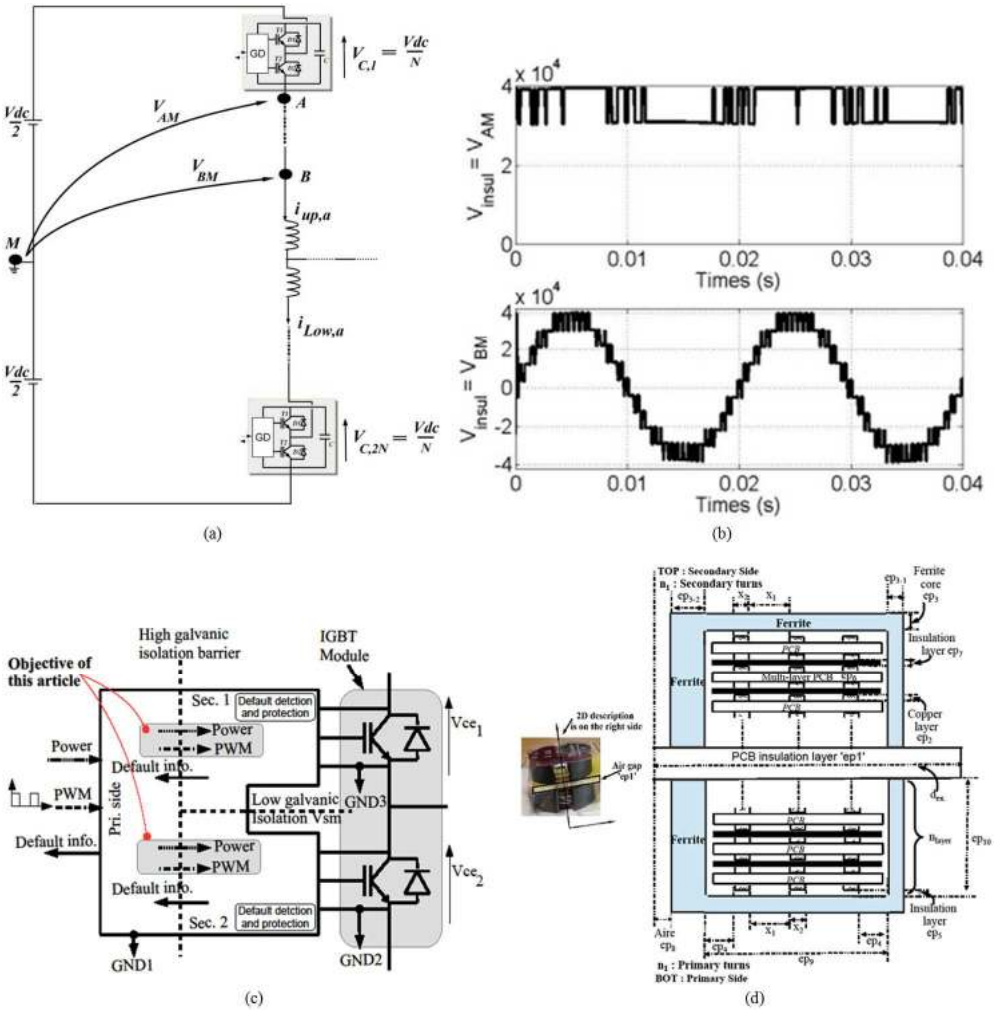


Figure 1. *(a) MV-MMC converter with SMs, (b) determination of insulation voltage level for MV-MMC, (c) IGBT gate driver's functions and objective of this article, (d) geometric of transformer design.*

2. Design for a Single Channel IGBT Gate Driver

2.1. Impulse Signal Transmission Function

Figure 2a presents a proposed circuit for an impulse signal transmission function. According to this figure, a series resonant (C_1, L_p, R_p, N-MOSFET) and a parallel resonant (L_s, R_s, C_2) are proposed to form an impulse transmission circuit that is generated by N-MOSFET. Moreover, for discharging the energy in C_1, R_1 = 10kΩ is required and is located in parallel to this capacitor. The transformer air gap thickness (ep_1) and its polyetherimide dielectric are used to determine the galvanic insulation voltage level. According to Am et al. [7], ep_1 = {0.5mm - 3mm} can achieved the insulation voltage level more than 10kV.

Maximize the output voltage (v_{out}) and minimize the input current (i_{mos}) are set as a bi-objective optimization problem. This current must be minimized for reducing the power consumption in the system. To achieve these bi-objectives, the optimization variables are: C_1, C_2, R_{out} (electrical) and n_1, x_1, n_{layer} (geometrical of the transformer). Then, with the help of the effective virtual prototyping tool (genetic algorithm: GA code) [19-20], the optimization results under the Pareto front forms are obtained.

Optimization variables for an impulse signal transmission function: The optimization variables are abstracted in vector X: $X_{PWM} = (n_1, x_1, n_{layer}, C_1, C_2, R_{out})^t$. As presented in Figure 1d, x_2 is an internal geometrical variable and is expressed in equation (1) as a function of other geometrical variables and parameters. The geometrical parameters are constants and are summarized in Table 1.

$$x_2 = \frac{ep_9 - 2ep_4 - (n_1 - 1)x_1}{n_1} \quad (1)$$

Optimization flowchart and constraints for an impulse signal transmission function: Figure 2b details the optimization procedure for this proposed design. As presented previously, v_{out} (to be maximized) and i_{mos} (to be minimized) are determined as a bi-objective function. And this optimization design process must satisfy the optimization constraints listed in Table 1.

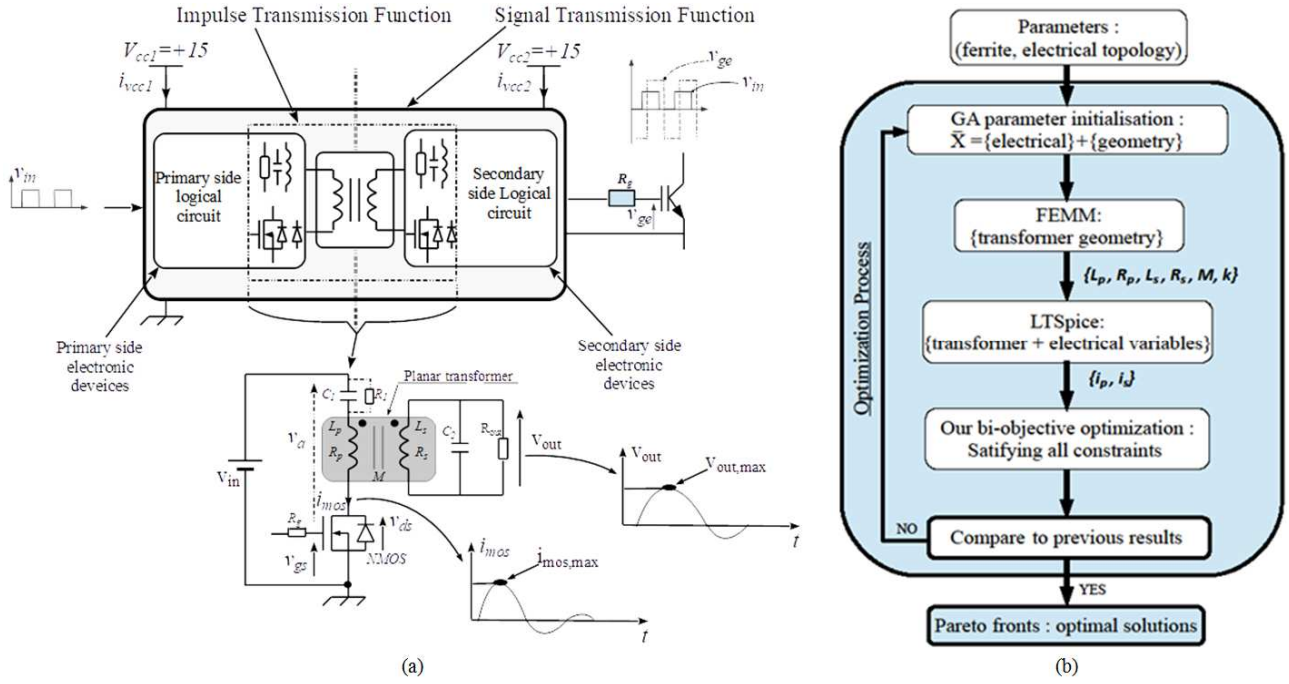


Figure 2. *(a) An impulse signal transmission function, (b) optimization flowchart for this function.*

Table 1. *Constant parameters and constraints for a transformer.*

Parameters	Values
ep_1: air gap	{0.5mm to 3mm}
ep_2: the thickness of the copper	{70µm, 105µm}
{ep_3, $ep_{3\ 1}$, $ep_{3\ 2}$, ep_8, ep_9, ep_{10}}: pot core dimension [21]	--
ep_4: reserve length	0.2mm
ep_6: PCB layers	0.4mm
ep_7: insulation between layers	18µm
$ep_5 = ep_{10}+ep_7-n_{layer}(ep_6+ep_7+2ep_2)$	--
D_F: pot core diameter	{7mm, 9mm, 14mm}
Opt. constraints	Values
n_1, n_{layer}	{1, 5}
x_1	[0.2mm, 0.4mm]
C_1 and C_2	[0.1nF, 10nF]
R_{out}	[1kΩ, 30kΩ]
ep_5	≤ 0.3mm
C_{ps}	≤ 10pF

2.2. Power Supply Function

As shown in Figure 3a, a DC-DC isolated power supply is required for supplying the necessary power to electronics and logic components at the secondary side of the gate driver system. For ensuring the operation, the insulation of power supply function and signal transmission function must be at the same level. According to Am et al. [7-8], a full-bridge series-series resonant converter is highly recommended in terms of high efficiency (ZVS operation) and high insulation achievements. Figure 3b shows the equivalent circuit of a selected DC-DC power supply topology. This converter constructs with: 4 MOSFETs for an active inverter stage from DC input power to AC output (resonant tank), series resonant tanks (C_{pr} and C_{se} in series with a primary and a secondary winding), four diodes for an uncontrolled rectifier stage. Finally, the filter capacitor C_f has placed to smooth-out the final DC output voltage (V_{out}). Moreover, the voltage ratio (G_v=V_{out}/V_{in}) of this DC-DC converter is illustrated in Figure 3c. According to these G_v curves with different load levels, the output voltage can be independent of the magnetic coupling of the transformer and the load when G_v=1. According to the demonstration in the article [7-8] and resonant tanks parameters in Table 2, the voltage transfer ratio is derived as presented in equation (4). Based on this equation and Figure 3c, the G_v can be operated independently of the magnetic coupling (k) and the load (R_L) at frequency $f_{V,H}$=fres/$\sqrt{(1-k)}$ where the zero voltage switching (ZVS) condition is achieved [16 - 18].

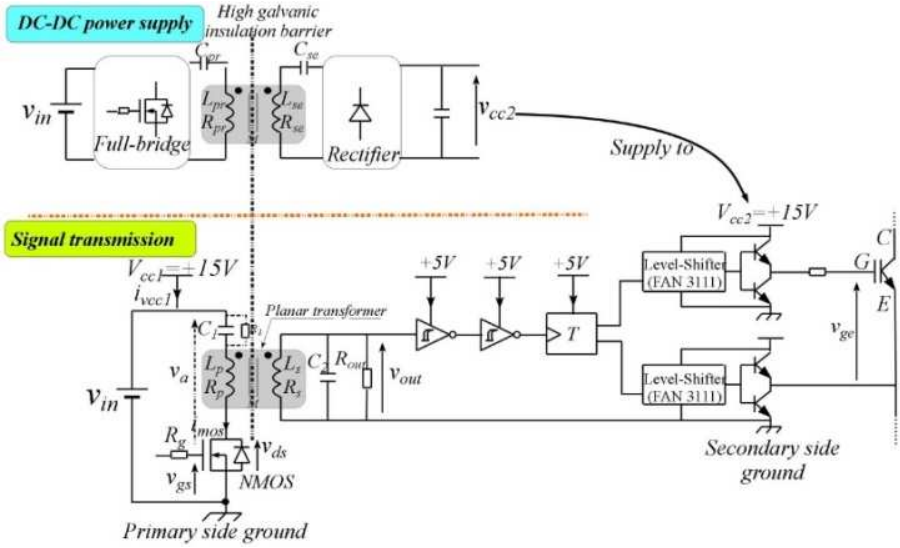
$$i_{se} = \frac{j\omega M V_{in}}{(Z_{se}+R_L)(Z_{pr}+Z_r)} \tag{2}$$

$$V_{RI} = R_L \frac{j\omega M V_{in}}{(Z_{se}+R_L)(Z_{pr}+Z_r)} \tag{3}$$

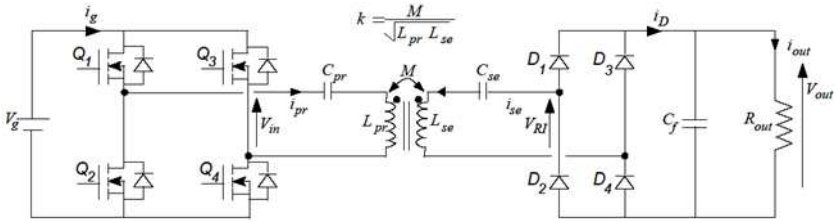
$$G_v = \frac{V_{out}}{V_g} = \frac{j\omega M}{\frac{Z_{pr}Z_{se}+(\omega M)^2}{R_L}+Z_{pr}} \tag{4}$$

The output P_{out} and the converter efficiency η_{con} of this converter are presented in detail by Dijiruc et al. [14]. Thus, maximize the converter efficiency η_{con} and minimize the output power are set as a bi-objective optimization problem.

Optimization variables for a power supply function: the same as a PWM signal transmission function, the variables compose of the electrical variables (C_{pr}, C_{se}, f_p, R_{out}) and geometrical variables (cf. Figure 1d: n_1, x_1, n_{layer}, ep_2, ep_6). Thus, the vector optimization variables X is X_{power} = (n_1, x_1, n_{layer}, ep_2, ep_6, C_{pr}, C_{se}, f_p, R_{out})^t. Moreover, the optimization parameters are mostly the same as a PWM signal design except for the pot core diameter D_F. For a power supply design, these diameter D_F are 14mm, 18mm, and 22mm.



(a)



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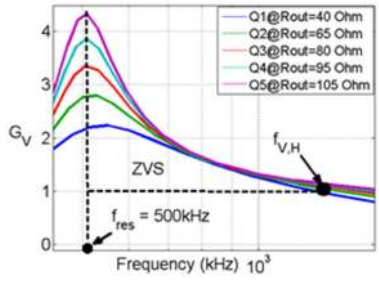

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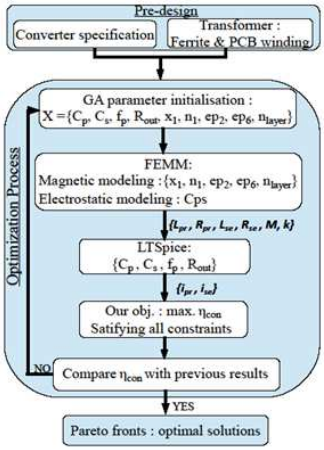


(d)

Figure 3. *(a) A complete IGBT gate driver (b) a proposed DC-DC isolated converter for a power supply function, (c) Voltage transfer ration G_v, and (d) optimization flowchart for this function.*

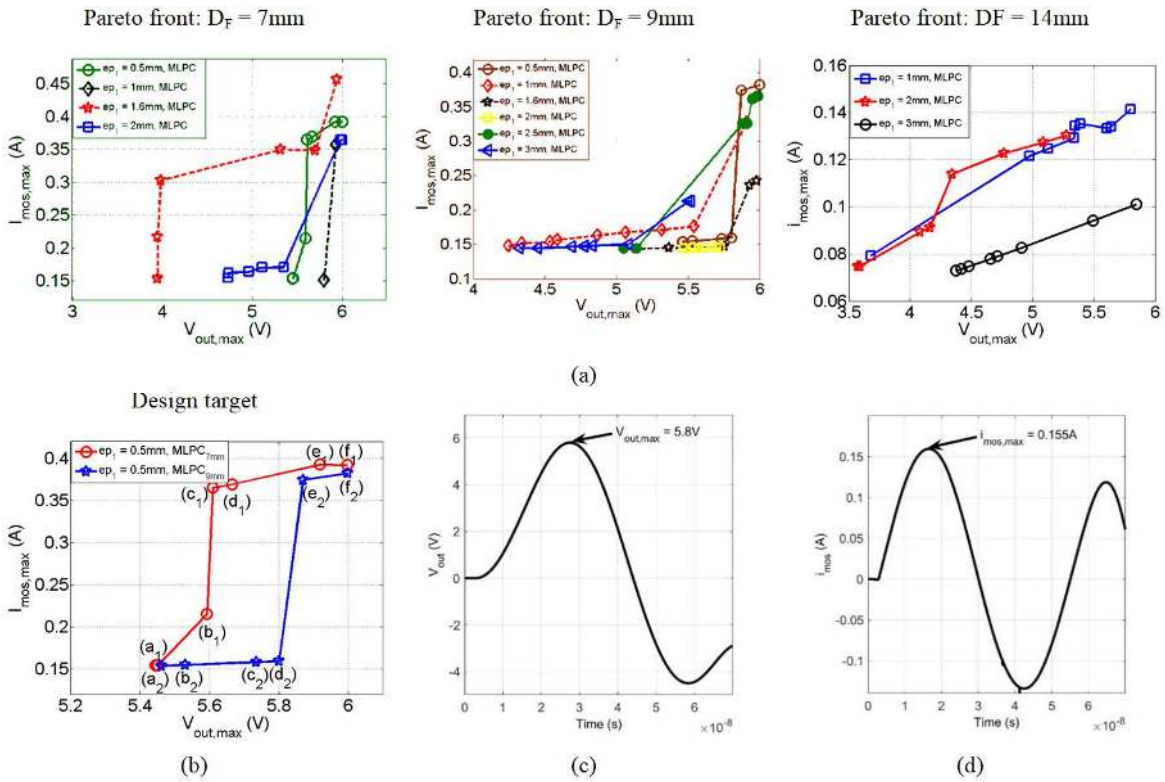


Figure 4. *(a) Pareto front results for different D_F and ep_1, (b) design target for the prototype (c)-(d) simulation result of v_{out}, i_{mos}., respectively.*

Optimization flowchart and constraints for a power supply function: Figure 3d details about the optimization procedure by taking into account all the variables and parameters. But in order to achieve the bi-objective optimization with the feasibility of the physical design, numerous technical constraints must be respected (referred to Table 3).

Table 2. *Equation of the system (calculations from Figure 3b).*

Definition	Equation
Input tank	$V_{in} = (4/\pi)V_g \sin(\omega t)$
Compensation	$C_{pr} = 1/\omega^2 L_{pr};\ C_{se} = 1/\omega^2 L_{se}$
Pri. impedance	$Z_{pr} = j\omega L_{pr} + 1/j\omega C_{pr} + R_{pr}$
Sec. impedance	$Z_{se} = j\omega L_{se} + 1/j\omega C_{se} + R_{se}$
Load	$R_l = 8R_{out}/\pi^2$
Equi. impedance	$Z_r = (\omega M)^2/(Z_{se} + R_L)$
Input current tank	$i_{pr} = V_{in}/(Z_{pr} + Z_r)$
Output current tank	$i_{se} = j\omega M i_{pr}/(Z_{se} + R_L)$
Output voltage	$V_{Rl} = R_L i_{se} = (4/\pi)V_{out} \sin(\omega t)$

Table 3. *Optimization constraints for a power supply design.*

Description	Constraints
x_1	[0.2mm - 0.5mm]
n_1	{1 - 5}
n_{layer}	{2 - 4}
ep_2	{35; 70; 105; 210; 235; 435} [µm]
ep_6	{0.4; 0.5; 0.8; 1.2; 1.6} [µm]
C_{pr}, C_{se}	[1nF - 100nF],
f_p	[150kHz - 1MHz],
R_{out}	[10Ω - 100Ω],
V_{out}	[V_g - 20V]
i_{out}	≤ 0.5A
B_{max}	≤ Bsat
ep_5	≤ 0.5mm
C_{ps}	≤ 10pF

3. Simulation and Validation Results

3.1. Simulation Results

A signal transmission function: the optimization results under the Pareto fronts, for D_F = {7mm, 9mm, and 14mm} and ep_1 = {05mm to 3mm}, are shown in Figure 4a. As previously mentioned, an ep_1 = 0.5mm associated with a polyetherimide material is recommended for the 40kV MV-MMC application. Thus, with this insulation level, one Pareto front from D_F = 7mm and one Pareto front from D_F = 9mm are considered for the design target as presented in Figure 4b. Amongst these possible solutions, the solution d_2 is selected because of its low power consumption and acceptable voltage information. Table 4 summarized all the numerical values of this solution. Figure 4c and Figure 4d illustrates the output voltage v_{out} and a primary side current i_{mos}. According to the rate of this current, the proposed PWM signal transmission technology consumes much energy less than the result in the article [5].

A power transmission function: The Pareto fronts ($_{con}$ versus P_{out}) for ferrite diameter D_F = {14mm, 18mm, 22mm} and ep_1 ={0.5mm - 3mm} are shown in Figure 5a-c. According to these results, the solution from D_F=14mm is dominant in terms of the highest efficiency. For the same insulation as an impulse signal transfer, the solution from ep_1=0.5mm is considered. So, the solution (a) is selected for prototype work because of its output power of 2W is achieved (cf. Figure 4d). This solution (a) is summarized in Table 4.

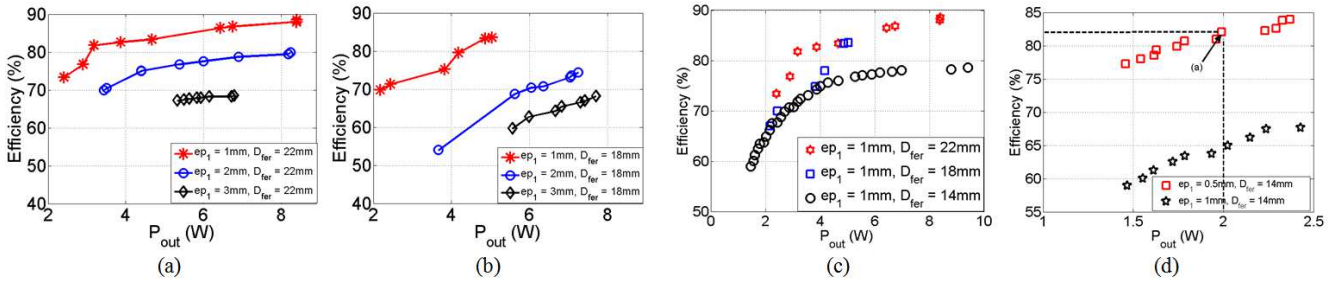


Figure 5. *Pareto front results of a power supply function for different D_F: (a) 22mm, (b) 18mm, (c) 14mm, and (d) the optimization design target for prototype.*

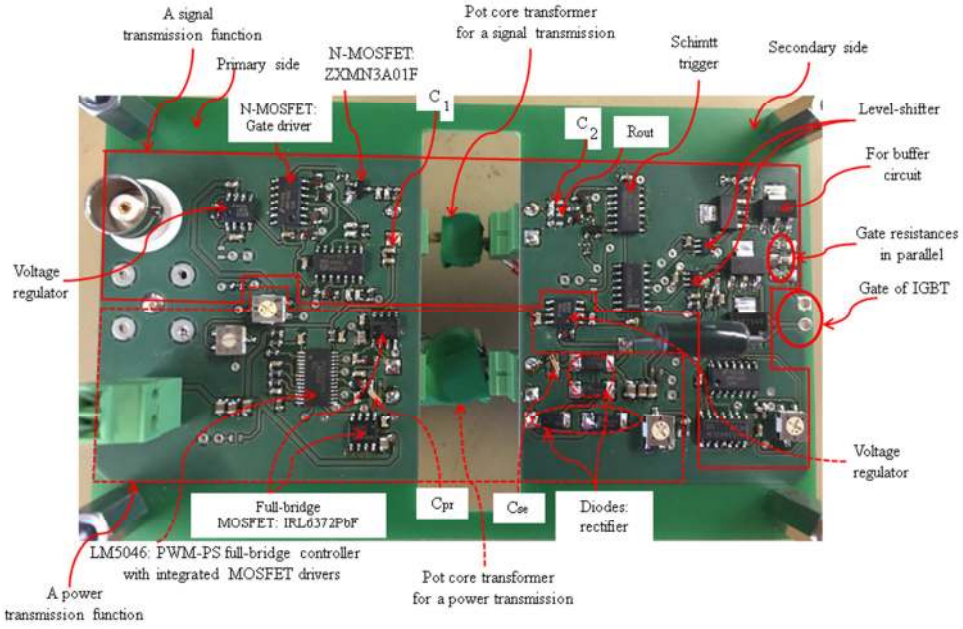
Table 4. *Numerical solutions: solution (d_2) for a PWM signal transmission function and solution (a) for a power supply function.*

Optimization results	Solution (d_2)
V_{out}/i_{mos}	5.8V/0.15A (see Figure 4c)
ep_1/D_F	0.5mm/9mm
L_p/R_p	2.03µH/0.26Ω
L_s/R_s	2.03µH/0.26Ω
M/k	1.57µH/0.776
R_{out}/R_1	30kΩ/10kΩ
$x_1/n_1/n_{layer}$	0.32mm/2turns/3layers
Optimization results	Solution (a)
η_{con}/P_{out}	82%/2W
V_{out}/I_{out}	13.3V/0.16A
ep_1/D_F	0.5mm/14mm
C_1/C_2	68nF/68nF
L_{pr}/R_{pr}	17.24µH/0.46Ω
L_{se}/R_{se}	17.24µH/0.46Ω
M/k	10.49µH/0.78
R_{out}/R_1	30kΩ/10kΩ
C_{ps} (capacitor parasitic)	6.67pF
R_{out}/f_p	76.9Ω/266kHz
x_1/x_2	0.25mm/0.87mm
n_1/n_{layer}	2 turns/ 4 layers
ep_2/ep_6	105µm/0.4mm

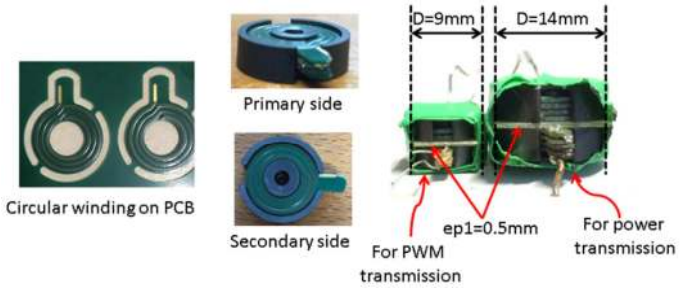
3.2. Comparison Results

Figure 6a shows the prototype of a single channel IGBT gate driver. The power supply locates at the lower side. The main components for this function are 2 full-bridge MOSFETs (IRL6372PbF) are controlled by LM5046 controller, 4 diodes (MBRA340T3), a pot core transformer (D_F =14mm), and 2 capacitors. The upper side of Figure 6a illustrates the prototype of a PWM signal transfer. The main components for this function are N-MOSFET (ZXMN3A01F) is controlled by 74LS32, 2 capacitors, a pot core transformer (D_F = 9mm) and output resistor. Figure 6b presents the sample of the prototype of an optimal transformer. Then, the experimental test-bench is resumed in Figure 6c.

Validation results for a power supply function: According to the voltage transfer ratio G_v (cf. Figure 7a), in order to achieve ZVS condition and obtain $V_{out} \leq 20V$, the operating frequency must stay between 200kHz and 350kHz. The comparison results for the selected solution (a) are illustrated in Figure 7b. The small error between these two cases surely comes from little error values of each component. Figure 7c shows the comparison results for frequency varies from 200kHz to 350kHz. Then, another comparison result for load varies (R_L = [39Ω to 82Ω]) are shown in Figure 7d. Based on these, the output voltage from 12.5V to 13V and output power from 2W to 4W are achieved. Then, the efficiency higher than 74% is recorded.



(a)



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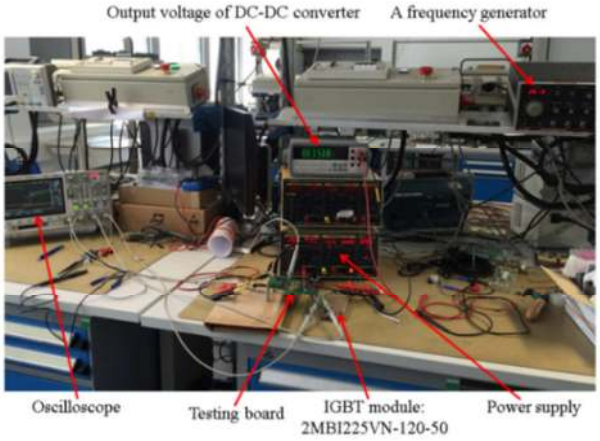

(c)

Figure 6. *(a) A prototype of a single channel IGBT gate driver, (b) optimal transformer set-up, (c) Experiment test-bench for the prototype.*

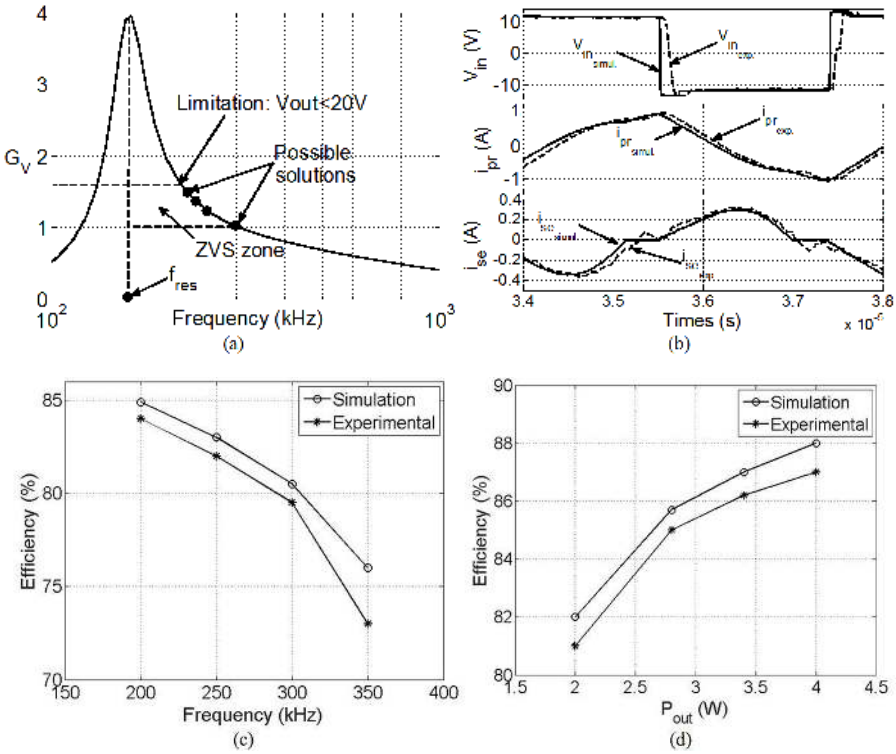

Figure 7. *(a) Voltage transfer ratio: G_v, (b) validation results for i_{pr}, i_{se}, v_{in} of the resonant tanks of solution (a), (c)-(d) converter efficiency for frequency and load varies, respectively.*

Validation results for a PWM signal transmission function: As discussed in the previous section, the optimal solution (d_2: D_F = 9mm and ep_1 = 0.5mm) of a PWM signal transmission function is selected for practical works. Figure 8b illustrates the experimental results of the voltages V_{out} (output voltage), V_{ds} (drain-source voltage of N-MOSFET) and V_{ge} (gate-

emitter voltage of IGBT). According to these experimental results, the propagation delay is around 70ns the same as mentioned in an article Am et al. [5] but consumes less power compared to that article. The output voltage information V_{out} of a proposed circuit is the vital variable for experimental validation for comparing to the simulation result. As shown on the left side in Figure 8c, $V_{out,max}$ is 5.7V for the practical work result which is about 0.1V lower than the simulation result. The difference surely comes from the parasitic elements (passive components) and circuit layout.

Furthermore, on the right side of Figure 8c, the comparison waveforms of i_{mos} are also provided where the peak is about 1.5A (for experimental result) and 1.55A (for the simulation one). Then, the gate-emitter voltage $V_{ge}(t)$ = +/- 15V of the IGBT module is achieved as illustrated in Figure 8d for a few electrical periods.

4. Conclusion

This research article presents a high insulation voltage single-channel IGBT gate driver: a power supply function and a PWM signal transmission function. Two proposed topologies are described for the application where the insulation voltage of 40kV is required. This voltage level can be achieved by using 0.5mm air-gap with polyetherimide material of pot core transformers.

For the PWM signal transmission function, several optimal Pareto fronts are obtained. Amongst these solutions, the solution d_2 (ep_1= 0.5mm/ D_F = 9mm) is selected for experimental works. For the power supply function, a full-bridge resonant topology is chosen. Then, numerous optimization results under Pareto front forms are obtained for different insulation voltage levels. Optimal solution a (ep_1 = 0.5mm/ D_F = 14mm) is selected for practical works.

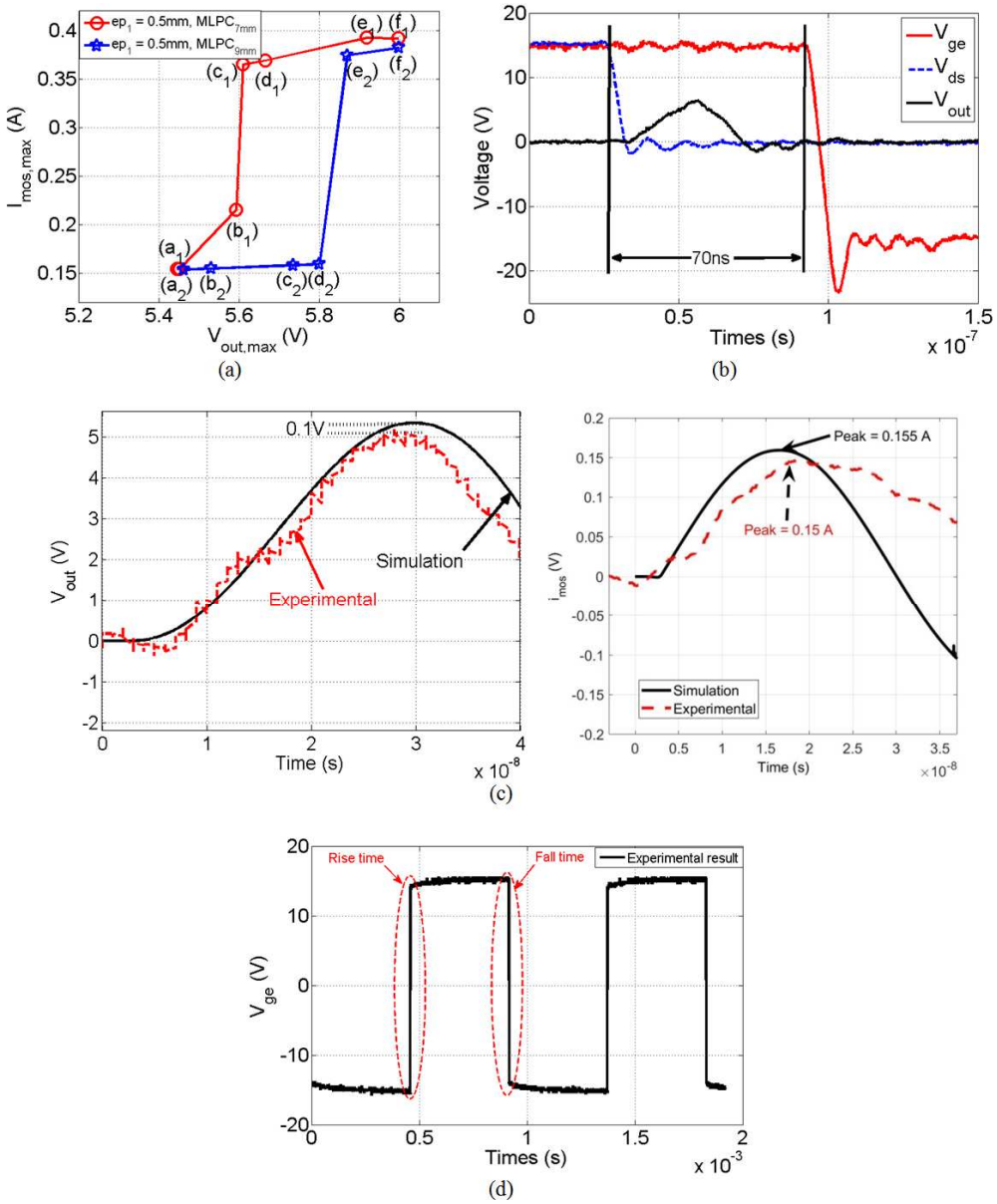

Figure 8. *(a) optimization solution (d_2) of a PWM signal transmission function, (b) waveform of V_{out}, V_{ds} of MOSFET at primary side and V_{ge} of IGBT for a solution (d_2), (c) The comparison results in the output voltage and a primary side current, (d) $V_{ge}(t)$ = -/+15V of IGBT module.*

For the experimental works, two optimal transformers and experimental boards are set up. Then, the experimental waveforms are measured to compare with the simulation ones. The comparison trends for important variables are shown with a small difference that comes from the parasitic elements and circuit layout.

For the next study, the authors focus on a very high insulated power transmission of gate drivers in a series connection of multiple power devices. The series connection of multiple devices is shown in Figure 9. We will investigate on a power transformer, EMI reducing architecture, minimization of the parasitic capacitor, etc.

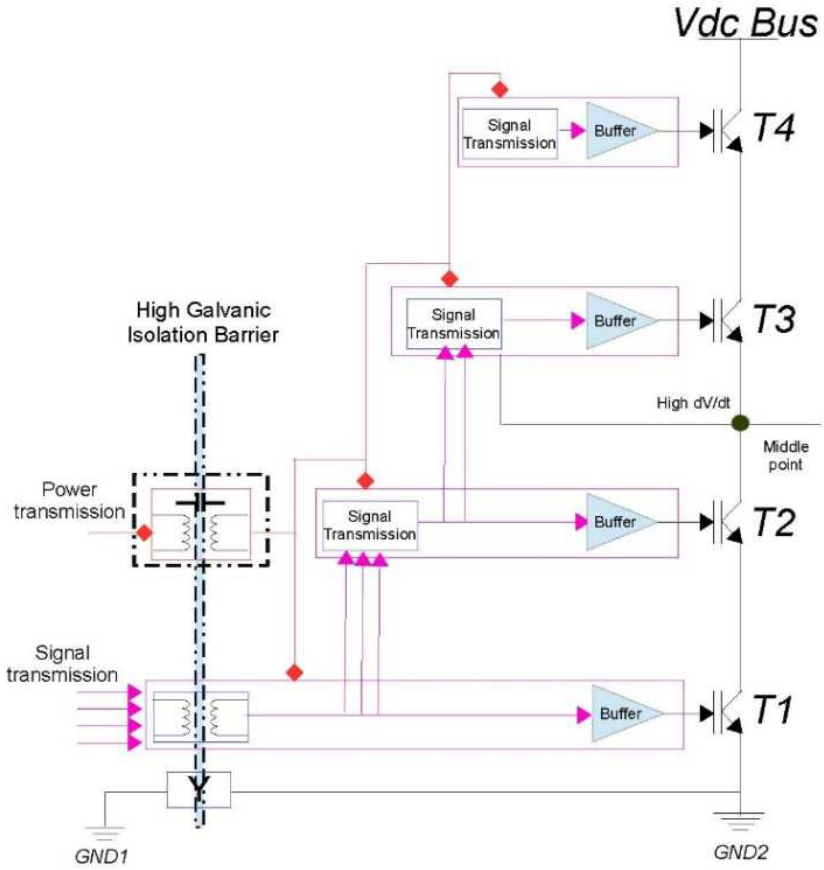

Figure 9. *A synopsis of high insulated power transmission for a series connection of power devices.*

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