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A Single-Chip CMOS Transceiver for 802.11a/b/g Wireless LANs

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***Abstract*—A dual-band trimode radio fully compliant with the IEEE 802.11a, b, and g standards is implemented in a 0.18-μm CMOS process and packaged in a 48-pin QFN package. The transceiver achieves a receiver noise figure of 4.9/5.6 dB for the 2.4-GHz/5-GHz bands, respectively, and a transmit error vector magnitude (EVM) of 2.5% for both bands. The transmit output power is digitally controlled, allowing per-packet power control as required by the forthcoming 802.11 h standard. A quadrature accuracy of 0.3° in phase and 0.05 dB in amplitude is achieved through careful analysis and design of the I/Q generation parts of the local oscillator. The local oscillators achieve a total integrated phase noise of better than −34 dBc. Compatibility with multiple baseband chips is ensured by flexible interfaces toward the A/D and D/A converters, as well as a calibration scheme not requiring any baseband support. The chip passes ±2 kV human body model ESD testing on all pins, including the RF pins. The total die area is 12 mm^2. The power consumption is 207 mW in the receive mode and 247 mW in the transmit mode using a 1.8-V supply.**

***Index Terms*—Dual conversion, IEEE 802.11a/b/g, orthogonal frequency-division multiplexing (OFDM), receiver, RF CMOS, RF transceiver, synthesizer, transmitter, wireless LAN (WLAN).**

I. Introduction

LOCAL-AREA networks (LANs) are being deployed extensively worldwide using a well-established copper cable infrastructure. Wireless LANs (WLANs), on the other hand, have become available in the 2.4-GHz Instrumentation, Scientific and Medical (ISM) band [1] and are currently witnessing significant growth. A 2.4-GHz higher data rate (54 Mb/s) WLAN standard (802.11g) based on orthogonal frequency-division multiplexing (OFDM) has recently been ratified by the IEEE [1] to reduce multipath fading effects and to maintain robust system performance. 802.11g is also backward compatible to the already deployed 802.11 (1 and 2 Mb/s) and 802.11b standards (11 Mb/s). However, the 2.4-GHz ISM band is also used for other wireless standards including cordless phones and Bluetooth, which could cause interference leading to slower data rates for WLAN. 802.11a [1] operates in The Unlicensed National Information Infrastructure (UNII) 5-GHz band, which is "cleaner" and has more bandwidth to accommodate more WLAN channels at higher data throughput (54 Mb/s or higher), also using 64-quadrature-amplitude modulation (QAM) OFDM-type modulation.

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With the increasing demand for user capacity at higher data rates, WLAN chips must be able to cover WLAN standards in both the ISM and UNII bands for smooth migration to higher data rates and transition between different standards. In this context, a single-chip dual-band radio transceiver capable of supporting the three different WLAN standards (802.11a/b/g) should achieve the best performance/price ratio and is therefore a very desirable solution for WLAN applications.

Single-chip CMOS radio transceivers for wireless LAN applications targeting either the 5-GHz band (802.11a) or the 2.4-GHz band (802.11b) have recently been reported [2], [3]. Dual-band solutions have also been reported in SiGe technology [4] or in a two-chip CMOS solution [5]. This study describes a single-chip dual-band tri-mode 0.18-μm CMOS radio transceiver compliant with the IEEE 802.11a, b, and g standards.

Most of the previously reported WLAN RFICs are designed to work with a certain companion digital baseband chip. This limits the portability of the radio, i.e., its ability to operate with other digital basebands having different requirements or certain desirable functionalities. Particularly, in multiband multimode solutions, it is desirable that the choice of the digital baseband chip be relatively independent of the radio. To achieve maximum compatibility toward a multitude of baseband chips, a flexible baseband interface and autonomous calibration schemes were set as design goals for this chip, in addition to the obvious goals of good performance, low power, and low cost.

OFDM was chosen as the modulation in the 802.11a and g standards because of its good spectral efficiency and excellent tolerance of multipath fading channels. However, it poses additional requirements on the radio chip. Noise and linearity are of concern for any radio standard, but, in addition, OFDM requires excellent quadrature accuracy, both in phase and in amplitude [6]. Quadrature inaccuracy will cause some of the power of the $-n$th subcarrier to fold on top of the $+n$th subcarrier. Since the data content of the two subcarriers is highly uncorrelated, this will result in a reduced signal-to-noise ratio (SNR) and, hence, performance degradation. To guarantee good quadrature performance, a twofold approach was taken in this design. First, every measure was taken to make the quadrature accuracy natively as good as possible. Second, a possibility to further tune the phase and amplitude of the quadrature signals was implemented.

This paper is organized as follows. Section II describes the architecture of the chip, as well as the frequency planning. Section III covers the circuit design of the receiver, transmitter, and

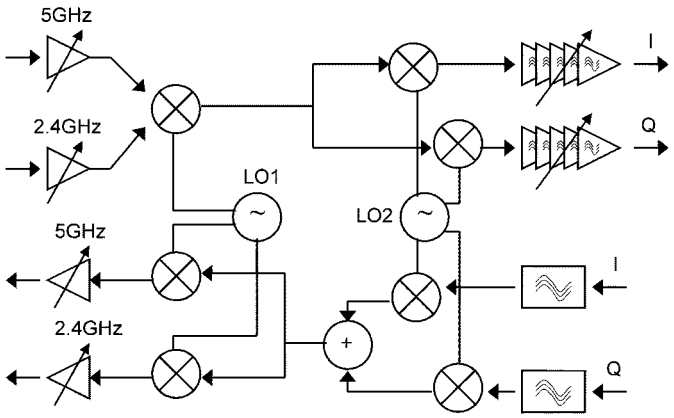

Fig. 1. Block diagram of the transceiver.

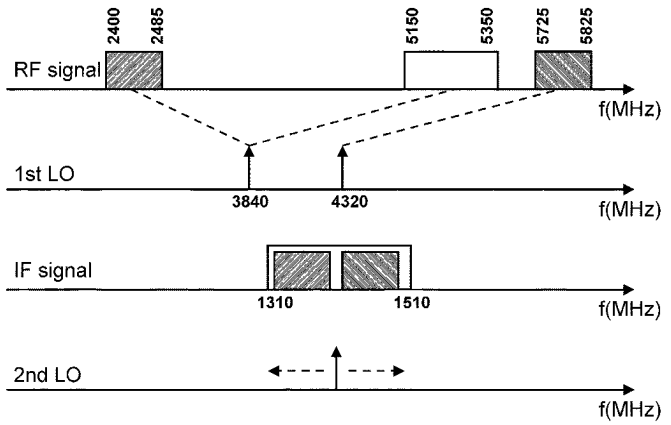

Fig. 2. Frequency plan of the transceiver.

frequency synthesizers, together with experimental results. Section IV describes the high-accuracy quadrature generation in more detail. Finally, Section V discusses the chip implementation and overall performance.

II. Architecture

The transceiver architecture (Fig. 1) is based on a wideband IF receiver and a two-step upconversion transmitter. The RF band, 5 GHz or 2.4 GHz, is first downconverted to a common IF frequency using a fixed first local oscillator (LO1). The LO1 frequency is chosen to be approximately halfway between the two RF bands. The IF signal (1300–1500 MHz) is then down converted to baseband using a complex I/Q mixer. The channel is selected using a variable second local oscillator (LO2) for the IF to baseband down conversion. Channel selection filtering is done at the baseband. In addition to the blocks shown in Fig. 1, the chip also integrates a crystal oscillator generating the 20-MHz reference for the phase-locked loops (PLLs), a bandgap bias generation block, a received signal strength indicator (RSSI), and a four-wire serial digital interface for programming various radio parameters. All of the signal paths are fully differential, although the architecture diagram is single-ended for simplicity.

Fig. 2 shows the frequency plan adopted in this design. It has three fundamental benefits: inherent image rejection, excellent quadrature accuracy, and maximum hardware share between the frequency bands. Since the separation between the wanted signal and the image at IF is almost 3 GHz, no image rejection scheme, on or off chip, is required. The implicit bandpass characteristics of a simple RF-band select filter, the input matching and the low-noise amplifier result in a measured image rejection of 73 and 56 dB for the 2.4- and 5-GHz bands, respectively. To reach the maximum sensitivity of the 5-GHz receiver in environments where very strong 2.4-GHz band signals are present, a steeper band select filter may be required.

The 5-GHz band, which is almost 1 GHz wide, is translated to a much narrower band in IF. This relaxes the design requirements of the LO2 circuitry, resulting in improved phase-noise performance. LO1, although operating at a high frequency, only needs to lock to a few distinct frequencies with a large step size. This allows a low division ratio in the LO1 PLL, resulting in lower phase noise. More importantly, I/Q modulation and demodulation is moved to the IF range which makes accurate quadrature generation easier. This multiband multistandard architecture achieves maximum hardware share resulting in considerable savings in chip area. The LNAs, TX RF mixers, and preamplifiers are the only parts that are not shared. The architecture supports the entire 5-GHz band (4.9–5.9 GHz). However, the implementation reported here is optimized for the lower 5-GHz band only (5.15–5.35 GHz).

A potential hazard in this kind of an architecture would be harmonic mixing. A strong neighboring channel could get downconverted on top of the wanted channel by the harmonics of the local oscillators. In this design, the LO frequencies were carefully chosen to avoid the problem. In fact, the lowest order harmonic product falling in band is $4 \times \text{LO1-}7 \times \text{LO2}$. Harmonics of this high order are obviously not very high in power.

III. Circuit Design

A. Receiver

The receiver has two differential cascode LNAs, one for each band, providing the necessary front-end gain and low noise. The unused LNA is always switched off to minimize the overall current consumption. The LNA inputs are internally matched using a detailed package model and an on-chip LC network. The input impedance as seen from outside the package is 100-Ω differential. After the LNAs, the rest of the receiver chain is shared between the two frequency bands. The LNAs drive a dual-input RF mixer which translates the RF signals to the IF band. Quadrature demodulation is then performed by the IF mixers. The quadrature baseband signals are further processed in the receiver baseband. The baseband consists of a fourth-order Butterworth opamp-*RC* channel-select filter, a variable-gain amplifier, and an RSSI. The filter attenuates the strongest adjacent channel signals allowed by the 802.11b standard to approximately the same level as the wanted signal, but not below it. Therefore, some additional digital filtering may be required, depending on the baseband chip. The cutoff frequency of the filter is automatically calibrated to 10 MHz with an absolute accuracy of 5% at power-up. The calibration uses a test integrator to calibrate the *RC* product against the 20-MHz crystal oscillator clock [7]. The measured average mismatch between the cutoff frequencies of the I- and Q-branch filters is less than 0.25%.

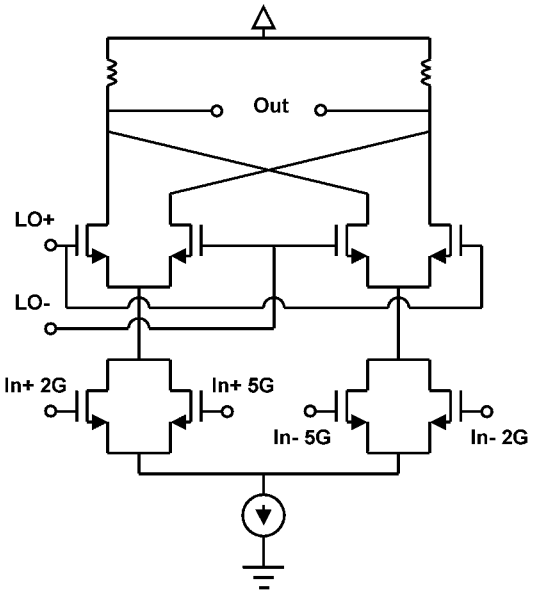

Fig. 3. Simplified schematic of the dual-input RF-to-IF receiver mixer.

To ease the linearity requirements of the mixers and the baseband, the LNAs are designed to provide two different gain settings (25/0 dB). The maximum receiver gain is more than 80 dB, and the gain control range is 75 dB. To accommodate a variety of different analog-to-digital converters (ADCs), the common-mode voltage of the I/Q outputs is adjustable from 0.55 to 1.25 V and can either be set internally or from an external source. The baseband variable-gain amplifier provides 50 dB of controllable gain in 0.8-dB steps. The gain is controlled by the baseband chip through a parallel digital bus in order to achieve a sufficiently fast gain switching (measured gain switching time is 200 ns).

The receiver architecture originally called for two different RF mixers, one for each band. Using a differential architecture and a traditional inductively degenerated Gilbert cell mixer, this would have required two load inductors and two degeneration inductors in each mixer, resulting in a total of eight on-chip inductors. However, to save area, the two mixers are merged into a single dual-input mixer, as shown in Fig. 3. Since the output frequency of the mixers is the same, the switching stages and loads can be shared between them. There are two parallel input pairs, one for each frequency band, and the active input is selected by changing the dc biasing of the input devices. However, inductive degeneration is no longer possible, since the source node of the input pairs now has two possible operating frequencies. With no feedback left, the bias current of the RF input devices has to be increased to maintain adequate linearity. Other than the increased bias current, there is no penalty in combining the two mixers. The resulting mixer reduces the silicon area dramatically by eliminating six of the original eight inductors, while still maintaining nearly equal performance. Furthermore, the IF mixers use resistive rather than inductive degeneration and adopt a current mode interface to the analog baseband, resulting in simplified circuitry while maintaining good linearity.

In any design having high gain at low frequency, dc offset must be taken care of. In this design, the receiver baseband filter has two highpass poles, one in front of the variable-gain amplifier to handle offsets from the preceding stages, and a servo loop to handle the offsets of the low-pass filter itself. The placement of these poles cannot be done arbitrarily. The 802.11a and g standards allow a $\pm$20-ppm frequency error. In the worst case, where both the transmitting radio and the receiving radio have the maximum error, the frequency offset can be as high as 214 kHz, while the center frequency of the first OFDM subcarrier is only 312.5 kHz. If the highpass cutoff frequency of the baseband filter is too high, the lowest subcarriers will get severely attenuated by the filter, thus degrading the receiver performance. In [8], this issue was handled by an automatic frequency control (AFC) algorithm that corrected for any frequency offsets in the downconversion stage. The AFC algorithm, however, requires support from the baseband chip, and one of the goals in this design was to be independent of the baseband. The approach taken here is to place the highpass filter poles low enough so as not to cause any performance degradation even in the presence of a worst-case frequency offset. The first and second highpass poles are at $<$200 Hz and $<$1 kHz, respectively, in any process corner. According to system simulations, much higher pole frequencies would suffice in additive white Gaussian noise (AWGN) channels, even with maximum allowed frequency offsets. However, in multipath fading channels, these very low pole frequencies are required to cause no noticeable performance degradation in any conditions.

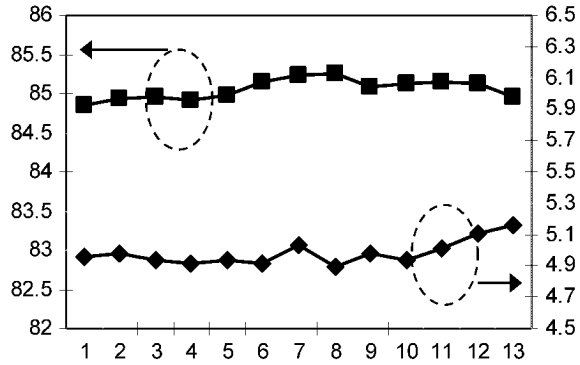

Fig. 4. Measured gain and NF of the 2.4-GHz receiver as a function of channel number.

A common problem in variable-gain amplifiers with offset compensation is that the offset changes when the gain is changed, and the offset settling is very slow due to the low cutoff frequencies of the highpass filters. In this chip, the variable-gain amplifier was designed in such a way that the bias conditions of the amplifying devices are constant for all gain settings, and therefore their offset is also constant. Thus, the output offset of the variable-gain amplifier is to a first order not affected by gain switching, and therefore the low cutoff frequencies of the highpass filters do not cause problems. Second-order effects, like charge redistribution, can cause small offset changes, but the measured offset step due to a gain change never exceeds 10 mV.

Fig. 4 shows the measured gain and noise figure (referred to the differential input of the chip) of the 2.4-GHz receiver as a function of the channel number, and Fig. 5 shows the same measurement for the 5-GHz receiver. A statistical measurement of a hundred samples on a middle channel gives an average gain of 85 dB/83 dB with a standard deviation of 0.5 dB/0.6 dB for

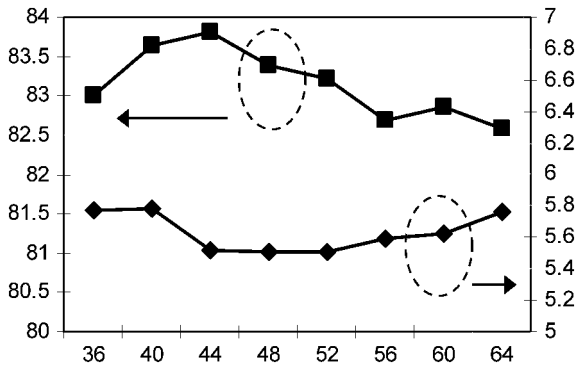

Fig. 5. Measured gain and NF of the 5-GHz receiver as a function of channel number.

the 2.4-GHz/5-GHz receivers, respectively. The corresponding average noise figure is 4.9 dB/5.6 dB with a standard deviation of 0.15 dB/0.13 dB. The sensitivity of the receiver depends not only on the radio chip but the baseband chip as well. However, estimates can be given based on the measured receiver EVM of the radio chip. Assuming that the signal-to-noise ratio (SNR) requirement of the baseband chip for the 54-Mb/s data rate is 20 dB, we define the "sensitivity" of the receiver as the input level where the receiver EVM exceeds 10%. Both the 2.4-GHz and the 5-GHz receivers achieve better than 10% EVM down to an input power level of −75 dBm.

B. Transmitter

The transmitter path is shared between the two frequency bands up to the intermediate frequency. The RF mixers and the preamplifiers are separate for the two bands. The transmitter has 30 dB of power control range in 2-dB steps, all of which is implemented in the preamplifiers. Implementing the power control in the RF part, after all filtering, allows the power control to be very fast (switching time of less than 300 ns). To eliminate any additional delays caused by the serial bus interface, the output power is controlled through a parallel digital bus (pins shared with the RX AGC). The fast power control is implemented in anticipation of the forthcoming 802.11 h standard, which will require per-packet power control. Implementing the power control solely in the preamplifiers also saves power when the maximum output power is not needed. The supply current of the chip in transmit mode is reduced from 137 mA at the full output power to only 75 mA at the lowest output power level.

To accommodate different digital-to-analog converters (DACs), a flexible input buffer was designed for the transmit baseband filter. The buffer has complementary input pairs (both an NMOS and a PMOS differential pair) to accommodate any common-mode level between 0.4–1.2 V with a very high input impedance. Furthermore, the input buffer can be bypassed, thereby allowing common-mode voltages down to 0 V, although with a lower input impedance of 8 kΩ. The TX low-pass filter is a fourth-order Chebyshev with a cutoff frequency of 10 MHz, calibrated with the same engine as the receiver filter to an accuracy of 5%. As in the receiver filters, the measured average mismatch between the I- and Q-branch filter cutoff frequencies is less than 0.25%.

Fig. 6 shows the measured spectrum mask and the signal constellation diagram of the 2.4-GHz transmitter, measured at the highest data rate supported by the 802.11g standard, 54-Mb/s. Fig. 7 shows the same measurement for the 5-GHz transmitter. Both measurements show good margin to the spectrum mask, allowing for signal degradation in the external power amplifier. A measurement of 100 samples on a middle channel gives an average EVM of 3.1%/3.4% with a standard deviation of 0.2%/0.2% for the 2.4-GHz/5-GHz bands, respectively, measured at the maximum output power of −4 dBm.When the output power is backed off by 2–3 dB, a minimum EVM of 2.5% is achieved at both frequency bands.

C. Frequency Synthesis

Two separate PLL frequency synthesizers are used for the required LO1 and LO2 signals. An integer-N PLL architecture is employed in both synthesizers. The synthesizers are fully integrated, except for the passive loop filters which reside off chip. The LO1 synthesizes the fixed RF LO (3840 MHz) from a 20-MHz reference signal, generated by an on-chip crystal oscillator. The LO2 synthesizes the variable-frequency IF LO with a 1-MHz step in the frequency range of 1300–1500 MHz.

The LO1 voltage-controlled oscillator (VCO) uses only PMOS devices due to lower flicker noise contributions. The VCO tank consists of a center-tapped (differential) inductor, accumulation-mode NMOS varactor diodes, and switched capacitors. Critical performance parameters in this VCO design are phase noise, flicker noise corner, supply sensitivity, bias current sensitivity, harmonic levels, and power consumption.

The reference bias current for the VCOs is taken from an on-chip bandgap circuit. This reference current is distributed to the LO1 blocks. The reference current noise seen by the VCO is the sum of bandgap and bias mirrors noise; this noise is converted to phase noise in the VCO. To reduce the bias-induced noise, a dynamic bias filter was developed. The voltage in the bias node is filtered using an *RC* filter with a very low cutoff frequency of 2.5 kHz. A low cutoff frequency, however, translates into a long startup time for the VCO. Therefore, a bypass switch shorts the resistor in the *RC* filter for a short period of time to speed up the startup. Another purpose of the bias filter is to suppress bias sensitivity of the VCO. The reference bias current from bandgap is disturbed during RX-to-TX or TX-to-RX switching. A dynamic transient disturbance occurs in the bandgap generated bias current during the switching since a large amount of dc current is switched (in the order of 100 mA). This dynamic variation in the reference current, in turn, could result in disturbance in VCO output frequency and could pull the PLL out of lock.

Fig. 8 shows the composite phase noise of the two synthesizers, measured at the output of the preamplifier. The dominant phase noise contributor at large offset frequencies is the LO1 VCO. The close-in phase noise, on the other hand, is dominated by the crystal oscillator. The integrated phase noise of the frequency synthesizers is less than −34 dBc (1.1°), which exceeds the 64-QAM performance requirements for 802.11a/g. The phase noise profile is somewhat different from traditional PLL designs, because the loop parameters were optimized with two conflicting goals: low phase noise and good stability during

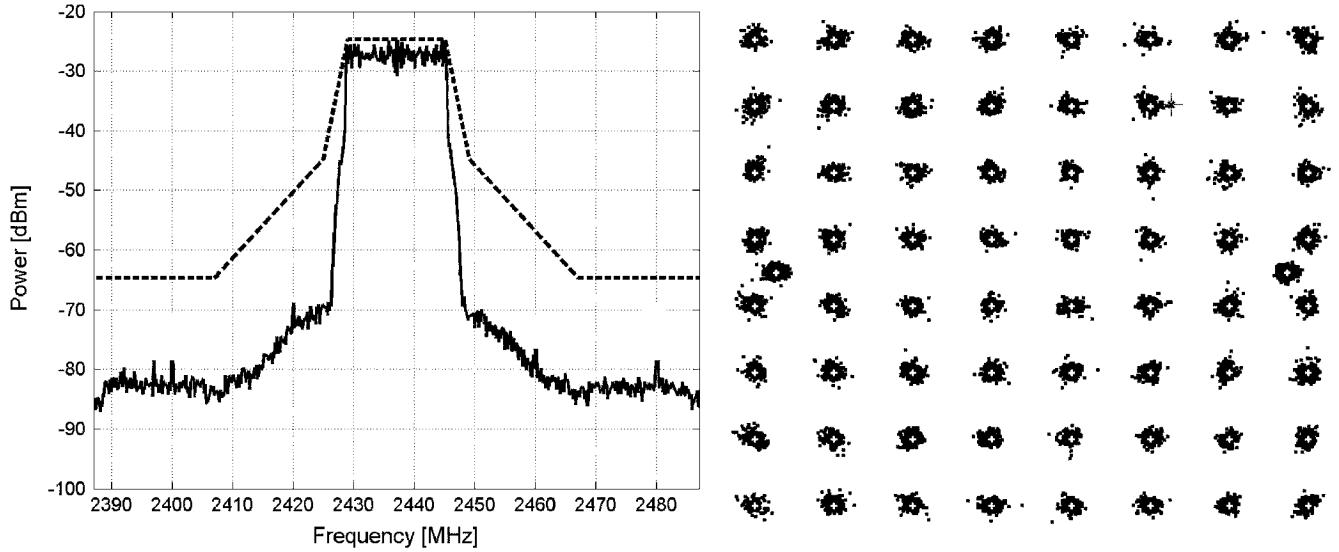

Fig. 6. Measured spectrum mask and signal constellation diagram of the 2.4-GHz transmitter.

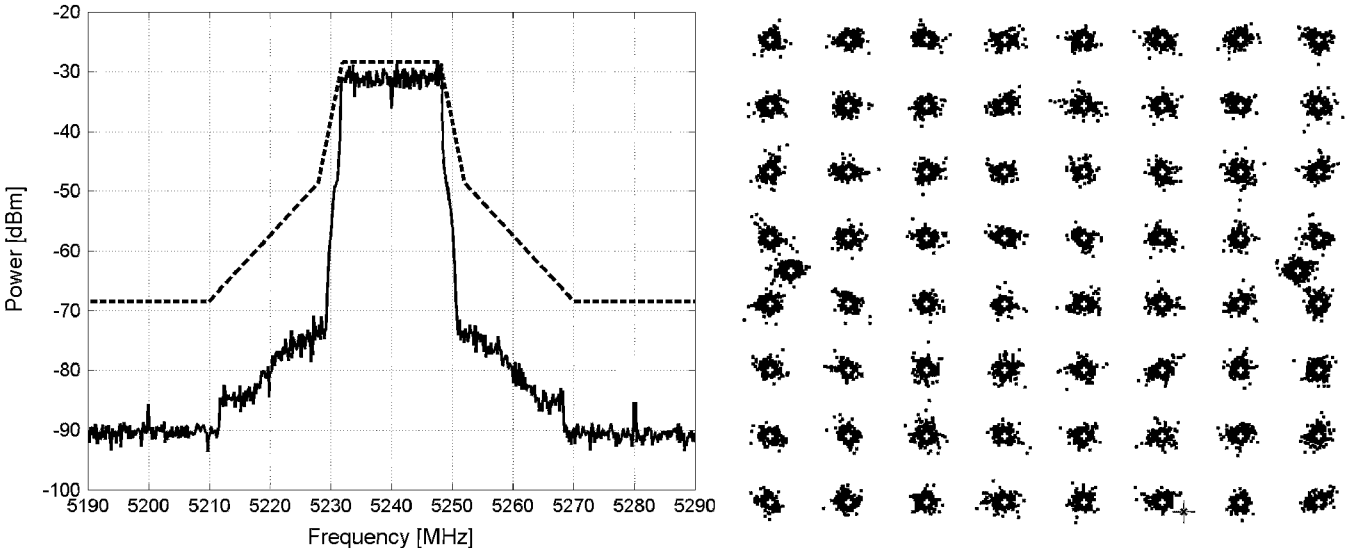

Fig. 7. Measured spectrum mask and signal constellation diagram of the 5-GHz transmitter.

TX-to-RX turnaround when the supply, ground, and bias lines can experience serious disturbance.

IV. High-Accuracy Quadrature Generation

In complex modulation schemes, such as 64-QAM, the quadrature accuracy (both phase and amplitude) is extremely important. Typically, a phase accuracy better than 1° and an amplitude accuracy better than 1% are required to guarantee that the quadrature inaccuracy is not limiting the overall performance. In previously published work [9], [10], the required accuracy is only achievable with the help of calibration algorithms, requiring support from the baseband chip. However, as stated before, one of the main targets for this work was that the radio chip should be as independent of the baseband IC as possible. Therefore, the RFIC should meet the accuracy requirements without calibration.

In this design, the quadrature LO signals for the IF mixers are generated with a second-order *RC–CR* polyphase filter. The transfer function of the polyphase filter from the LO input to the

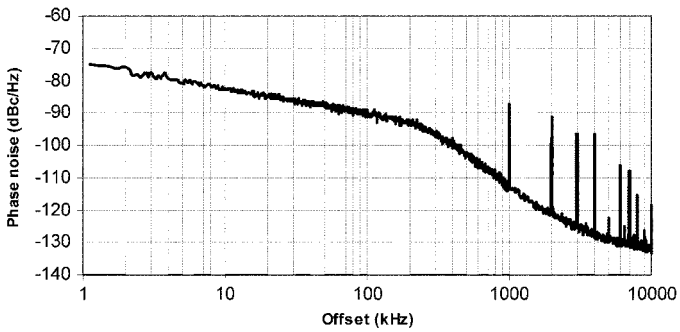

Fig. 8. Composite phase noise of the two PLLs, measured at the output of the preamplifier.

I/Q outputs is perfectly symmetrical only for the fundamental tone. Harmonic tones will have asymmetric transfer functions, resulting in different waveforms at the in-phase and quadrature outputs. Any differences in the waveform shape will cause the zero crossing points of the waveforms to vary. After amplification in the limiting buffers feeding the mixers, the differences in zero crossing points will translate into a quadrature phase error.

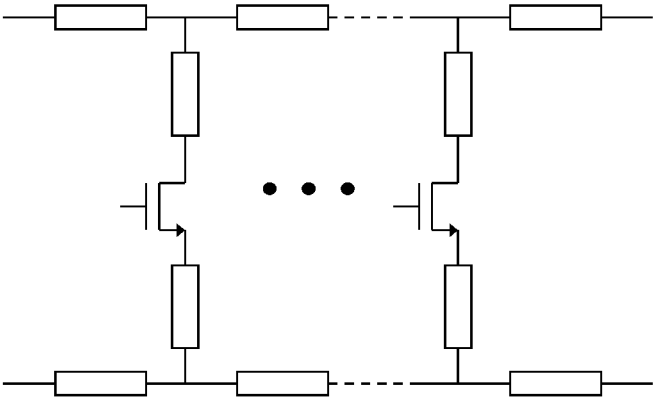

Fig. 9. Switchable resistive ladder implementing the amplitude tuning.

Thus, to achieve a good quadrature accuracy, the harmonic content of the signal going into the polyphase filter must be minimized. To accomplish this, a linear buffer is used between the VCO and the polyphase filter, so that the signal entering the polyphase filter is as purely sinusoidal as possible. A sinusoidal LO signal, however, is not optimal for the mixers. Therefore, the quadrature signals from the polyphase filter are amplified using limiting buffers before feeding them into the mixers. There are separate limiters for the RX and TX mixers. This allows placing them physically very close to the mixers, thus reducing the capacitive loading seen by the limiters.

Since different baseband chips have different requirements for quadrature accuracy, tuning mechanisms for both the phase and amplitude balance were also built in. This ensures that the radio chip can meet even the most stringent balance requirements, even if the native quadrature accuracy would not be good enough for a particular baseband chip. The calibration engine for the quadrature accuracy tuning, however, is not implemented on chip. Therefore, if calibration should be needed, it will require support from the baseband chip.

The quadrature amplitude tuning circuit, shown in Fig. 9, is a simple switchable resistive ladder, placed between the baseband filter and the output driver in the receive path and between the baseband filter and the IF mixer in the transmit path. The amplitude of each channel is controlled by a 4-b control word with a step size of 0.05 dB, resulting in a total tuning range of ± 0.8 dB. However, the tuning is typically not needed at all; a statistical measurement of a hundred samples shows an average amplitude error of 0.05 dB with a standard deviation of 0.03 dB without tuning, which is more than good enough.

The quadrature phase tuning is implemented in the limiting buffers driving the second LO signal to the mixers. In principle, the phase tuning could be implemented in the signal path as well, but it would have to be linear and broadband. When implemented in the LO path, the tuning only needs to operate at a point frequency, and linearity is not as much of a concern. The last stage of the limiting buffer, shown in Fig. 10, is a pair of source followers that drive the mixer LO ports. The phase tuning is done by changing the bias current through one of the source followers slightly. The change in the drain current causes the gate–source capacitance of the source follower to change, thereby changing the phase of the signal. As long as the required change in phase is small, the resulting amplitude imbalance is negligible. The current in the limiters in both channels

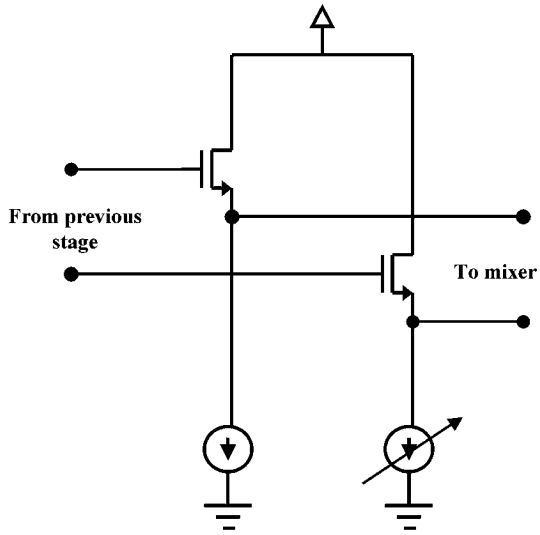

Fig. 10. Quadrature phase-tuning implementation in the limiting buffer.

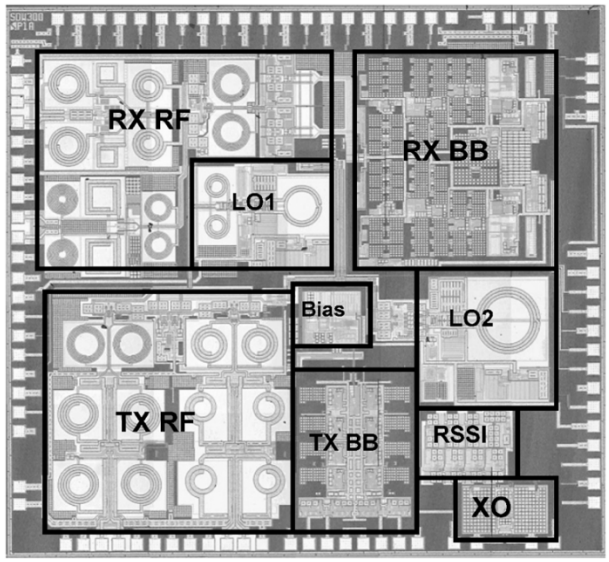

Fig. 11. Chip microphotograph.

is controlled by a 4-b control word with a step size of 0.25°, resulting in a total tuning range of $\pm 4°$. Since there are separate limiters for the receive and transmit mixers, the phase balance in the receiver and the transmitter can be controlled independently. However, as was the case with the amplitude tuning, the phase tuning is typically not needed at all. A statistical measurement of a hundred samples shows an average quadrature error of 0.3° (averaged over all OFDM subcarriers) with a standard deviation of 0.3° without tuning, i.e., the native quadrature balance is excellent.

V. Chip Implementation and Performance Summary

The transceiver has been implemented in a 0.18-μm single-poly six-metal CMOS process and occupies a total die area of 12 mm^2. It is packaged in a 48-pin QFN package with an exposed ground paddle. A die microphotograph is shown in Fig. 11. To provide better isolation between different blocks, the chip is divided into five supply domains. The grounds for these domains are all downbonded to the ground

TABLE I
TRANSCEIVER PERFORMANCE SUMMARY

Parameter	2.4GHz	5GHz
Supply voltage	1.8V±10% (I/O 1.6V-3.6V)	
Supply current RX mode TX mode	 115mA 137mA	 118mA 137mA
RX chain noise figure	4.9dB	5.6dB
RX chain gain (max / min)	85dB / 8dB	83dB / 9dB
RX chain IIP3 (min / max gain)	-1dBm / -26dBm	-1dBm / -23dBm
TX max output power	-4dBm (EVM 3.2%)	-4dBm (EVM 3.6%)
TX minimum EVM	2.5% (@ -6dBm)	2.5% (@ -7dBm)
TX OIP3	+17.3dBm	+13.3dBm
LO integrated phase noise	-34dBc (1.1°)	
I/Q amplitude balance	0.05dB	
I/Q phase balance	0.3°	
ESD tolerance (all pins)	>2kV HBM	

paddle of the package, while the supplies are combined on the printed circuit board level. The coupling between the on-chip inductors and nearby interconnects was modeled through 2.5-dimensional electromagnetic simulations. This allowed minimizing the empty space required around the inductors, thus reducing the overall die area.

The chip passes full ±2-kV human body model (HBM) ESD testing on all pins. The 2.4-GHz RF pins employ the standard analog ESD protection provided by the foundry, i.e., reverse-biased P+/N-well diodes connected between the signal path and the supply rails. For the 5-GHz RF pins, the junction capacitance of the standard diodes degraded the performance too much, and the diode area had to be significantly reduced. The limit of performance degradation was set to a maximum 0.5-dB increase in receiver noise figure and a maximum 0.5-dB decrease in output power. Simulating the ESD performance of the modified protection circuitry using standard circuit simulation tools is extremely difficult, if not impossible. However, comprehensive testing shows that even the reduced diodes provide the required ±2-kV ESD robustness.

The chip consumes 207 mW in the receive mode and 247 mW in the transmit mode, while transmitting at full output power. The transmit mode power consumption is a strong function of the output power, reducing to 135 mW at the lowest output power level. The supply voltage of the entire chip is 1.8 V, except for the digital I/Os that support supply voltages up to 3.6 V to comply with standard 3.3-V I/Os in most baseband chips. The key performance parameters of the chip are summarized in Table I.

VI. CONCLUSION

This paper presented a dual-band tri-mode WLAN CMOS radio transceiver solution having the smallest die size and lowest power consumption reported to date. The wideband IF architecture used provides implicit image rejection and maximum hardware share between the two bands. The chip is designed to work with a multitude of different baseband chips. The key features enabling this are flexible interfaces toward A/D and D/A converters, autonomous calibration schemes, and excellent native quadrature accuracy. Calibration schemes for both amplitude and phase of the quadrature signals are also presented, in case even better accuracy is required. The experimental results show high performance with small chip-to-chip variations, allowing for high yield.

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