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A Single-Chip Dual-Band Tri-Mode CMOS Transceiver for IEEE 802.11a/b/g Wireless LAN

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***Abstract*—A single-chip dual-band tri-mode CMOS transceiver that implements the RF and analog front-end for an IEEE 802.11a/b/g wireless LAN is described. The chip is implemented in a 0.25-μm CMOS technology and occupies a total silicon area of 23 mm^2. The IC transmits 9 dBm/8 dBm error vector magnitude (EVM)-compliant output power for a 64-QAM OFDM signal. The overall receiver noise figure is 5.5/4.5 dB at 5 GHz/2.4 GHz. The phase noise is −105 dBc/Hz at a 10-kHz offset and the spurs are below −64 dBc when measured at the 5-GHz transmitter output.**

***Index Terms*—Frequency synthesizer, IEEE 802.11a, IEEE 802.11b, IEEE 802.11g, low-noise amplifier (LNA), orthogonal frequency-division multiplexing (OFDM), power amplifier, RF transceiver, wireless LAN (WLAN).**

I. Introduction

RECENT years have seen the rapid deployment of wireless local area networks (WLANs) in offices, homes, and hot spots, and numerous descriptions of single-mode WLAN CMOS transceivers have been published [1]–[7]. However, the proliferation of multiple IEEE 802.11 WLAN standards has created the need for integrated low-cost multimode multiband transceivers [8]–[13] that can enable seamless connectivity for mobile users as they roam between access points operating with different WLAN standards. The three popular WLAN standards in use today are based on the IEEE 802.11a [15], 802.11b [16], and 802.11g [17] specifications. The 802.11a standard, which was ratified in 1999, operates in the 5-GHz unlicensed national information infrastructure (UNII) band. The UNII band consists of two subbands:[1] 5.15 to 5.35 GHz, and 5.725 to 5.825 GHz, which together provide a total bandwidth of 300 MHz and offer 12 nonoverlapping data channels of 20 MHz each. The 802.11a standard employs orthogonal frequency-division multiplexing (OFDM) modulation with 52 subcarriers. Each of the subcarriers can be a BPSK, QPSK, 16-QAM, or 64-QAM signal. The OFDM modulation provides a data rate that ranges from 6 to 54 Mb/s. Although the 802.11b standard was ratified at the same time as the 802.11a, 802.11b products were commercially available a couple of years earlier, making 802.11b the incumbent standard. The 802.11b standard operates in the 2.4-GHz ISM band with an aggregate bandwidth of 83.5 MHz and a total of 11 channels, only three of which are nonoverlapping. It employs direct sequence spread spectrum (DSSS) modulation for data rates of 1–2 Mb/s and complementary code keying (CCK) modulation for data rates of 5.5–11 Mb/s. The 802.11g standard, which was ratified in June 2003, shares the same three nonoverlapping channels in the 2.4-GHz band with the 802.11b standard. The 802.11g can provide either the high data rate of the 802.11a or 802.11b compatibility, but not at the same time. In a legacy 802.11b network, an 802.11g device will operate in the DSSS/CCK mode with data rates of 1–11 Mb/s. In an 802.11g network with no legacy 802.11b devices, 802.11g devices will operate in the OFDM mode with data rate of 6–54 Mb/s.

This paper describes a single-chip dual-band tri-mode CMOS transceiver that supports the IEEE 802.11a/b/g WLAN standards. The transceiver operates in both the 2.4- and 5-GHz unlicensed frequency bands. It has fully integrated synthesizers and transmit and receive chains, including on-chip baseband gm-C filters, synthesizer loop filters, and voltage-controlled oscillators (VCOs). Section II discusses the architectural design of this dual-band transceiver. The implementation details are presented in Section III, and the experimental results are summarized in Section IV.

II. Architecture

Fig. 1 shows a block diagram of the implemented multistandard WLAN system consisting of an RF transceiver and a companion digital baseband chip. The RF transceiver consists of a dual-band receiver, a dual-band transmitter, and a frequency synthesizer. The companion baseband chip integrates all of the digital PHY and MAC functions, as well as two 9-b pipelined ADCs and two 9-b D/A converters (DACs) operating at 88 and 176 MS/s, respectively. The 5- and 2.4-GHz RF signals are connected to two dual-band antennas through on-board transmit/receive selection and antenna diversity switches. Optional external low-noise amplifiers (LNAs) and power amplifiers (PAs) can be used to enhance the receive sensitivity and boost the transmitter output power.

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[1]An additional 255 MHz is being added to the 5-GHz band. U.S., European, and other delegations at the 2003 International Telecommunications Union World Radio Conference (WRC-03) agreed to globally allocate 5.15–5.35 GHz and 5.47–5.725 GHz for a total of 455 MHz for WLAN devices globally.

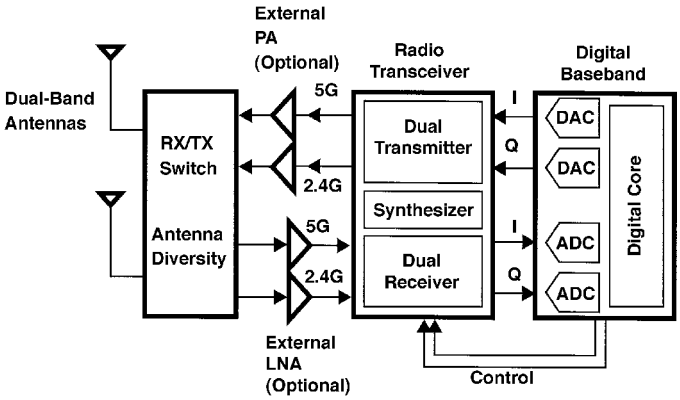

Fig. 1. RF system block diagram.

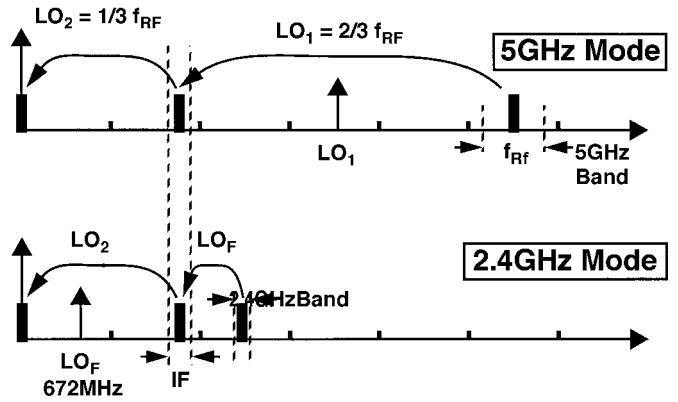

Fig. 2. Dual-band receiver frequency plan.

This radio uses a sliding intermediate frequency (IF) architecture [1]. The dual-band design relies heavily on reusing circuit blocks between different modes of operation so as to reduce the overall die area. The 2.4-GHz and 5-GHz transceivers share common IF and baseband circuits on both the transmitter and receiver. However, each frequency band has dedicated RF circuits. Fig. 2 shows the frequency plan from the viewpoint of the receiver. In the 5-GHz mode of operation, the RF signal is downconverted to the IF and consequently to the baseband by the local oscillators (LOs). LO_1 at 2/3 of f_{RF} is generated by a programmable frequency synthesizer. LO_2 at one third of f_{RF} is generated from LO_1 with a divide-by-two. With this sliding IF architecture, LO_1, LO_2, and, therefore, the IF, change or *slide* with the RF channel frequency. This choice of one third and two thirds of f_{RF} for the LO frequencies provides a large separation of more than 3.5 GHz between the desired RF channel and its image frequency so that no receive image rejection mixer is needed. In the 2.4-GHz mode, a different fixed frequency synthesizer at LO_F of 672 MHz is used to down convert the RF signal to the same IF as in the 5-GHz mode. Channel selection is performed by LO_2, which is generated by the same synthesizer as in the 5-GHz mode. The transmitter uses the same frequency plan as the receiver. There are two frequency synthesizers on this chip: a programmable frequency synthesizer that generates LO_1 and LO_2 at 2/3 and 1/3 of f_{RF} in the 802.11a mode as well as LO_2 in 802.11b mode and a fixed frequency synthesizer that produces the offset LO_F at 672 MHz for the 2.4-GHz mode of operation.

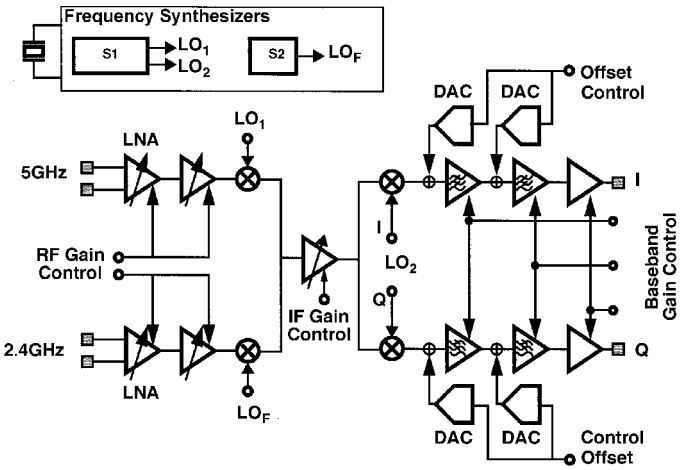

Fig. 3. Dual-band receiver block diagram.

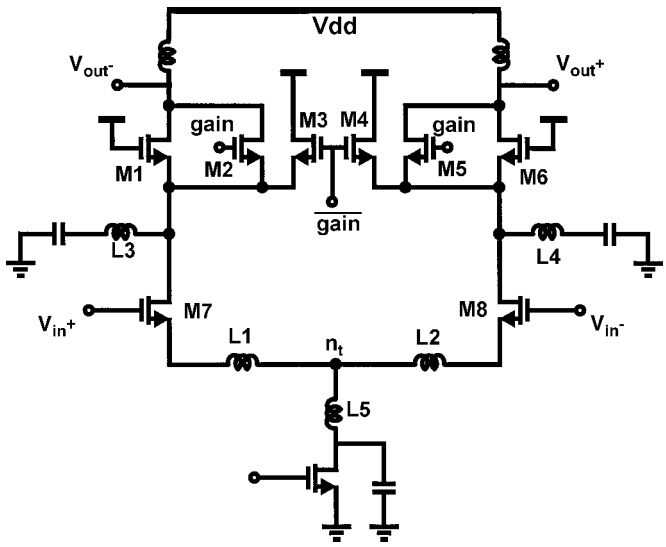

Fig. 4. Schematic of the 5-GHz LNA.

III. Implementation

A. Receiver

Fig. 3 shows a detailed block diagram of the dual-band receiver. The RF signals in 2.4 and 5 GHz are amplified by their corresponding LNAs and RF variable-gain amplifiers (VGAs) before being downconverted to a common IF of approximately 1.7 GHz. This IF signal is further mixed down to quadrature baseband I and Q signals with LO_2. Channel select filtering is performed using on-chip baseband gm-C filters. The dc offsets in the baseband filters are cancelled using two pairs of 6-b DACs controlled by the companion baseband IC on a per-packet basis [2]. The receiver has a programmable gain of up to 90 dB, approximately evenly split between RF and baseband. The overall receive chain noise figure is 5.5 dB for the 5-GHz mode and 4.5 dB for 2.4-GHz operation.

The schematic of the 5-GHz LNA with improved compression and common-mode rejection is shown in Fig. 4. The amplifier consists of a cascoded differential pair that is optimized for a low noise figure. When a large input RF signal is applied, the LNA is switched to a low-gain mode to avoid signal compression. The gain reduction is achieved by transistors M2–M5

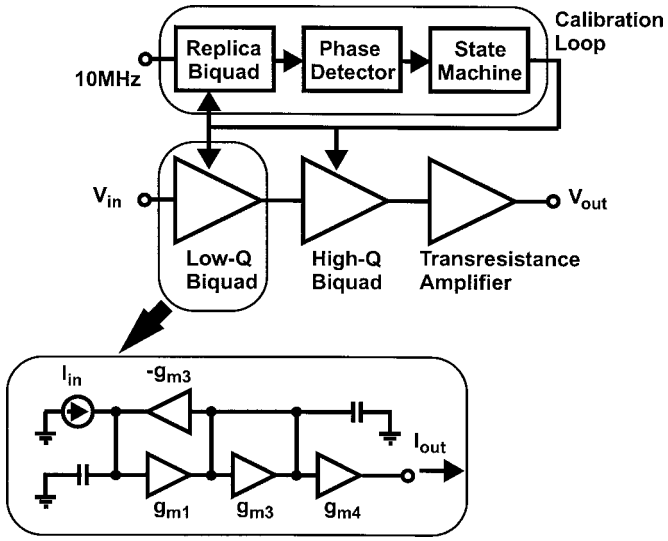

Fig. 5. Receive baseband filter.

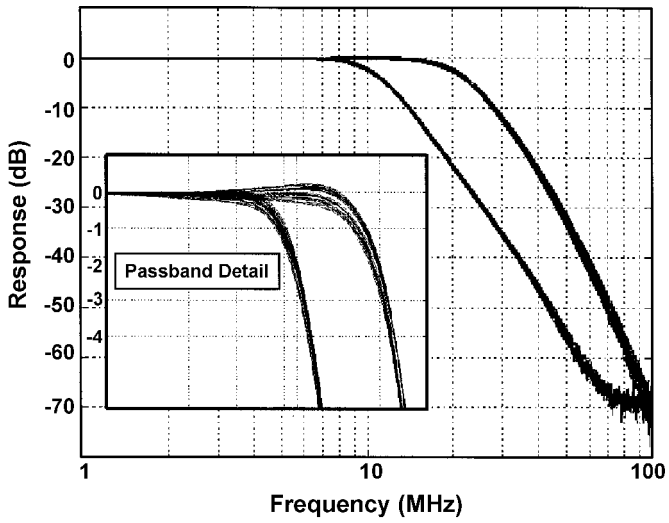

Fig. 6. Frequency response of the receive baseband filter.

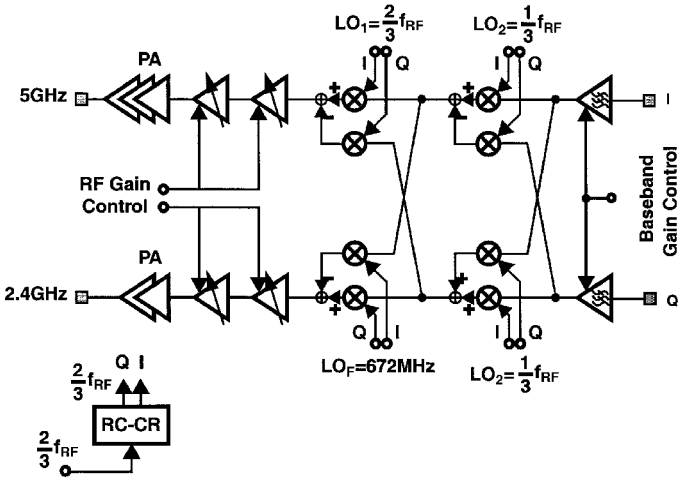

Fig. 7. Dual-band transmitter block diagram.

acting as a pair of current switches that reduce the output signal by shunting signal current away from the inductive load. The accuracy of this gain change depends on matching of transistor sizes and is very well controlled over all process and temperature corners. To reduce the noise contribution of the cascode devices, the parasitic capacitances at the cascode nodes are resonated out by inductors L3 and L4. Inductor L5 improves the common-mode rejection of the LNA by tuning out the parasitic capacitance at the tail node of the differential pair M7 and M8. The increased common-mode impedance at the tail node improves the common-mode rejection and thereby permits the LNA to be used with a single-ended RF input, eliminating the need for a balun.

The receiver baseband filters, shown in Fig. 5, implement a fourth-order Butterworth low-pass characteristic with a selectable cutoff frequency of either 10 or 20 MHz. This Butterworth low-pass filter, when combined with subsequent filtering in the digital domain, meets the receiver blocker rejection requirement. The four filter poles are constructed by cascading two biquad filter sections. Each biquad is implemented using a gm-C architecture, and is tunable by means of digitally controlled capacitor arrays. A calibration loop that consists of a replica biquad block, a phase detector, and a state machine selects the appropriate capacitor setting. If the biquad is tuned exactly to the cutoff frequency, the filter output will be phase shifted by exactly 90° with respect to the reference input. If the biquad is tuned low, the phase shift will be more than 90° and the state machine will attempt to subtract capacitance until the phase shift reaches 90°. The measured frequency response of the baseband filters over process and temperature variations for programmed bandwidths of 10 and 20 MHz, illustrated in Fig. 6, shows that the filter response varies by less than 0.3 dB in the passband, which far exceeds the ±2-dB flatness required of the transmitter [15].

B. Transmitter

Fig. 7 shows a block diagram of the dual-band transmitter. The quadrature baseband I and Q signals generated by the DACs in the companion digital chip are current inputs to the transmitter. The inputs are first filtered by reconstruction filters and then mixed up to the 1.7-GHz IF. Depending on whether the transmitter is operating in the 2.4-GHz or 5-GHz mode, the IF signal is upconverted by LO_F or LO_2. Image reject mixing is required in the transmitter in order to avoid the need for an IF filter. The quadrature LO_2 and LO_F for the mixers in Fig. 7 are provided directly from the synthesizers, whereas the quadrature LO_1 for the RF mixer is generated locally using an *RC–CR* filter. After passing through the RF variable gain stages, the RF signal in each path drives the on-chip PA.

The transmit baseband filter shown in Fig. 8 has a third-order Butterworth low-pass response with a programmable cutoff frequency of either 15 or 30 MHz. The transmit reconstruction filter is more relaxed than the receive baseband filter because it only needs to attenuate the spectral images of the DACs. The filter corner frequencies are chosen to guarantee passband flatness as well as stopband rejection over all design corners so that there is no need for automatic tuning.

A class-A PA for an OFDM system that transmits error vector magnitude (EVM)-compliant and spectral-mask-compliant power must satisfy a very strict linearity requirement. This linearity constraint can, in turn, translate into high power

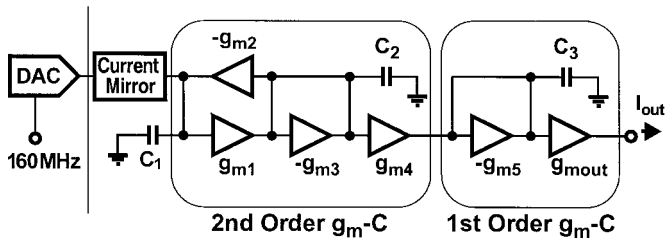

Fig. 8. Transmit baseband filter.

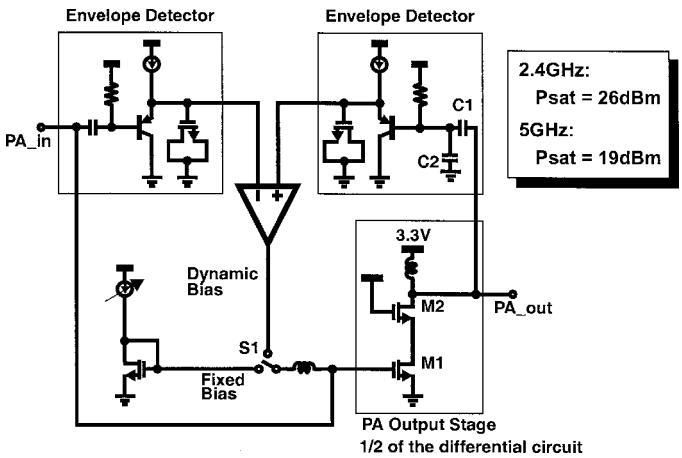

Fig. 9. Dynamically biased PA.

dissipation. In a conventional class-A amplifier, a fixed dc bias current is chosen to accommodate the largest possible signal. Its power dissipation is fixed regardless of the output signal amplitude and, hence, results in a poor power efficiency if the signal amplitude is below the maximum level. The power dissipation can be significantly reduced with a dynamically biased output stage whose dc current is proportional to the envelope of the output signal [14]. This concept is analogous to that of a class-B PA. A dynamically biased amplifier, however, dissipates very low power at small-signal levels, and the power dissipation increases only during the signal peaks. This characteristic fits nicely with the nature of an OFDM signal where the peak-to-average ratio is as large as 17 dB, but signal peaks are infrequent.

Fig. 9 shows a schematic of the integrated PA with a dynamic bias control that requires no off-chip component. The PA output stage is formed by cascoded transistors M1 and M2. Cascoding is used to allow for reliable operation from a 3.3-V supply and to ensure a stable amplifier. In this design, an error amplifier compares the envelopes at the input and output signals of the PA and produces a voltage that controls the gate drive of the output driver. The power dissipation of the PA increases only at the peaks of the output signal. The feedback loop also forces the PA to have a fixed linear gain for both large- and small-signal envelopes, thereby improving the linearity. Fig. 10 compares the plot of the EVM as a function of the output power (by varying the PA input) for a class-A output stage and a dynamically biased output stage. In each case, the EVM gets worse as the output power increases, mainly due to the increased nonlinearity. At around 10 dBm, the curves intersect and the two PAs achieve the same EVM of -28 dB, but the class-A PA dissipates

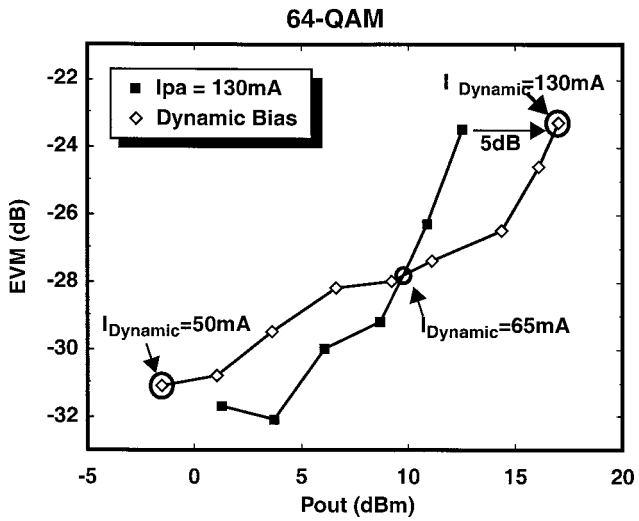

Fig. 10. Comparison of fixed bias and dynamic bias for a 2.4-GHz PA.

twice the power. For an EVM of -23.5 dB, the two PAs dissipate the same amount of power with a bias current of 130 mA; however, the dynamically biased PA delivers 5 dB more output power.

C. Frequency Synthesizer

The dual-band transceiver has two frequency synthesizers: a programmable synthesizer that is used in the 5-GHz band and a fixed frequency-offset synthesizer at 672 MHz which, together with the programmable synthesizer, cover the 2.4-GHz band. The frequency plan for the transceiver, shown in Fig. 2, requires LO_1 to be tunable from 3.2 to 4 GHz for an RF signal frequency of 4.8–6 GHz in the 802.11a mode of operation. To achieve channel spacing of 20, 10 and 5 MHz, respectively, in the 5-GHz mode, the synthesizer must operate with reference frequencies of 13.3, 6.6, and 3.33 MHz. In the 2.4-GHz mode of operation, a reference frequency of 10 MHz is used. The offset synthesizer employs an integrated *LC* VCO at twice that of the 672-MHz and uses a reference frequency of 8 MHz. All reference frequencies for both synthesizers are derived from an on-chip 40-MHz crystal oscillator.

The programmable synthesizer, a block diagram of which is shown in Fig. 11, consists of a phase-frequency detector, a charge pump with a dedicated supply regulator, an integrated programmable loop filter, and a wideband VCO, as well as a high-frequency divide-by-two circuit and an 8/8.5 dual-modulus divider in the feedback path to form a 16/17 prescaler. In addition, a digital block implements the control logic, the channel decoder, the reference divider, and the program (P) and swallow (S) counters of the feedback divider. Retiming circuits eliminate the noise introduced by the reference divider and part of the feedback divider. A lock detector provides a lock signal to the control logic. The VCO output (LO_1) and the I and Q phases generated by the high-frequency divide-by-two circuit (LO_2) drive LO buffers.

Fig. 12 shows a schematic of the charge pump. Transistors M_P and M_N are the up and down current sources, respectively. These current sources are turned on and off by switches controlled with the up and down signals. The NMOS current

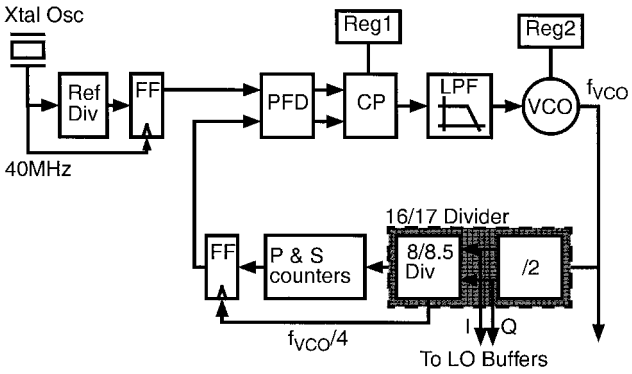

Fig. 11. Frequency synthesizer.

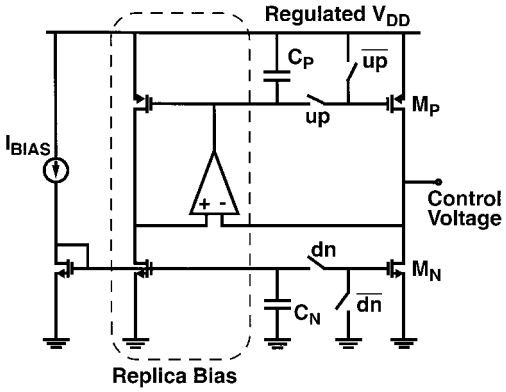

Fig. 12. Charge-pump schematic.

source bias is generated from a constant current mirror, while the PMOS device bias is generated with a replica bias circuit. The replica bias can match the up and down current sources even when transistor M_P is in triode. Capacitors C_N and C_P act as low-impedance voltage sources to reduce the switching transients and ensure fast turn on of the current sources. C_P also acts as the compensation capacitor for the replica bias amplifier. This topology is capable of providing large charge pump current, without dissipating high dc current. Very small overlap time of the up and down signals provides low charge-pump noise contribution and low spurs. A high charge-pump current allows the use of a small loop filter resistor. Such a small resistor introduces lower noise and reduces the noise contribution of the charge pump. The integrated *RC* loop filter consists of MOS capacitors and N-well resistors.

Fig. 13 shows a simplified schematic of the VCO. It consists of stacked cross-coupled pairs of NMOS and PMOS devices. The tank inductor is a single-turn inductor with a patterned ground shield [18]. The varactor is implemented with p+ in n-well diodes. To cover the required tuning range while maintaining a low VCO gain, the VCO includes a binary array of switchable capacitors with 7-b control. Each switchable capacitor unit is implemented with metal–insulator–metal (MIM) capacitors and NMOS transistors. The bypass capacitor C1 from the output of the current source to ground provides high-frequency supply noise rejection. A low VCO gain is chosen to improve the VCO phase noise and reduce the noise contribution of the loop filter resistor.

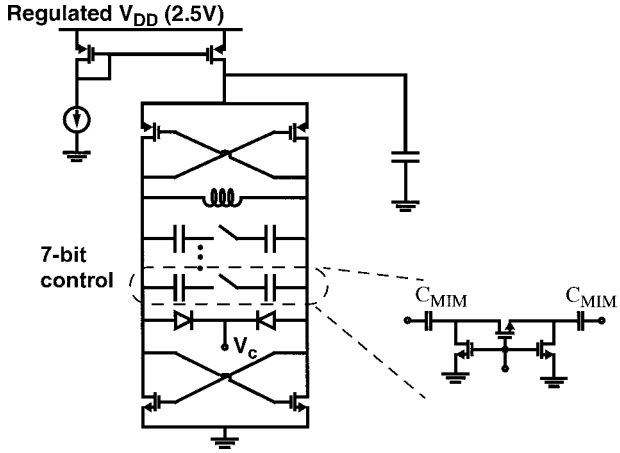

Fig. 13. VCO schematic.

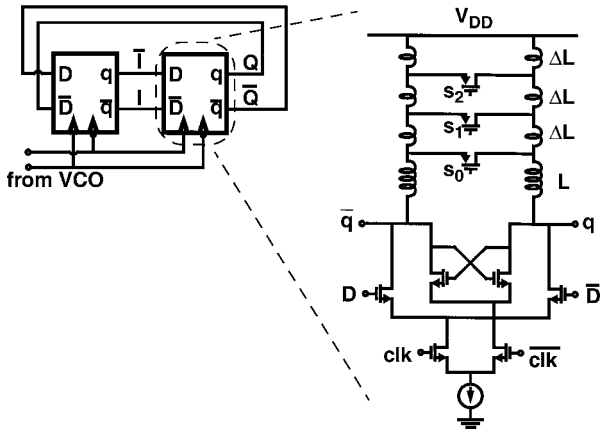

Fig. 14. High-frequency divide-by-two circuit with switchable inductors.

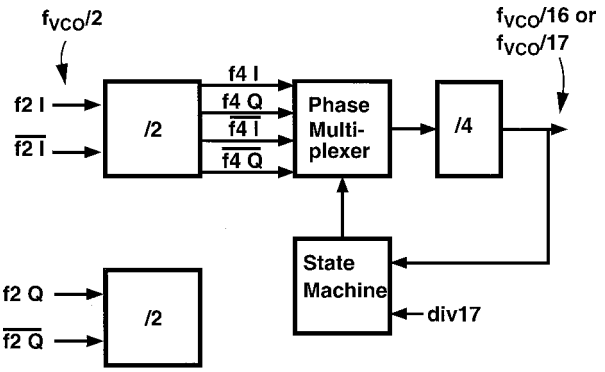

Fig. 15. The 8/8.5 dual-modulus divider.

The high-frequency divide-by-two circuit, illustrated in Fig. 14, consists of two inductively loaded current-mode flip-flops in a feedback loop clocked by the VCO output. Inductive loads are used to tune out the relatively large capacitive load associated with the feedback divider, the I and Q buffers, and wiring capacitance. Inductively loaded flip-flops in a divider configuration are topologically identical to a quadrature oscillator and behave as an injection-locked frequency divider [19]. The locking range of the injection-locked divider is increased using switchable inductors. The control signals for the PMOS switches are derived from the two MSBs of the

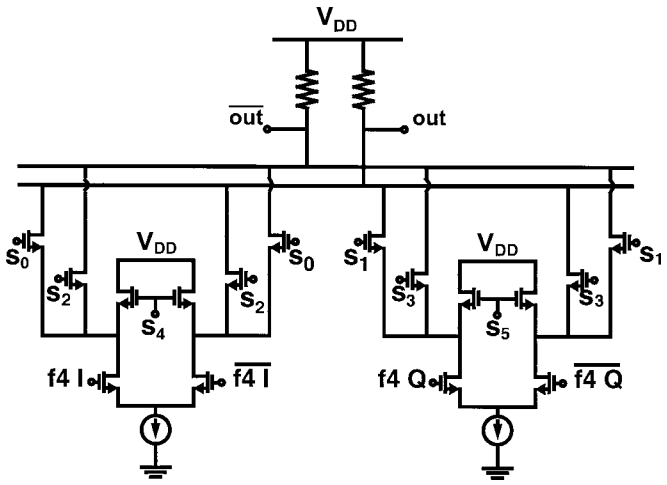

Fig. 16. Phase multiplexer used in the 8/8.5 dual-modulus divider.

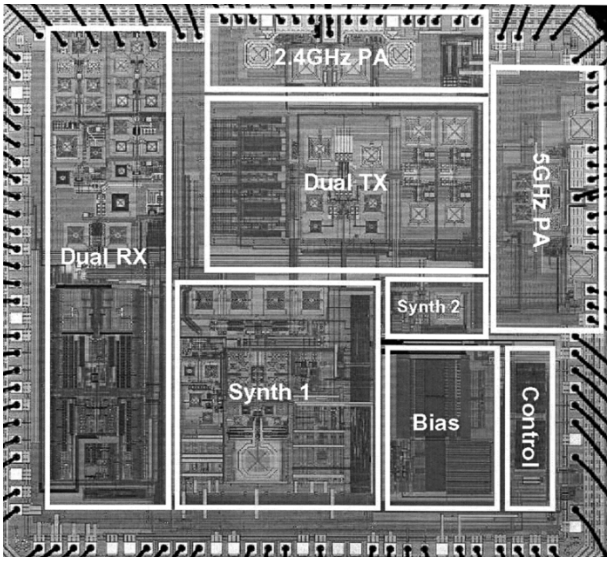

Fig. 17. Chip microphotograph.

VCO tuning control bits. Unlike switched capacitors, the use of switchable inductors provides a relatively constant output load impedance across the wide frequency range because the inductance increase at low frequency compensates for the lower ω and lower Q.

The output of the high frequency divide-by-two circuit is further divided by two in order to generate four phases at one fourth of the VCO frequency. These four phases are then fed to a phase multiplexer, which is followed by a divide-by-four circuit, as shown in Fig. 15. Division of the VCO frequency by 16 is achieved by using only one of the four phases at the multiplexer input, while division by 17 is achieved by continuously rotating among them at every output cycle. The algorithm employed by this prescaler is similar to that in [20]. A schematic of the phase multiplexer is shown in Fig. 16. The I and Q phases at one fourth of the VCO frequency are connected to the gates of two differential pairs. By controlling the gates of the cascoding devices with appropriate select signals, each phase can be connected to the output load, directly or with inverted polarity, or it can bypass the load by redirecting the current to V_{dd}. Because of the compact implementation of this phase rotator, low power consumption and good matching between the phases is achieved.

TABLE I
PERFORMANCE SUMMARY

Technology	0.25μm CMOS, 1P5M
Transmitter Power Dissipation 2.4 GHz 5 GHz	 741 mW @ Pout = 5 dBm 710 mW @ Pout = 5 dBm
Receiver Power Dissipation 2.4 GHz 5 GHz	 370 mW 320 mW
TX EVM 2.4 GHz 5 GHz	 -32 @ Pout = 5 dBm -30 @ Pout = 5 dBm
RX Noise Figure 2.4 GHz 5 GHz	 4.5 dB 5.5 dB
Phase Noise @ 100 kHz offset 2.4 GHz 5 GHz	 -109 dBc/Hz -107 dBc/Hz

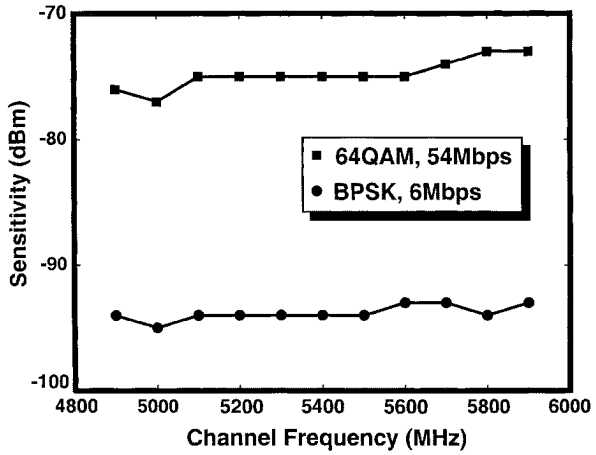

Fig. 18. Receiver sensitivity.

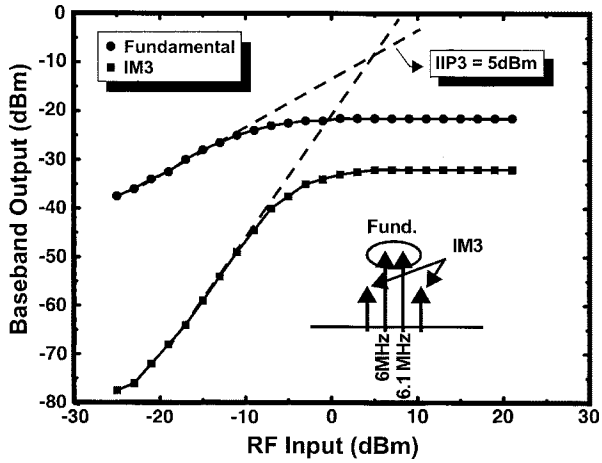

Fig. 19. Receiver intermodulation test.

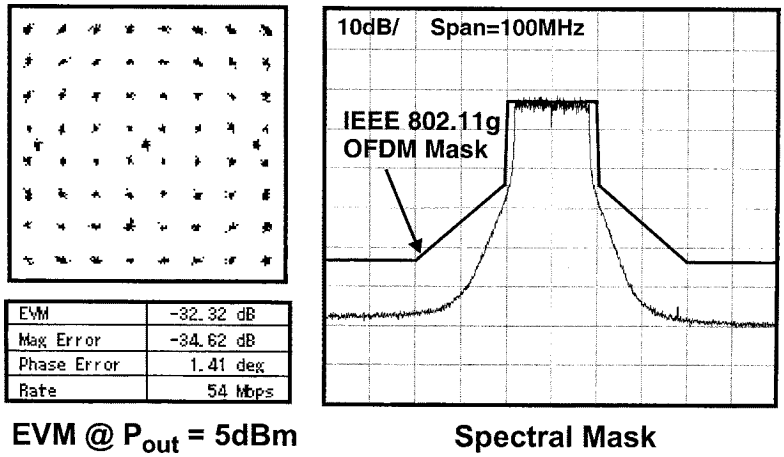

Fig. 20. Output spectrum and EVM of the 2.4-GHz transmitter.

The entire process from power up to complete settling is faster than 150 μs. During this time, the binary search for the 7 bits that control the VCO tuning capacitor array is performed, and the control voltage value is optimized. Control voltage optimization is achieved by readjusting the VCO capacitors and resettling several times until optimal VCO gain is achieved. Without this optimization step, the settling time can be well below 100 μs.

IV. Experimental Results

The dual-band radio chip was integrated in a 0.25-μm five-layer metal CMOS process, occupies a total silicon area of 23 mm^2, and is packaged in a 64-pin plastic leadless chip carrier with an exposed backside contact. A die microphotograph of the chip is shown in Fig. 17. The performance of the dual-band transceiver is summarized in Table I.

Fig. 18 shows the sensitivity of the receiver, with no external LNA, RF switches, or filters, in the 5-GHz mode when the radio is combined with the companion baseband chip. A sensitivity level of -76 dBm is measured for the 54-Mb/s mode and -94 dBm for the 6-Mb/s QPSK mode of operation. The sensitivity remains fairly flat over different channel frequencies. The linearity of the receiver chain was measured with a two-tone test, with tones centered at 6 and 6.1 MHz away from the channel center frequency. Fig. 19 shows the resulting third-order intermodulation product (IP3) as a function of the RF input level for the 5-GHz mode of operation at the minimum gain setting. The input-referred IP3 is measured to be approximately 5 dBm.

Fig. 20 shows the measured characteristics of the 2.4-GHz transmitter. The transmit constellation for a 64-QAM signal has a measured EVM of better than -32 dB at 5-dBm output power. The corresponding OFDM spectrum fits well within the IEEE 802.11g mask.

Fig. 21 shows the single-carrier-transmitter output spectrum at 5.44 GHz. At this RF frequency, the synthesizer uses a reference frequency of 13.33 MHz. The measured spurs at the crystal oscillator frequency of 40 MHz are below -70 dBc, and the reference spurs are below -75 dBc. For this channel, the value of the S counter is zero, which means that the prescaler does not perform phase rotation. Fig. 22 shows the single carrier spectrum at 5.3 GHz with the same reference frequency of 13.3 MHz. At this frequency, the S counter value is 9 and the

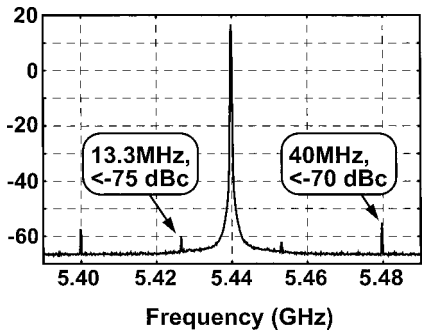

Fig. 21. Transmitter output at 5.44 GHz (S counter = 0).

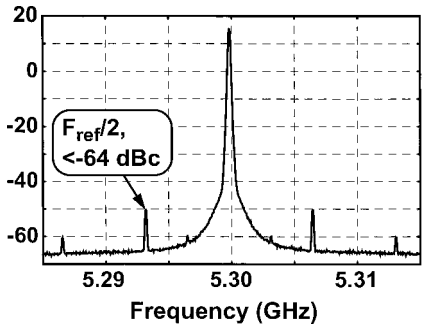

Fig. 22. Transmitter output at 5.44 GHz (S counter = 9).

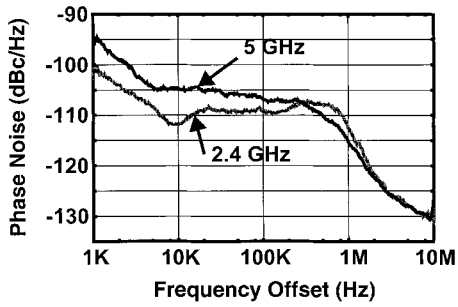

Fig. 23. Phase noise at the transmitter output.

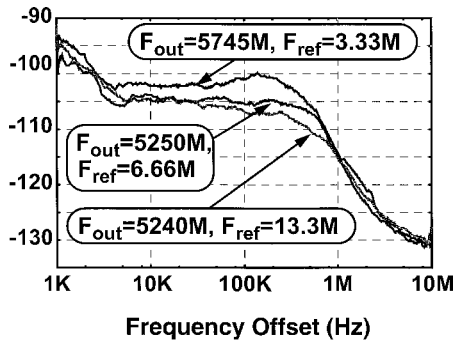

Fig. 24. Phase noise at the 5-GHz transmitter output for different operating conditions.

prescaler does perform phase rotation. Mismatches among the rotated phases give rise to fractional reference spurs. In this case, the fractional spurs are at half the reference frequency. Across the channels, these fractional spurs remain below −64 dBc.

The phase noise profile measured at the output of the 5-GHz transmitter with a reference frequency of 13.3 MHz is shown in Fig. 23. The spot phase noise is −105, −107, and −115 dBc/Hz at 10-kHz, 100-kHz and 1-MHz frequency offset, respectively. The integrated phase noise from 1 kHz to 10 MHz is −45.1 dBc or 0.31°. The phase-noise profile at the output of the 2.4-GHz transmitter, also shown in Fig. 23, is about 5 dB lower across most of the frequencies. By reducing the programmable loop bandwidth, we can measure the VCO phase noise at a frequency offset significantly larger than the loop bandwidth. With reduced loop bandwidth, the spot phase noise at the output of the 5-GHz transmitter, at 1-MHz offset from the 5.44-GHz carrier, is −121 dBc/Hz. Because the VCO runs at 2/3 of the RF frequency, this measurement translates to a phase noise of −124.5 dBc/Hz for the VCO running at 3.626 GHz. Fig. 24 shows phase-noise profiles under different operating conditions of the transceiver, namely channel spacing of 20 and 10 MHz in the low 5-GHz band and 5 MHz in the upper 5-GHz band.

The radio chip has been integrated along with the companion baseband chip into an IEEE 802.11a/b/g wireless LAN system. The performance of this WLAN system in an open office environment was measured according to the procedures described in [21]. A dramatic improvement in both range and throughput was observed compared to the first-generation WLAN chip set published in [1]. The range and throughput of this design in the IEEE 802.11a/b/g modes are illustrated in Fig. 25. The data indicate no significant performance difference between the 2.4- and 5-GHz modes within the office at ranges up to 200 ft.

V. Conclusion

A dual-band tri-mode radio transceiver meeting the IEEE 802.11a/b/g standards has been integrated in a 0.25-μm CMOS technology. The transceiver has dedicated RF front-ends for the 2.4- and 5-GHz bands but shares the IF and baseband circuits to minimize die area. The use of dual conversion with a high sliding IF requires only one synthesizer for the 5-GHz path, while a fixed frequency offset synthesizer is needed for the 2.4-GHz path. The transceiver is fully integrated including the synthesizer loop filters and baseband filters. The receive

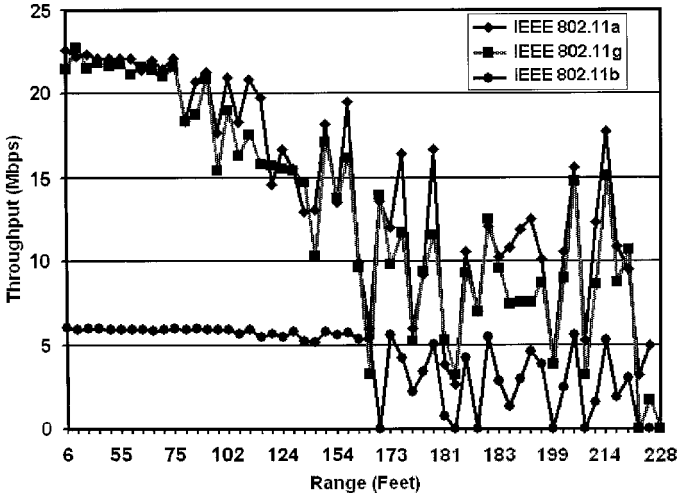

Fig. 25. Throughput/range of present design in IEEE 802.11a/b/g modes.

chain has a composite noise figure of 5.5/4.5 dB at 5/2.4 GHz. The transmitter delivers 9 dBm/8 dBm EVM-compliant output power for a 64-QAM OFDM signal. The synthesizer phase noise at the 5-GHz RF output is −105 dBc/Hz at 10-kHz offset, and all spurs are below −64 dBc.

Acknowledgment

The design and implementation of a wireless LAN system requires many resources, far beyond the analog and RF circuit designs described in this paper. The authors wish to acknowledge the contributions of the entire wireless team at Atheros Communications, including, but not limited to, the digital, algorithms, protocols, software, and system engineering teams. Special thanks are due to H. Dieh and J. Lu and S. Auyeung.

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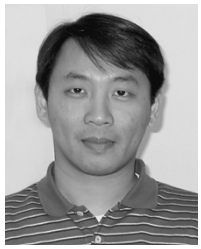

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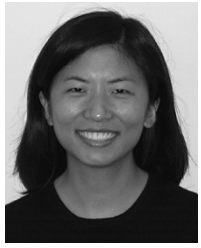

MeeLan Lee received the B.S. and M.Eng. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, in 1995 and 1997, respectively.

From 1997 to 1999, she was with Chromatic Research, Sunnyvale, CA, working on media processors. From 1999 to 2001, she worked was with Level One Communications, San Francisco, CA, designing cordless telephone chipsets. She is currently with Atheros Communications, Sunnyvale, CA.

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From 1991 to 1996, he was with Micro Linear Corporation, San Jose, CA, where he worked on motion control, high-speed logic, and wired ethernet products. From 1996 to 2001, he was with Level One Communications, which was acquired by Intel Corporation. At Intel, he worked on the first fully integrated CMOS radios, for which he designed switched-capacitor filters and other analog circuits. In addition, he performed system calculations for future RF CMOS products. In July of 2001, he joined Atheros Communications, Sunnyvale, CA, where he has primarily focused on data converters, frequency synthesizers, and mixed-signal circuits for wireless communication products.

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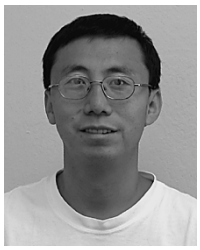
Mr. Samavati received a departmental Fellowship from Stanford University in 1995 and a Fellowship from IBM Corporation in 1998. He was the recipient of the ISSCC Jack Kilby Outstanding Student Paper Award for the paper "Fractal Capacitors" in 1998.



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