A Single-Chip Fingerprint Sensor and Identifier

Satoshi Shigematsu, *Member, IEEE*, Hiroki Morimura, *Member, IEEE*,
Yasuyuki Tanabe, Takuya Adachi, and Katsuyuki Machida

Abstract— A chip architecture that integrates a fingerprint sensor and an identifier in a single chip is proposed. The fingerprint identifier is formed by an array of pixels, and each pixel contains a sensing element and a processing element. The sensing element senses capacitances formed by a finger surface to capture a fingerprint image. An identification is performed by the pixel-parallel processing of the pixels. The sensing element is built above the processing element in each pixel. The chip architecture realizes a wide-area sensor without a large increase of chip size and ensures high sensor sensitivity while maintaining a high image density. The sensing element is covered with a hard film to prevent physical and chemical degradation and surrounded by a ground wall to shield it. The wall is also exposed on the chip surface to protect against damage by electrostatic discharges from the finger contacting the chip. A 15×15 mm^2 single-chip fingerprint sensor/identifier LSI was fabricated using 0.5-μm standard CMOS with the sensor process. The sensor area is 10.1×13.5 mm^2. The sensing and identification time is 102 ms with power consumption of 8.8 mW at 3.3 V. Five hundred tests confirmed a stranger-rejection rate of the chip of more than 99% and a user-rejection rate of less than 1%.

Index Terms— Biometrics sensors, fingerprint identification, fingerprint sensor, image processing, pixel-parallel processing, smart pixel.

I. INTRODUCTION

PORTABLE and mobile types of equipment, like IC cards, notebook computers, and cellular phones, are becoming increasingly popular. Consequently, user authentication to prevent unauthorized use of such equipment has become an important issue. For consumer products, the authentication process should be simple and reliable. Methods of user authentication include the use of passwords, personal identification numbers (PIN's), and verification using the iris in the human eye. One of the simplest and most reliable authentication methods is the fingerprint. For use in portable and mobile equipment, the fingerprint identification unit should be compact and inexpensive and must guarantee security of the user's data and privacy.

A fingerprint identification unit is composed of a fingerprint sensor, a fingerprint identification device, and a memory that stores a template of the user's fingerprint. The conventional optical fingerprint sensor generally consists of a prism, a charge-coupled-device sensor for photo detection, and a light-emitting diode as a light source. Fingerprint identification

requires extensive image processing, performed by a high-performance microprocessor, and a large memory. The template is also stored in this memory. The size and cost of the components make such a unit unsuitable for application to portable equipment.

Recently, some small, thin, and inexpensive direct-touch semiconductor fingerprint sensors have been proposed [1]–[4], [15], [16]. These devices sense the capacitance formed by the finger when it makes direct contact with the chip. However, for fingerprint identification, they require several support chips, i.e., a high-performance microprocessor and large memory. This makes the identification unit large and expensive. Moreover, the personal data in these chips can be tampered with easily because the chips are separated in the system and the data must be sent from chip to chip for identification. Thus, embedding such a fingerprint identification unit into mobile and portable equipment is difficult.

We propose a new chip architecture that integrates the sensor and identifier in a single chip, which is the most effective way to solve the above-mentioned problems. One of the key concepts of the architecture is an identifying pixel in which the fingerprint sensing element and the processing element are vertically integrated. The sensing element senses the capacitance formed by a finger surface and a metal plate within the sensor. The identification is accomplished by parallel processing of identifying pixels. A new sensor structure with electrical, physical, and chemical tolerance is also proposed. A single-chip fingerprint sensor/identifier LSI is presented for the first time.

In this paper, we describe the chip architecture and the fingerprint identification process in Section II. The concept of the identifying pixel is described in Section III, and the structure of the sensing element is explained in Section IV. The implementation of the chip and the experimental results are presented in Sections V and VI.

II. FINGERPRINT SENSOR/IDENTIFIER CHIP

A. Requirements for Fingerprint Chip Architecture

Recently, some architectures for the integration of the sensor and processing unit in a single chip have been reported [7]–[13]. These architectures are proposed for a photo-image sensing chip. Fig. 1 shows the conventional photo-image-sensing chip architecture. In the architecture for a sensor-embedded chip, the sensor and processing unit are integrated on a single chip by placing them side by side, as shown in Fig. 1(a). The photo sensor does not require a large area, but a rather large number of pixels are needed for capturing a
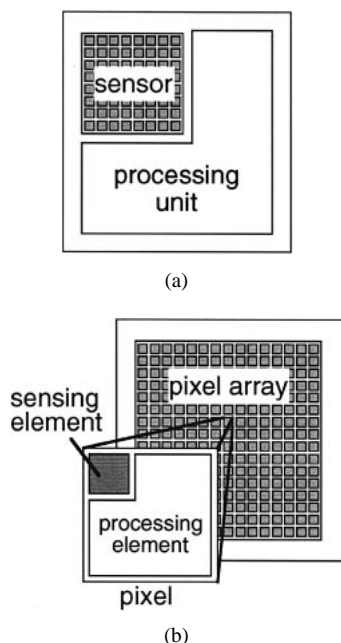
(a)

(b)

Fig. 1. Conventional architectures for integration of sensor and processing unit in single chip. (a) Sensor embedded chip and (b) sensor-embedded-pixel array.

TABLE I
CHARACTERISTICS OF CONVENTIONAL ARCHITECTURES FOR FINGERPRINT SENSING

	sensor emb. chip	sensor-emb.- pixel array	requirement for fingerprint
Sensor area	small	**large**	**large**
Sensing element (sensitivity) *	**large (high)**	small (low)	**large (high)**
Image density	**high**	low	**high**
Chip size	large	**small**	**small**

* sensitivity for sensing capacitance.

Fig. 2. Fingerprint sensor and identifier chip architecture.

high-resolution image. On the other hand, the sensing area of a direct-touch fingerprint sensor should be as large as the finger (over 10×10 mm^2) because the sensor senses the fingerprint of a finger in contact with the chip. Recently, a small-area slim fingerprint sensor was proposed [4]. It senses fractional images of a fingerprint as the finger is slid across it. After the sensing, a full fingerprint image is synthesized from these sensed images. If this architecture were used to design a single-chip fingerprint sensor and identifier, the chip area would increase even though a sensor is small, because this sensor requires a high-performance processor and large memory to make a full image and store a large number of fractional images.

The architecture for the sensor-embedded-pixel array employs a pixel array; a sensing element and processing element are placed side by side in each pixel, as shown in Fig 1(b). In this architecture, the array of pixels forms the sensor and processing unit. Image processing is carried out by parallel processing of the processing elements. The photo sensor does not require a very large area for the sensing element to enhance sensitivity, and so the sensing element occupies only a part of the pixel. In contrast, a direct-touch fingerprint sensor requires a large sensing element, for example over 30×30 μm^2, because the sensor senses the capacitance of the finger on the sensing element, and its sensitivity depends on the size of the detection plate within the sensing element. If this architecture were used for fingerprint sensing, each pixel would have to be increased in area so that the sensing element in the pixel could be enlarged, and this would cause a reduction in the density of the sensed image.

If these architectures were employed to provide a single-chip fingerprint sensor and identifier, the characteristics would be as summarized in Table I. The fingerprint chip architecture requires not only a large-area sensor in a small chip but also

an expanded sensing element with higher image density. The sensor-embedded chip can provide a large sensing element and high sensitivity. It can also enhance the density of the sensed fingerprint image. However, expanding the sensor area would increase the chip size. The sensor-embedded-pixel array can achieve both large sensor area and small chip size, but enhancing the sensitivity by expanding the sensing element would reduce the image density. Therefore, these conventional architectures are inappropriate for incorporating a fingerprint sensor and identifier in a single chip.

B. Fingerprint Chip Architecture

The present fingerprint sensor/identifier chip architecture is proposed to satisfy all requirements for the integration of the fingerprint sensor and identifier in a single chip. Fig. 2 is a block diagram of the chip architecture. The innovative features of the proposed architecture are that a fingerprint is sensed and identified by the array of pixels and the sensor is stacked above the identifier to integrate them in each pixel.

The chip is composed of an identifying array and a small embedded controller. The array consists of pixels, each of which has a sensor and a processing element and handles one pixel of fingerprint image data. The identifier is based on a pixel-parallel structure and identifies a fingerprint by image processing of the pixels. Stacking the sensor above the processing element in each pixel offers a large sensing element while maintaining higher image density. The pixel-parallel structure of the identifier provides a large sensor area

in a small chip. Thus, the proposed chip architecture satisfies all of requirements for the fingerprint chip architecture.

In the architecture, the pixel size would depend on the size of the processing element. For a high-density sensor, the processing element has to be small, and its function also has to be limited. In order to provide an identifier using such pixels, the architecture employs an optimized fingerprint-identification algorithm, which uses the combination of simple image processings to identify a fingerprint. On the other hand, stacking the sensor element above circuits increases the influence of parasitic capacitance. In the proposed architecture, the sensing circuit is designed to suppress the influence of parasitic capacitance.

In this chip architecture, the user's template fingerprint data are stored in the chip, and sensing and identification are completely performed without any other chips. The only data output from the chip is the identification result; there is no transmission of user fingerprint data between the chip and external devices. Therefore, the user template cannot be replaced with a different one, and the user's fingerprint image cannot be stolen. Moreover, high-speed and low-power fingerprint identification can be achieved.

C. Fingerprint Identification

In the proposed architecture, the fingerprint is identified by the parallel processing of the pixels. To enhance the density of the sensor, the size of the processing circuit has to be limited, and an algorithm suitable for such processing circuit is required. In our pixel array, we adopt the fingerprint verification method based on thinned-image pattern matching [5]. This algorithm employs a large number of simple image processings, such as image pattern matching, for a fingerprint identification, so it is quite suitable for the array of the pixels, which can handle simple image processing at high speed and low power.

In this algorithm, a user's original fingerprint image is thinned down to make a user's template. For the identification, the sensed fingerprint is binarized to a black-and-white image. The identification is carried out on the basis of image pattern matching between the thinned template and the binarized fingerprint images. If the maximum matching ratio of the two images were higher than a threshold, identification would be achieved and the fingerprint authenticated. Using a thinned image as a template allows for fluctuation and rotation (up to 10°) of the fingerprint image.

Fig. 3 shows the process for fingerprint registration and identification. For registration, the sensor produces an image of the user's fingerprint, and the image is sent to an external PC. The PC thins the lines in the image down to a width of 1 pixel and writes this thinned image to the memory of the identifier as the user template. Then, the interface circuit, which communicates with the external PC, is shut off by breaking it. The identifier cannot make a template by itself, and cannot input and output fingerprint images. This prevents illicit registration of a different template and theft of the user's template and sensed image. After registration, the chip alone senses and identifies the fingerprint. For identification, the
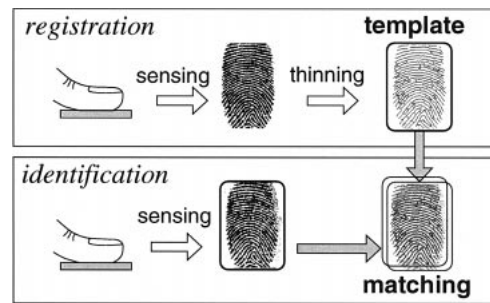

Fig. 3.   Process for registration and identification.

sensor again produces an image of the user's fingerprint when the finger makes contact with the chip. The identifier compares that image with the template using pixel-parallel processing, and produces an index indicating the closeness of the match. If the index is above a threshold, a positive result is output, meaning that the fingerprint is authenticated.

The details of how the chip carries out the fingerprint identification algorithm are as follows. First, the sensing circuit in each pixel senses the shape of the fingerprint and binarizes it into a 1-bit datum for digital processing. Then, the processing circuit in the pixel compares the binarized datum with user template datum. The embedded controller collects the results of the comparison from all pixels and evaluates the matching ratio, which indicates how many pixels are consistent. In practical use, it cannot be guaranteed that the finger is put at the same position on the sensor every time. So the pixel array, using communication among neighboring pixels, shifts the sensed image in order to allow for deviation of the finger location. The sensed image is shifted in all of the defined directions (i.e., horizontal and vertical axis from -20 to 20 pixels) and compared with the template at each shifting to produce the maximum matching ratio. Finally, according to the maximum matching ratio, the controller outputs the identification results to the external devices.

III. IDENTIFYING PIXEL

For the fingerprint identification, the array of identifying pixels employs pixel-parallel image processing. For such processing, each processing element in the identifying pixels has to perform image processing on a 1-pixel datum of a fingerprint image in parallel. Hence, an identifying pixel must:

- store the 1-pixel datum of the fingerprint image as a user template;
- sense the shape of a fingerprint and produce the fingerprint image;
- binarize the sensed image into a 1-bit datum for digital processing;
- shift the image to allow variations in finger position;
- compare the sensed datum with the template datum and transmit the result to the controller.

The identifying pixel is devised to handle all these functions while maintaining small pixel size. It consists of a sensor plate, a sensing circuit, a 1-bit memory, and a processing circuit, as shown in the block diagram in Fig. 4.
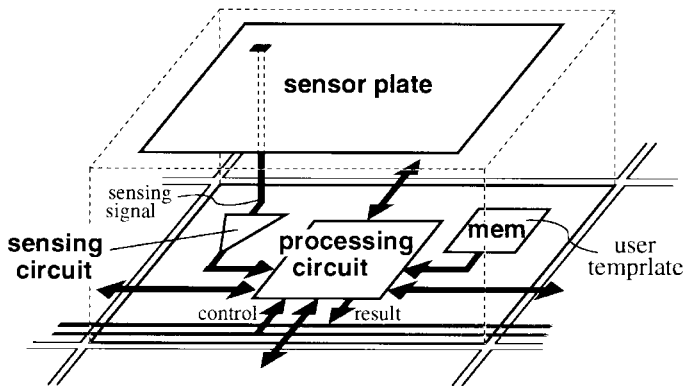
Fig. 4. Basic concept of the pixel.

Fig. 5. Circuit diagram of the pixel.

Fig. 6. Cross section of the pixel.

The memory stores a 1-pixel datum of the user template fingerprint image made by the external PC at registration. The sensor plate is the fingerprint sensing element and is built above the processing element in each pixel. Stacking the sensor plate above logic circuits achieves the vertical integration of the sensing element and processing element in the pixel while providing a larger sensing element and a higher image density. The sensing circuit is connected to the sensor plate and detects the fingerprint on the plate. In order to suppress the influence of the parasitic capacitance, the differential charge-transfer-amplifier technique [14] is applied to the sensing circuit. When the finger touches the chip, capacitance is formed between the surface of the finger and the sensor plate. It depends on the distance between the finger and the plate, and its value reflects the shape of the fingerprint. Then, the sensing circuit converts the sensed value into a 1-bit digital signal indicating whether the sensed point is a ridge or a valley and outputs it.

The processing circuit performs image processing according to the control signals from the controller. It is connected to the sensing circuit and the memory and gets data from them to compare a sensed image datum produced with the template image datum stored in the memory. The comparison result is sent to the controller for the evaluation of the matching ratio. The processing circuit is also connected to neighboring pixels to communicate the pixel datum. Communication among neighboring pixels enables shifting of a fingerprint image.

Fig. 5 shows the circuit diagram of an identifying pixel. It consists of a sensing circuit, a memory circuit, and a processing circuit containing a selector, register, and comparator.

In the processing circuit, the selector inputs the signals from the sensing circuit and the neighboring pixels. It selects these input signals according to the control signal from the controller and outputs the selected signal to the register. The register stores the signal from the selector with the control signal and outputs the stored data to the comparator and the neighboring pixels. If all of the pixels transfer the stored data to neighboring pixels in the same direction, the stored fingerprint image can be shifted. This direction depends on the signal selection of the selector. The comparator compares the sensed and shifted image datum with the template datum stored in the memory and sends the result of the comparison to the controller.
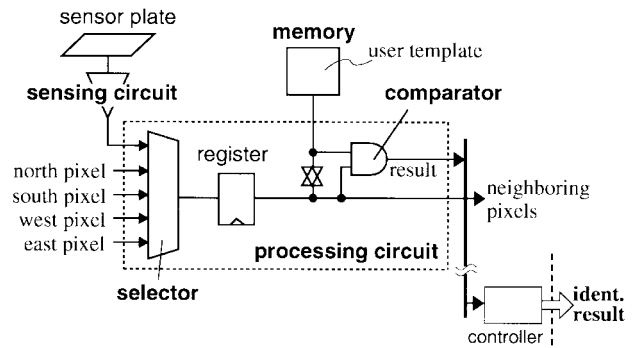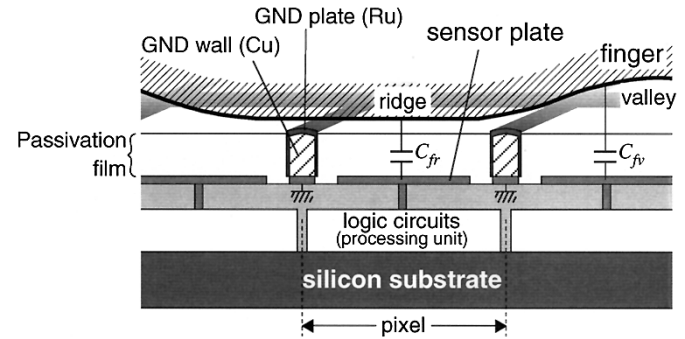
The memory circuit stores the pixel datum of the user template fingerprint, and it is connected to the comparator. It is also connected to the register through a switch circuit. One of the pixels in the array is connected to the controller. At registration, the controller sends the template datum to this pixel, and then that datum is transferred pixel by pixel to neighboring pixels using the image-shift operation. As a result, the user template data are spread over the registers of all pixels. When the switch circuit turns on, the register writes the transferred template datum into the memory circuit. As described above, the identifying pixel can perform all of the functions required for fingerprint-identification processing. The array of identifying pixels enables pixel-parallel processing for fingerprint identification and achieves a large-area sensor in a small chip and high-speed, low-power operation.

IV. SENSOR STRUCTURE

In a solid-state fingerprint sensor, a user touches the chip die directly, and the sensing elements detect a small capacitance. In the identifying-pixel architecture, the sensing element is built above the logic circuits. With this arrangement, the sensor and logic circuits are susceptible to several kinds of damage. Electrostatic discharge (ESD) could destroy circuits, and the noise caused by a coupling capacitance between sensors could corrupt the fingerprint image. To solve these problems, the new sensor structure is proposed.

Fig. 6 is a cross section of an identifying pixel. The sensor plate is situated above some logic circuits, which are composed of the sensing, memory, and processing circuits. When a finger comes in contact with the chip, the capacitance between the
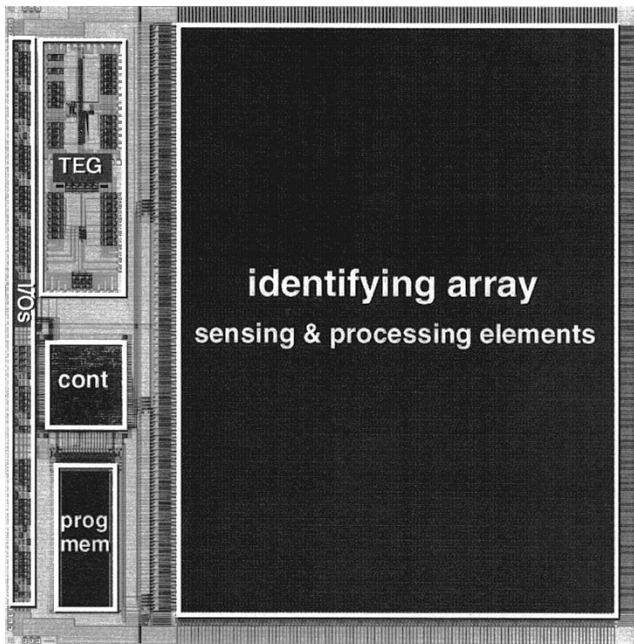
Fig. 7.   Chip micrograph.

Fig. 8.   Layout pattern of the pixel.

Fig. 9.   SEM micrographs of the chip: (a) pixel array and (b) cross section of the pixel.

plate and the finger is either C_{fr} for a ridge or C_{fv} for a valley. These capacitances are detected and binarized by the sensing circuits directly under the plate.

Each sensor plate is surrounded with a lattice-like wall. This wall is also exposed on the chip surface and connected to ground. It discharges the charge on the finger to protect the circuits from electrostatic discharge and to eliminate fluctuations in the detection voltage. The wall is made of copper and encapsulated by ruthenium. Ruthenium, which is well known as a contact material and whose oxide is conductive [6], is used as a protective material to prevent the oxidation of the copper. The wall also shields the sensor from neighboring sensors. This reduces the noise caused by the coupling capacitance and improves the signal-to-noise ratio of sensing.

To protect the surface of the chip and the logic circuits from physical and chemical damage, the sensor is covered with a hard passivation film, which is a kind of a polyimide. This film has the lower moisture adsorption characteristics than a conventional polyimide film. This structure solves the above-mentioned problems and provides robust identifying pixels.

V. IMPLEMENTATION

To check the effectiveness of the proposed architecture, a test chip was fabricated using a standard 0.5-μm CMOS three-metal process in combination with the sensor process. Fig. 7 is a micrograph of the chip. The die size is 15 by 15 mm^2, and the sensor region is 10.1 by 13.5 mm^2. The array size is 124 $\times$ 166 pixels, and there are 20 584 identifying pixels in the array. Each pixel is 81.6 μm square and contains 158 MOSFET's. The sensor plate is built above these transistors and is 63.2 μm square. The density of a fingerprint image is 311 dpi. The chip also has a 6.5-Kgate embedded controller and a 16-Kbit program memory. This memory stores only the program for the controller.
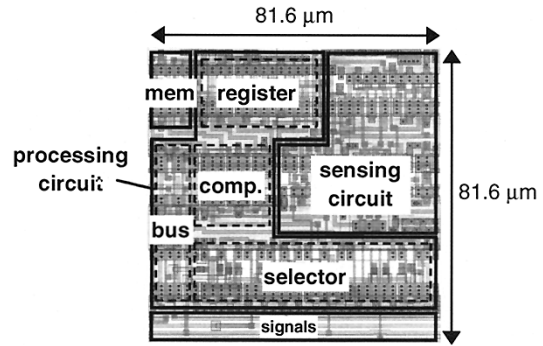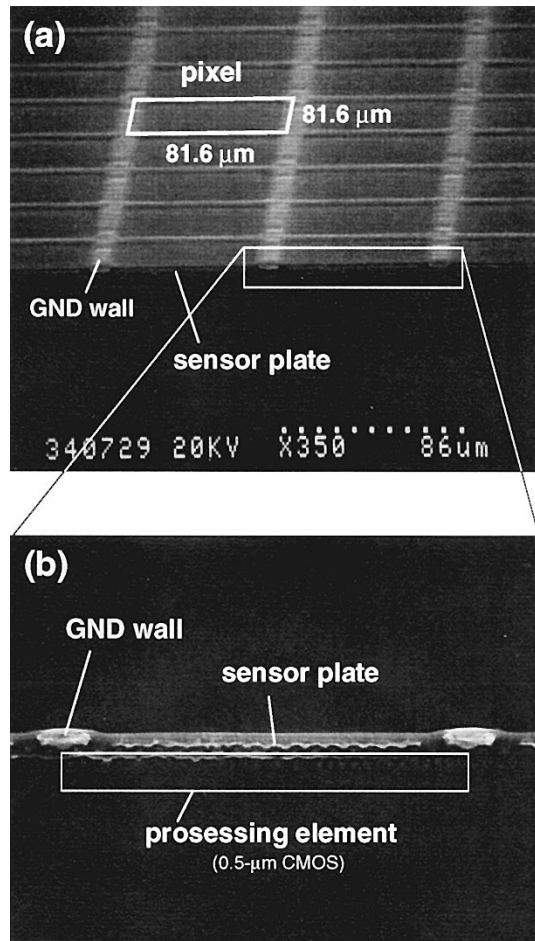
Fig. 8 shows how the sensing circuit, the memory, and the processing circuits, which consist of the register, comparator, selector, and bus driver, are laid out in the identifying pixel. The sensor plate and ground wall are built above these circuits. In this layout, the circuit elements, such as transistors and lines, are placed uniformly in the pixel, in order to make the sensor plate flat and enhance the yield of the chip.

Fig. 9 shows scanning electron microscope (SEM) micrographs of the pixel array and an individual pixel. A top view of the identifying-pixel array is shown in Fig. 9(a). It is clear
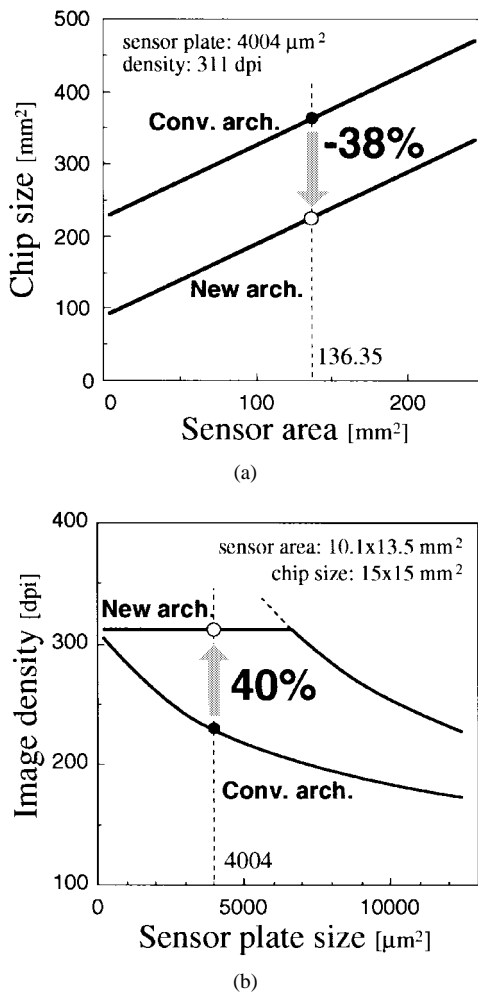
Fig. 10. Estimated effectiveness of chip architecture: (a) comparison with sensor-embedded chip architecture and (b) comparison with sensor-embedded-pixel-array architecture.

Fig. 11. Binarized fingerprint image from sensing circuits without any additional signal processing.

in this picture that each pixel is surrounded by the ground wall, and the wall is exposed on the chip surface. Fig. 9(b) is a cross-section view of an identifying pixel. One can see that the sensor plate and the ground wall are built above the logic circuit, and the sensor plate is shielded by the ground wall.

In order to confirm the effectiveness of the proposed chip architecture, the fingerprint sensor/identifier chips were designed using the sensor-embedded chip and the sensor-embedded-pixel array architecture, which are conventionally used for photo-sensing chips. Fig. 10 shows the estimated features of these chips. The sensor-embedded chip architecture has a tradeoff between chip size and sensor area. A high-density and high-sensitivity sensor can be fabricated, but the expansion of the sensor area greatly increases chip size. When the circuit for the processing unit is assumed to be the same as that in the fabricated chip, and the parameters, which are the sensor plate size, the image density, and the sensor area, are the same as those in the fabricated test chip, the fabricated chip is 38% smaller than the one with the sensor-embedded chip architecture, as shown in Fig. 10(a). The proposed architecture can expand sensor area without a large increase of chip size.

On the other hand, the sensor-embedded-pixel array architecture has a tradeoff between the sensor-plate size and image density. A large sensor area and small chip can be achieved, but the expansion of the sensor plate to enhance sensor sensitivity reduces the density of a fingerprint image. Fig. 10(b) shows the relationship between image density and sensor plate size, when the sensor plate and the sensor area are the same as those in the fabricated test chip and both chips are the same size. The density of the fabricated chip is limited to 311 dpi, because the pixel size is dominated by the size of the processing element under the plate when the sensor plate is smaller than the processing element. The image density of the fabricated chip is 40% higher than that of the chip with the sensor-embedded-pixel array. The proposed chip architecture can enhance both the image density and the sensor sensitivity.

VI. EXPERIMENTAL RESULT

Fig. 11 shows a binary fingerprint image obtained from the sensing circuits without any additional signal processing. It is confirmed that the sensor and the sensing circuit can sense and binarize the fingerprint. The sensing circuit produces a binary fingerprint image in about 2 ms. The fingerprint identification, in which the comparison and shifting of an image are repeated many times, is completed within 100 ms. The total period to sense and identify a fingerprint is 102 ms. This identification requires more than 200 million operations, so the processing performance of the pixel-parallel identifier is more than 2 GOPS. The power consumptions are 2.6 mW for sensing and binarizing and 6.2 mW for identification at a supply voltage of 3.3 V. In the measurement, both sensing and identification are performed at a rate of once a second. Therefore, the energy consumption of sensing and binarizing is 2.6 mJ, and that of identification is 6.2 mJ at 3.3 V. This is much less than the energy consumed by conventional systems consisting of a sensor, processor, and memory chips.

To determine the identification accuracy, we performed 500 tests. In the tests, a guide plate was placed on the

TABLE II
CHARACTERISTICS OF TEST CHIP

Process		0.5-μm standard CMOS, 3-metal, sensor process
Die size		15 mm x 15 mm
Identifying array	area	10.1 mm x 13.5 mm
	no. pixels	20,584 (124 x 166)
	density	311.3 dpi
	Tr. count	3252 K
Pixel	size	81.6 μm x 81.6 μm
	Tr. count	158
Time		
	sensing & binarize	2 ms / image
	identify	100 ms / image
Energy		
	sensing & binarize	2.6 mJ / image
	identify	6.2 mJ / image
Supply voltage		3.3 V

chip to help users put their finger at the same position. For each identification, five images are sensed to get fine fingerprint image. The stranger-rejection rate is more than 99%, and the user-rejection rate is less than 1%. These experimental results confirm that our new architecture is suitable for user authentication on small thin equipment. The chip characteristics are summarized in Table II.

VII. SUMMARY

A chip architecture that enables a fingerprint sensor and identifier to be integrated on a single chip has been presented. The key feature is a pixel architecture that incorporates a sensing element and a processing element by stacking them without a large increase of chip size. This enables a high-sensitivity sensing element to be fabricated above the processing element while maintaining high image density. Each pixel is surrounded by a ground wall to shield it to suppress the noise. This wall is also exposed on the chip surface and protects against damage by ESD. The sensor plate is covered with a hard film to prevent physical and chemical damage, and thus robust, low-noise operation is provided. When a proposed array of identifying pixels is fabricated, not only does the top surface constitute a sensing plate, but the circuitry below can also perform both sensing and identification functions.

A test chip was fabricated in a standard 0.5-μm CMOS process with the sensor process. The experimental results demonstrate the effectiveness of the architecture. The proposed chip architecture enables a fingerprint sensor and identifier to be integrated on a single chip, and for the first time provides a means of user authentication for portable and mobile equipment other than PIN's and passwords.

ACKNOWLEDGMENT

The authors would like to thank R. Kasai, J. Yamada, S. Konaka, H. Kyuragi, and T. Wakimoto for their support and comments.

REFERENCES

[1] N. D. Young, G. Harkin, R. M. Bunn, D. J. McCulloch, R. W. Wilks, and A. G. Knapp, "Novel fingerprint scanning arrays using polysilicon TFT's on glass and polymer substrates," *IEEE Electron Device Lett.*, vol. 18, pp. 19–20, Jan. 1997.
[2] M. Tartagni and R. Guerrieri, "A fingerprint sensor based on the feedback capacitive sensing scheme," *IEEE J. Solid-State Circuits*, vol. 33, pp. 133–142, Jan. 1998.
[3] C. Inglis, L. Manchanda, R. Comizzoll, A. Dickinson, E. Martin, S. Mandis, P. Silveman, G. Weber, B. Ackland, and L. O'Gorman, "A robust, 1.8 V 250 μW direct-contact 500 dpi fingerprint sensor," in *ISSCC Dig. Tech. Papers*, Feb. 1998, pp. 284–285.
[4] J. Lee, D. Min, J. Kim, and W. Kim, "A 600-dpi capacitive fingerprint sensor chip and image-synthesis technique," *IEEE J. Solid-State Circuits*, vol. 34, pp. 469–475, Apr. 1999.
[5] T. Kobayashi, "A fingerprint image recognition method for network user identification," in *Proc. 4th Int. Conf. Computing and Information*, 1992, pp. 341–344.
[6] M. Yaita, A. Hirata, K. Machida, H. Ishii, K. Saito, N. Kawamura, and N. Awaya, "Ru encapsulation over Cu interconnections by the use of selective electroless plating," in *Proc. Advanced Metallization Conf. 1998 Japan/Asia Session*, 1998, pp. 65–66.
[7] B. Ackland and A. Dickinson, "Camera on a chip," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf.*, 1996, pp. 22–25, TA 1.2.
[8] S. Kawahito, M. Yoshida, M. Sasaki, K. Umehara, D. Miyazaki, Y. Tadokoro, K. Murata, S. Doushou, and A. Matsuzawa, "A CMOS image sensor with analog two-dimensional DCT-based compression circuits for one-chip cameras," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2030–2041, Dec. 1997.
[9] M. Loinaz, K. Singh, A. Blanksby, D. Inglis, K. Azadet, and B. Ackland, "A 200-mW, 3.3-V, CMOS color camera IC producing 352 × 288 24-b video at 30 frames/s," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2092–2103, Dec. 1998.
[10] S. G. Smith, J. E. D. Hurwitz, M. J. Torrie, D. J. Baxtr, A. A. Murray, P. Likoudis, A. J. Holmes, M. J. Panaghiston, R. K. Henderson, S. Anderson, P. B. Denyer, and D. Renshaw, "A single-chip CMOS 306 × 244-pixel NTSC video camera and a descendant coprocessor device," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2104–2111, Dec. 1998.
[11] R. Dominguez-Castro, S. Espejo, A. Rodrigues-Vazquez, R. A. Carmona, P. Foldesy, A. Zarandy, P. Szolgay, T. Sziranyi, and T. Roska, "A 0.8-μm CMOS two-dimensional programmable mixed-signal focal-plane array processor with on-chip binary imaging and instructions storage," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1013–1026, July 1997.
[12] Y. Ni, F. Devos, M. Boujrad, and J. H. Guan, "Histogram-equalization-based adaptive image sensor for real-time vision," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2027–1036, July 1997.
[13] H. C. Jiang and C. Wu, "A 2-D velocity- and direction-selective sensor with BJT-based silicon retina and temporal zero-crossing detector," *IEEE J. Solid-State Circuits*, vol. 34, pp. 241–247, Feb. 1999.
[14] H. Morimura, S. Shigematsu, and K. Machida, "A high-resolution capacitive fingerprint sensing scheme with charge-transfer technique and automatic contrast emphasis," in *Dig. Tech. Papers Symp. VLSI Circuit*, June 1999, pp. 157–160.
[15] C. Tsikos, "Capacitive fingerprint sensor," U.S. Patent 4 353 056, Oct. 5, 1982.
[16] A. G. Knapp, "Fingerprint sensing device and recognition system having predetermined electrode activation," U.S. Patent 5 325 442, June 28, 1994.

Satoshi Shigematsu (M'93) was born in Tokyo, Japan, on August 2, 1967. He received the B.S. and M.E. degrees in system engineering from Tokyo Denki University, Tokyo, Japan, in 1990 and 1992, respectively.

In 1992 he joined Nippon Telegraph and Telephone Corp. (NTT), Tokyo. Since 1992, he has been engaged in the research and development of low-voltage, low-power CMOS circuits. He is now in the NTT Lifestyle and Environmental Technology Laboratories, Kanagawa, Japan. His research interests include biometrics sensor technology and low-power and high-speed circuit design technique. He is currently doing research on parallel processing circuits for CMOS fingerprint identifiers and developing single-chip fingerprint sensor and identifier LSI's.

Mr. Shigematsu is a member of the IEICEJ and Information Processing Society of Japan.

Hiroki Morimura (M'96) was born in Saitama, Japan, on January 9, 1968. He received the B.E. degree in physical electronics and the M.E. degree in applied electronics from Tokyo Institute of Technology, Tokyo, Japan, in 1991 and 1993, respectively.

In 1993, he joined Nippon Telegraph and Telephone Corp. (NTT), Tokyo. He has been engaged in the research and development of low-voltage, low-power SRAM circuits. He is currently doing research on sensing circuits for CMOS fingerprint sensors and developing single-chip fingerprint sensor and identifier LSI's.

Mr. Morimura is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

Takuya Adachi was born in Hyogo, Japan, on July 18, 1973. He received the B.S. and M.E. degrees in material science engineering from Osaka University, Osaka, Japan, in 1996 and 1998, respectively.

In 1998, he joined Nippon Telegraph and Telephone Corp. (NTT), Tokyo, Japan. He is now in the NTT Lifestyle & Environmental Technology Laboratories, Kanagawa, Japan. Since 1998, he has been engaged in the research and development of fingerprint identification algorithm.

Mr. Adachi is a member of the IEICEJ.

Yasuyuki Tanabe was born in Okayama, Japan, in 1953. He received the B.E. and M.E. degrees in electrical engineering from Waseda University, Tokyo, Japan, in 1976 and 1978, respectively.

Since joining NTT Electrical Communication Laboratories, Tokyo, in 1978, he has been engaged in research on high-speed silicon bipolar devices using polysilicon self-aligned process technology and the development of BiCMOS processes for telecommunications ASIC LSI's in NTT LSI Laboratories. He is now a Senior Research Engineer at NTT Telecommunications Energy Laboratories, Kanagawa, Japan.

Mr. Tanabe is a member of the Institute of Electronics, Information and Communication Engineers of Japan and the Japan Society of Applied Physics.

Katsuyuki Machida received the B.S., M.S., and Dr.Eng. degrees in electronics engineering from Kyushu Institute of Technology, Kitakyushu, Japan, in 1979, 1981, and 1995, respectively.

In 1981, he joined the Musashino Electrical Communication Laboratory, Nippon Telegraph and Telephone Public Corp. (NTT), Musashino, Tokyo, Japan. Since then, he has been engaged in the development of the interlayer dielectrics process for LSI multilevel interconnection. His current research interests includes the advanced functional device fabrication process and sensors for the mobile equipment. He is now a Senior Research Engineer, Supervisor, at the NTT Telecommunications Energy Laboratories, Atsugi, Kanagawa, Japan. He is an Associate Editor of the *Japanese Journal of Applied Physics*.

Dr. Machida is a member of the Japan Society of Applied Physics.